Am29C841A/Am29C843A

High Performance CMOS Bus Interface Latches

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-speed parallel latches**
  - D-Y propagation delay = 5 ns typical
- **Low standby power**
- **Very high output drive**
  - I_{OL} = 48 mA commercial, 32 mA Military
- **Extra-wide (9- and 10-bit) data paths**
- **Proprietary edge-rate controlled outputs dramatically reduce undershoots, overshoots, and ground bounce**
- **Power-up/down disable circuit provides for glitch-free power supply sequencing**
- **Can be powered off while in 3-state, ideal for card edge interface applications**
- **Minimal speed degradation with multiple outputs switching**
- **200 mV typical hysteresis on data input path**
- **JEDEC FCT-compatible specs**

GENERAL DESCRIPTION

The Am29C841A and Am29C843A CMOS Bus Interface Latches are designed to eliminate the extra devices required to buffer stand alone latches and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800A latches are produced with AMD's exclusive CS11SA CMOS process, and feature typical propagation delays of 5 ns, as well as an output current drive of 48 mA.

The Am29C841A is a buffered, 10-bit version of the popular '373 function. The Am29C843A is a 9-bit buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$)—ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C841A and Am29C843A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce) undershoots and overshoots. By controlling the output transient currents, ground bounce and output ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry which utilizes n-channel pull-up transistors (eliminating the parasitic diode to Vcc), provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C841A and Am29C843A are available in the standard package options: DIPs, PLCCs, and SOICs.

* For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

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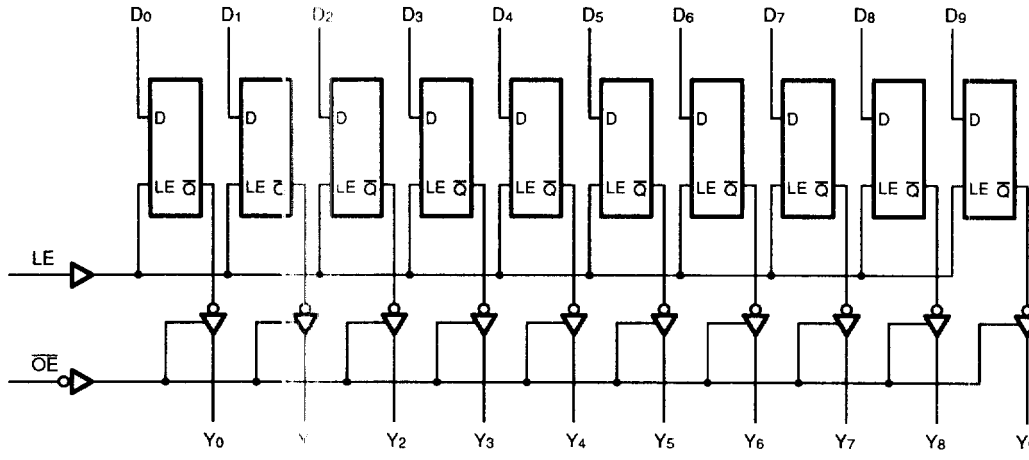
BLOCK DIAGRAMS
Am29C841A



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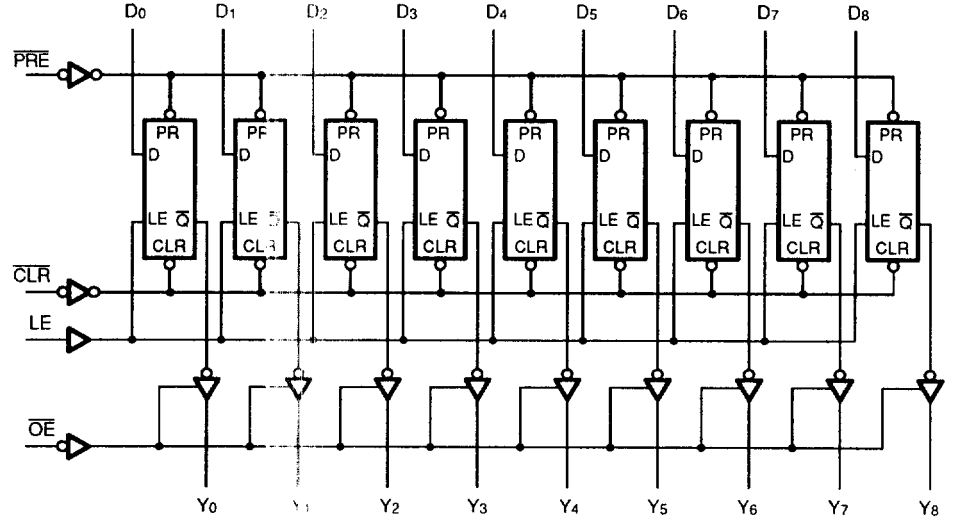
Am29C843A



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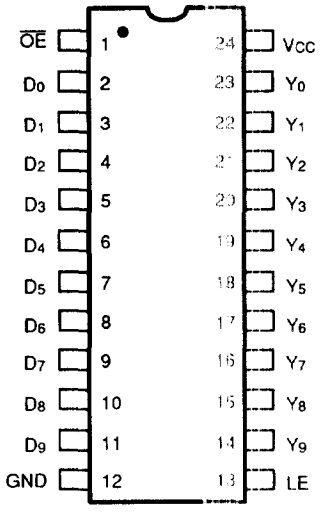
CONNECTION DIAGRAMS

Top View

Am29C841A

DIPs*



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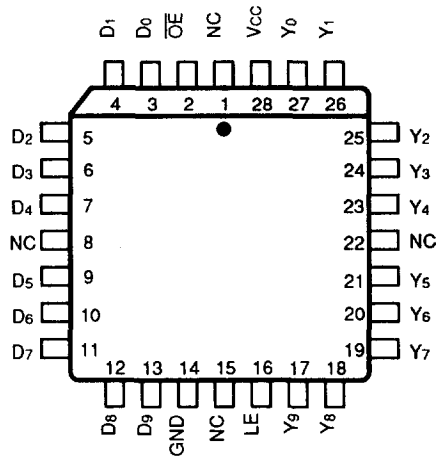
PLCC



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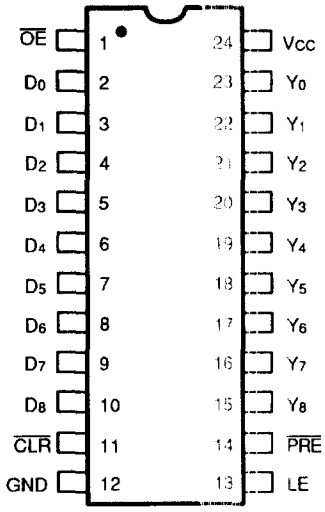
Am29C843A

DIPs*



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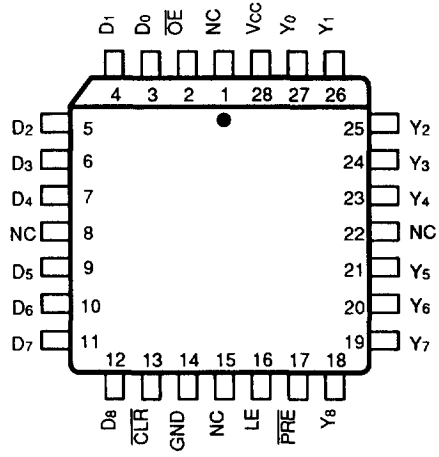
PLCC



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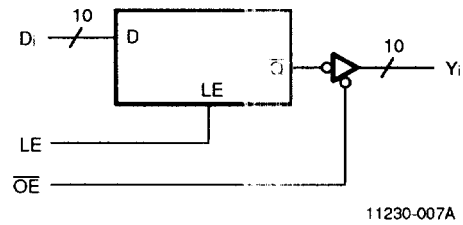
*Also available in 24-Pin Small Outline Package; pinout identical to DIPs.

Note:
Pin 1 is marked for orientation

LOGIC SYMBOLS

Am29C841A



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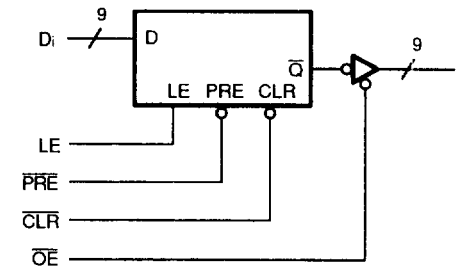
Am29C843A



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FUNCTION TABLES

Am29C841A

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	X	X	X	Z	Hi-Z
H	H	L	H	Z	Hi-Z
H	H	H	L	Z	Hi-Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

Am29C843A

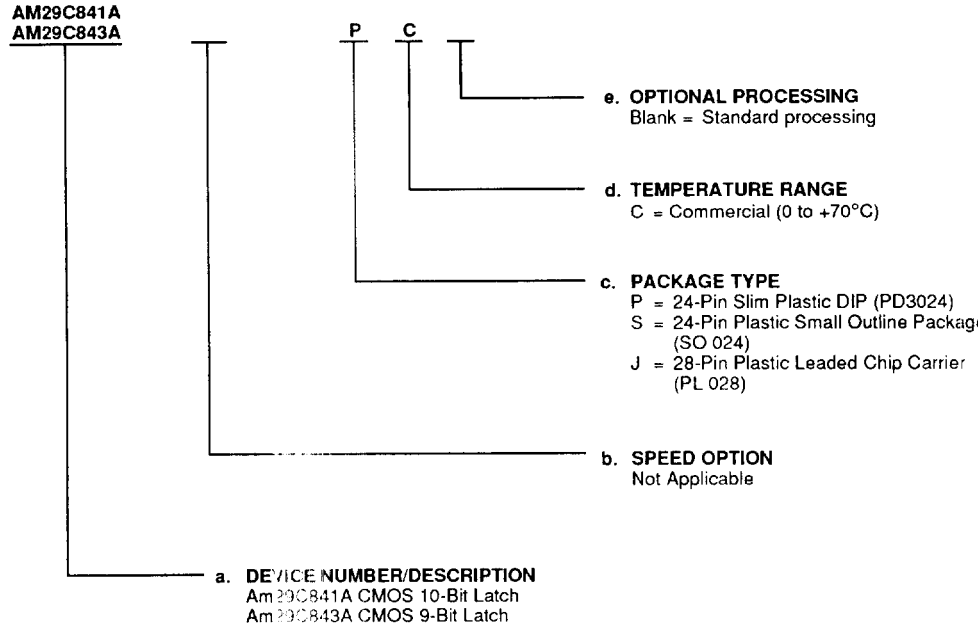
Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	L	Z	Hi-Z
H	H	H	H	H	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	L	H	Transparent
H	H	L	H	H	H	L	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

H = HIGH NC = No Change
L = LOW Z = High Impedance
X = Don't Care

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C841A	PC, SC, JC
AM29C843A	

Valid Combinations

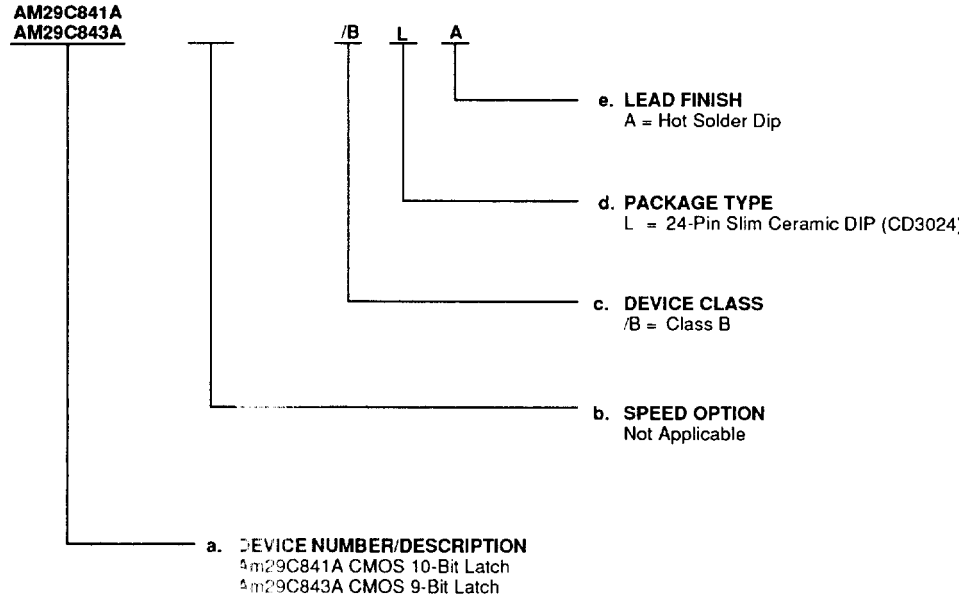
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Device Class**
d. **Package Type**
e. **Lead Finish**



Valid Combinations	
AM29C841A	/BLA
AM29C843A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C841A/Am29C843A

D_i

Data Inputs (Input)

D_i are the latch data inputs.

Y_i

Data Outputs (Output)

Y_i are the three state data outputs.

LE

Latch Enable (Input, Active HIGH)

The latches are transparent when LE is HIGH. Input data is latched on a HIGH-to-LOW transition.

$\overline{OE}$

Output Enable (Input, Active LOW)

When $\overline{OE}$ is LOW, the latch data is passed to the Y_i outputs. When $\overline{OE}$ is HIGH, the Y_i outputs are in the high impedence state.

Am29C843A Only

$\overline{PRE}$

Preset (Input, Active LOW)

When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides the $\overline{CLR}$ pin. $\overline{PRE}$ will set the latch independent of the state of $\overline{OE}$.

$\overline{CLR}$

Clear (Input, Active LOW)

When $\overline{CLR}$ is LOW, the internal latch is cleared. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW and $\overline{PRE}$ is HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7 V
DC Output Voltage	−0.5 V to +6 V
DC Input Voltage	−0.5 V to +6 V
DC Output Diode Current:	
Into Output	+ 50 mA
Out of Output	− 50 mA
DC Input Diode Current:	
Into Input	+ 20 mA
Out of Input	− 20 mA
DC Output Current per Pin:	
Into Output	+ 100 mA
Out of Output	− 100 mA
Total DC Ground Current	$(n \times I_{OL} + m \times I_{CCT})$ mA (Note 1)
Total DC V_{CC} Current	$(n \times I_{OH} + m \times I_{CCT})$ mA (Note 1)

Note:

1. n = number of outputs, m = number of inputs.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Military (M) Devices

Ambient Temperature (T_A)	−55 to +125°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V Min.	MIL I_{OL} = 32 mA			0.5	V
		V_{IN} = V_{IH} or V_{IL}	COM'L I_{OL} = 48 mA			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−5	µA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V				5	µA
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V				+10	µA
I_{OZL}		V_{CC} = 5.5 V, V_O = GND				−10	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 2)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/ Bit
				$\overline{OE}$, $\overline{PRE}$ $\overline{CLR}$, LE		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 3)		Outputs Open		275	µA/ MHz/ Bit
				Outputs Loaded		400	

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output should be shorted at a time. Duration should not exceed 100 milliseconds.
3. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS for light capacitive loading over operating ranges unless otherwise specified (for APL Products Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH) (Note 1)	C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω	2	7.5	2	8.5	ns
t_{PHL}			2	7.5	2	8.5	ns
t_S	Data to LE Setup Time		2.5		2.5		ns
t_H	Data to LE Hold Time		2.5		2.5		ns
t_{PLH}	Latch Enable (LE) to Y_i		1	8	1	9	ns
t_{PHL}			2	8	2	9	ns
t_{PLH}	Propogation Delay, Preset to Y_i		2	9	2	11	ns
t_{PHL}			2	9	2	11	ns
t_{REC}	Preset ($\overline{PRE}$ ↓) to LE Setup Time		4		4		ns
t_{PLH}	Propogation Delay, Clear to Y_i		2	11	2	12	ns
t_{PHL}			2	11	2	12	ns
t_{REC}	Clear ($\overline{CLR}$ ↓) to LE Setup Time		3		3		ns
t_{PWH}	LE Pulse Width HIGH		4		4		ns
t_{PWL}	Preset Pulse Width LOW		4		4		ns
t_{PWL}	Clear Pulse Width LOW		4		4		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↑ to Y_i		1	9	1	9.5	ns
t_{ZL}			3	12	3	13	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i		2	8	2	8.5	ns
t_{LZ}			2	8	2	8.5	ns

*See Switching Test Circuit and Waveforms listed in Chapter 2.

Note:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (Chapter 3).

SWITCHING CHARACTERISTICS for heavy capacitive loading over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description (Note 2)	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH) (Note 1)	C_L = 300 pF, R_1 = 500 Ω, R_2 = 500 Ω	2	14.5	2	16.0	ns
t_{PHL}			2	14.5	2	16.0	ns
t_{PLH}	Latch Enable (LE) to Y_i		2	16.5	2	18	ns
t_{PHL}			2	16.5	2	18	ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↓ to Y_i		2	16.5	2	17.0	ns
t_{ZL}			3	19.5	3	20.5	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i	C_L = 5 pF, R_1 = 500 Ω, R_2 = 500 Ω	2	7	2	7.5	ns
t_{LZ}			2	7	2	7.5	ns

*See Switching Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (Chapter 3).
2. These parameters are guaranteed by characterization but not production tested.