

## P-Channel 1.2 V (G-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
- 8	0.035 at V <sub>GS</sub> = - 4.5 V	- 11.7	21 nC
	0.042 at V <sub>GS</sub> = - 2.5 V	- 10.7	
	0.052 at V <sub>GS</sub> = - 1.8 V	- 9.6	
	0.069 at V <sub>GS</sub> = - 1.5 V	- 8.3	
	0.098 at V <sub>GS</sub> = - 1.2 V	- 1.02	

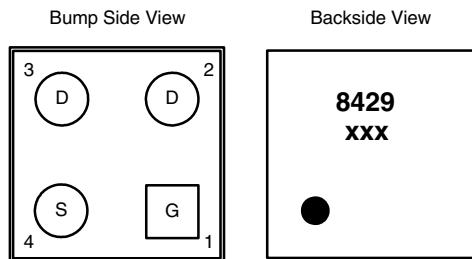
### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- Industry First 1.2 V Rated MOSFET
- Ultra Small MICRO FOOT<sup>®</sup> Chipscale Packaging Reduces Footprint Area, Profile (0.62 mm) and On-Resistance Per Footprint Area
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

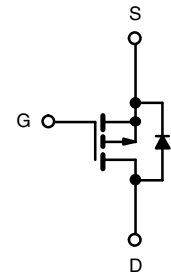
### MICRO FOOT



**Device Marking:** 8429  
xxx = Date/Lot Traceability Code

### APPLICATIONS

- Low Threshold Load Switch for Portable Devices
  - Low Power Consumption
  - Increased Battery Life
- Ultra Low Voltage Load Switch



P-Channel MOSFET

**Ordering Information:** Si8429DB-T1-E1 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	- 8	V	
Gate-Source Voltage	V <sub>GS</sub>	± 5		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	- 11.7	A
		T <sub>C</sub> = 70 °C	- 9.4	
		T <sub>A</sub> = 25 °C	- 7.8 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	- 6.3 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	- 25		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	- 5.7	
		T <sub>A</sub> = 25 °C	- 2.5 <sup>b, c</sup>	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	6.25	W
		T <sub>C</sub> = 70 °C	4	
		T <sub>A</sub> = 25 °C	2.77 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	1.77 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Package Reflow Conditions <sup>d</sup>	IR/Convection	260		

Notes:

- Based on T<sub>C</sub> = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
- In this document, any reference to the Case represents the body of the MICRO FOOT device and Foot is the bump.

**THERMAL RESISTANCE RATINGS**

Parameter	Symbol	Typ.	Max.	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	$R_{thJA}$	35	45	°C/W
Maximum Junction-to-Foot (Drain)	Steady State $R_{thJF}$	16	20	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under steady state conditions is 85 °C/W.

**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 8			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 7.5		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		- 2.2			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 0.35		- 0.8	V
		$V_{DS} = V_{GS}, I_D = -5\text{ mA}$		- 0.6		
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 8\text{ V}, V_{GS} = 0\text{ V}$			- 1	$\mu\text{A}$
		$V_{DS} = -8\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ °C}$			- 10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \leq 5\text{ V}, V_{GS} = -4.5\text{ V}$	- 5			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -1\text{ A}$		0.029	0.035	$\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -1\text{ A}$		0.035	0.042	
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		0.043	0.052	
		$V_{GS} = -1.5\text{ V}, I_D = -1\text{ A}$		0.051	0.069	
		$V_{GS} = -1.2\text{ V}, I_D = -1\text{ A}$		0.065	0.098	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -4\text{ V}, I_D = -1\text{ A}$		0.7	1.2	S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -4\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1640		pF
Output Capacitance	$C_{oss}$		590			
Reverse Transfer Capacitance	$C_{rss}$		380			
Total Gate Charge	$Q_g$	$V_{DS} = -4\text{ V}, V_{GS} = -5\text{ V}, I_D = -1\text{ A}$		24	26	nC
				21	32	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -4\text{ V}, V_{GS} = -4.5\text{ V}, I_D = 1\text{ A}$		1.8		
Gate-Drain Charge	$Q_{gd}$		3.7			
Gate Resistance	$R_g$	$V_{GS} = -0.1\text{ V}, f = 1\text{ MHz}$		22		$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$		12	20	ns
Rise Time	$t_r$		25	40		
Turn-Off Delay Time	$t_{d(off)}$		260	390		
Fall Time	$t_f$		155	240		



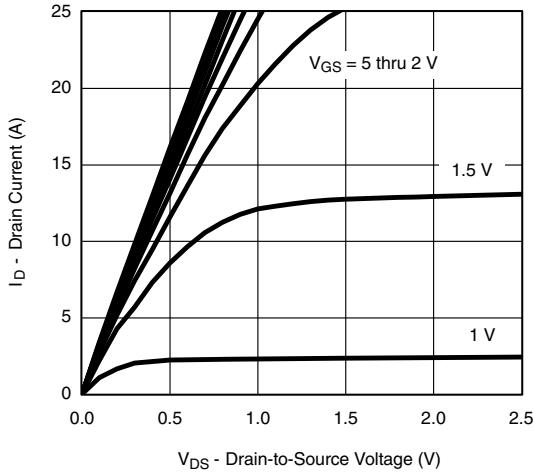
SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			- 2.5	A
Pulse Diode Forward Current	$I_{SM}$				- 25	
Body Diode Voltage	$V_{SD}$	$I_S = - 1\text{ A}, V_{GS} = 0\text{ V}$		- 0.7	- 1.1	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = - 1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		150	250	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			150	230	nC
Reverse Recovery Fall Time	$t_a$			57		ns
Reverse Recovery Rise Time	$t_b$			93		

Notes:

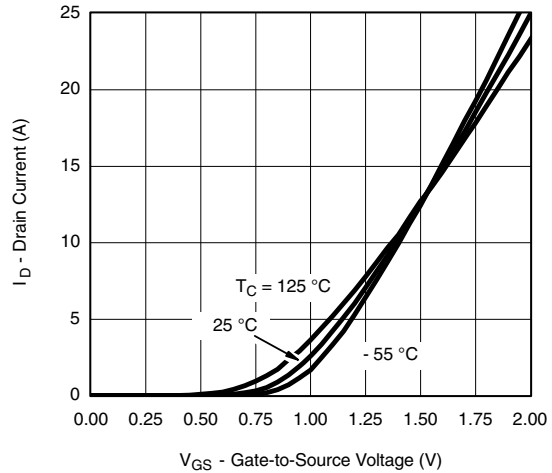
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

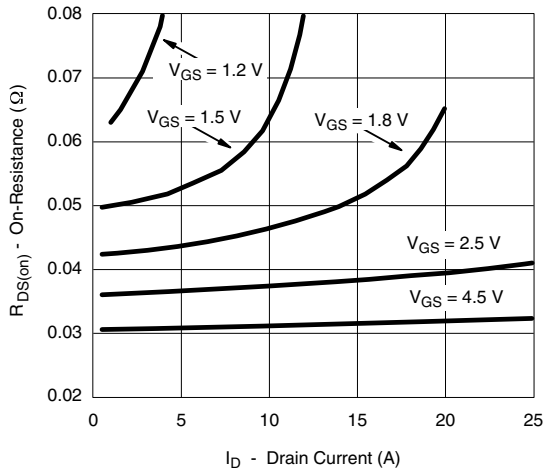
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



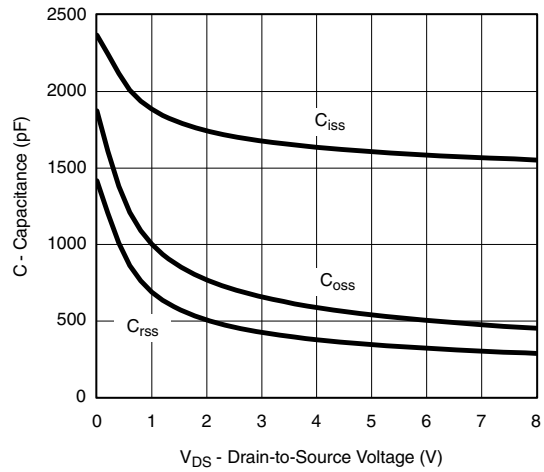
**Output Characteristics**



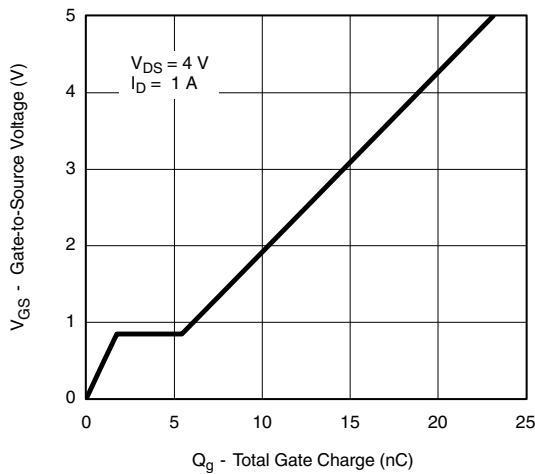
**Transfer Characteristics**



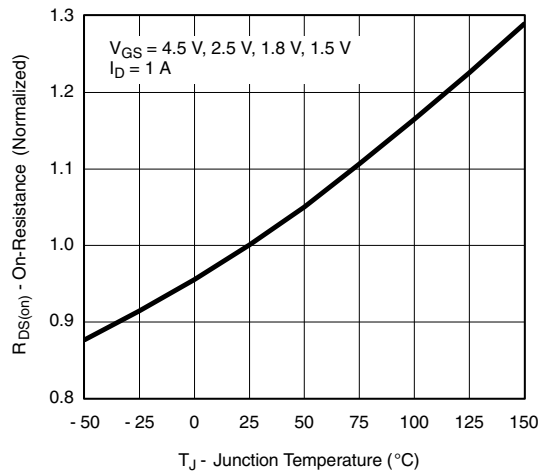
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

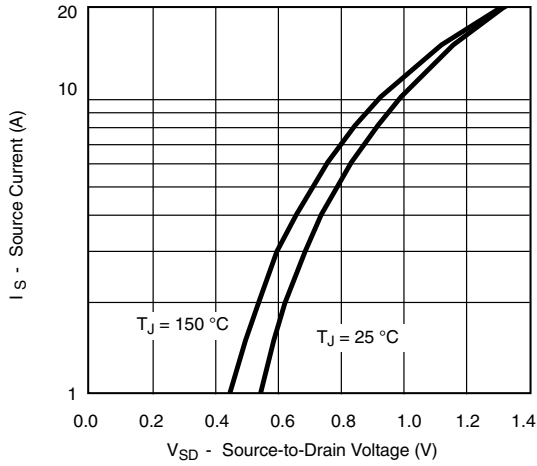


**Gate Charge**

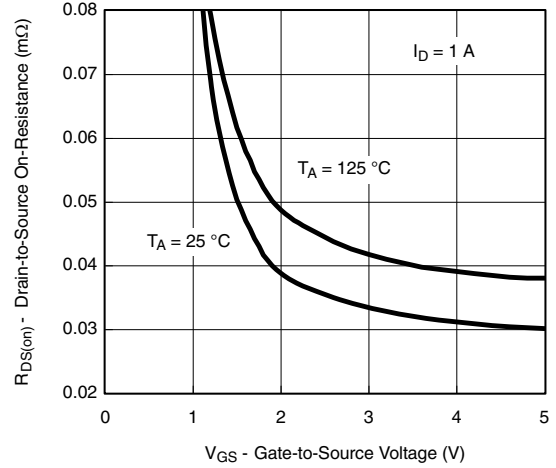


**On-Resistance vs. Junction Temperature**

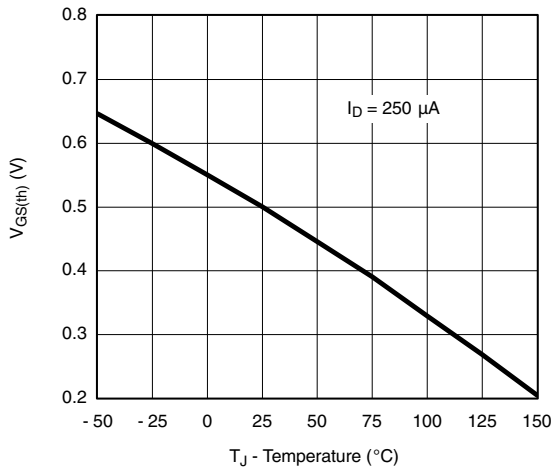
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



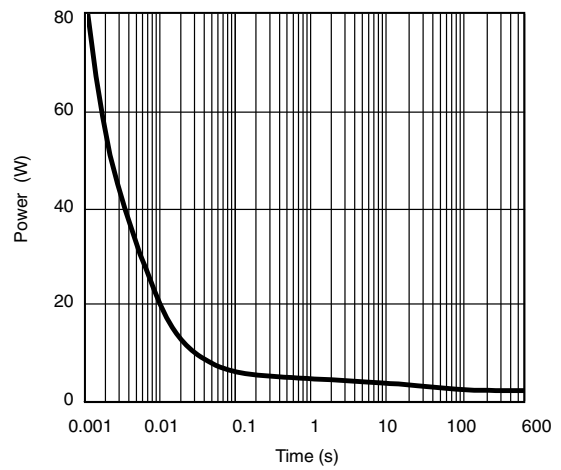
**Source-Drain Diode Forward Voltage**



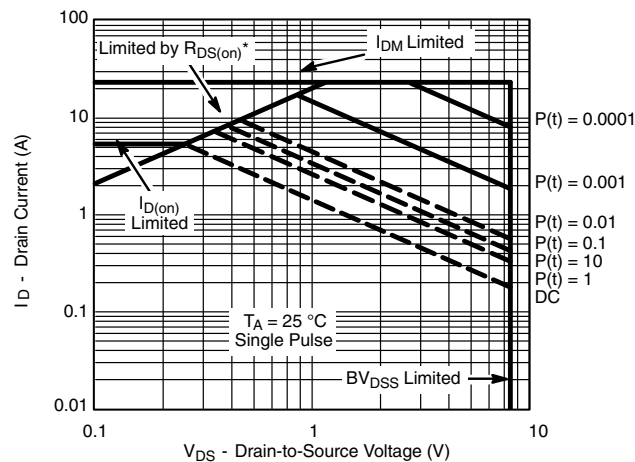
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



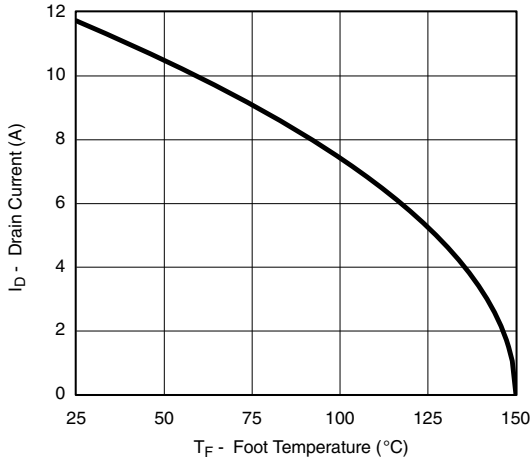
**Single Pulse Power, Junction-to-Ambient**



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

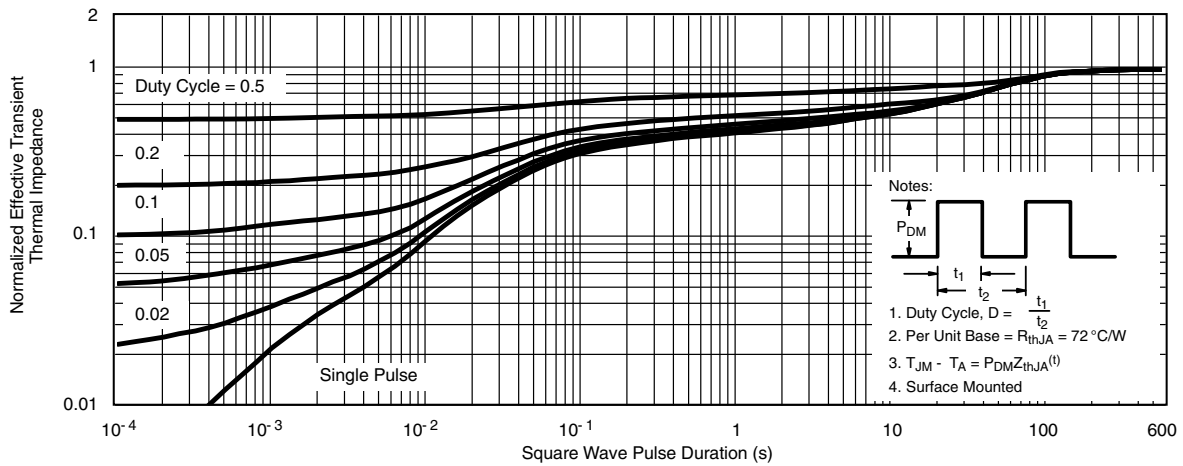
**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

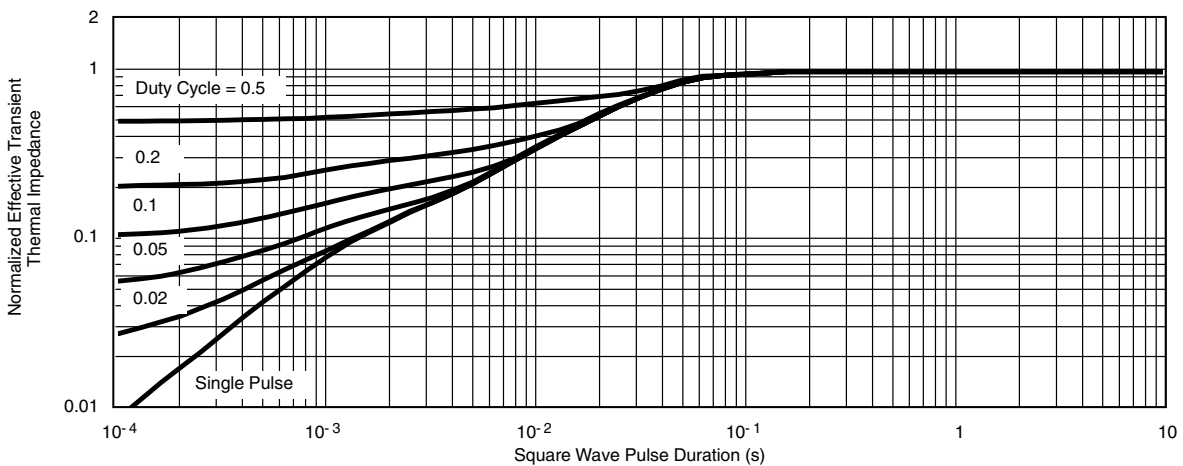


**Current Derating\***

\* The power dissipation P<sub>D</sub> is based on T<sub>J(max.)</sub> = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



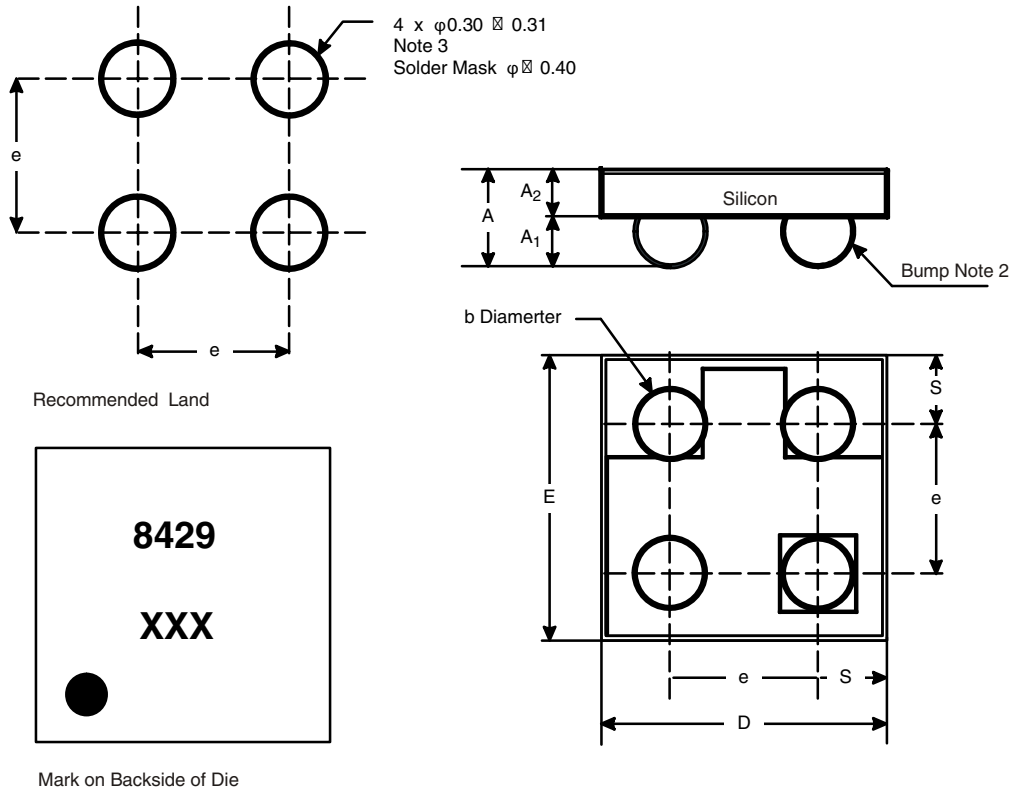
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

**PACKAGE OUTLINE**

**MICRO FOOT: 4-BUMP (0.8 mm PITCH)**



- Notes (unless otherwise specified):
1. Laser mark on the silicon die back, coated with a thin metal.
  2. Bumps are Sn/Ag/Cu.
  3. Non-solder mask defined copper landing pad.
  4. The flat side of wafers is oriented at the bottom.

Dim.	Millimeters <sup>a</sup>		Inches	
	Min.	Max.	Min.	Max.
<b>A</b>	0.600	0.650	0.0236	0.0256
<b>A<sub>1</sub></b>	0.260	0.290	0.0102	0.0114
<b>A<sub>2</sub></b>	0.340	0.360	0.0134	0.0142
<b>b</b>	0.370	0.410	0.0146	0.0161
<b>D</b>	1.520	1.600	0.0598	0.0630
<b>E</b>	1.520	1.600	0.0598	0.0630
<b>e</b>	0.800		0.0315	
<b>S</b>	0.360	0.400	0.0142	0.0157

- Notes:
- a. Use millimeters as the primary measurement

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?74399](http://www.vishay.com/ppg?74399).

## PCB Design and Assembly Guidelines For MICRO FOOT® Products

Johnson Zhao

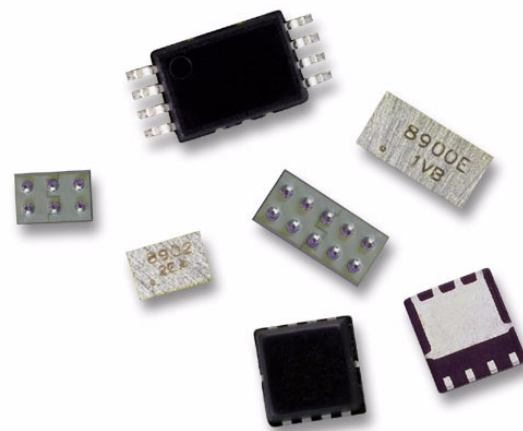
### INTRODUCTION

Vishay Siliconix's MICRO FOOT product family is based on a wafer-level chip-scale packaging (WL-CSP) technology that implements a solder bump process to eliminate the need for an outer package to encase the silicon die. MICRO FOOT products include power MOSFETs, analog switches, and power ICs.

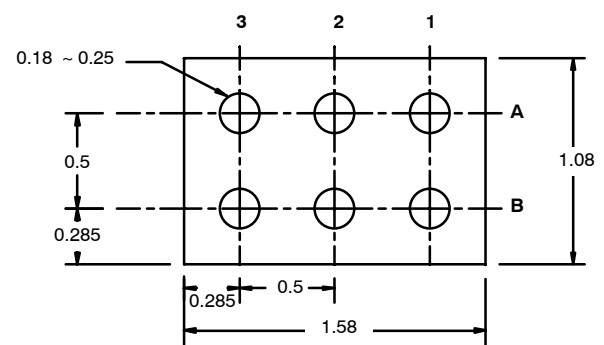
For battery powered compact devices, this new packaging technology reduces board space requirements, improves thermal performance, and mitigates the parasitic effect typical of leaded packaged products. For example, the 6-bump MICRO FOOT Si8902EDB common drain power MOSFET, which measures just 1.6 mm x 2.4 mm, achieves the same performance as TSSOP-8 devices in a footprint that is 80% smaller and with a 50% lower height profile (Figure 1). A MICRO FOOT analog switch, the 6-bump DG3000DB, offers low charge injection and 1.4 W on-resistance in a footprint measuring just 1.08 mm x 1.58 mm (Figure 2).

Vishay Siliconix MICRO FOOT products can be handled with the same process techniques used for high-volume assembly of packaged surface-mount devices. With proper attention to PCB and stencil design, the device will achieve reliable performance without underfill. The advantage of the device's small footprint and short thermal path make it an ideal option for space-constrained applications in portable devices such as battery packs, PDAs, cellular phones, and notebook computers.

This application note discusses the mechanical design and reliability of MICRO FOOT, and then provides guidelines for board layout, the assembly process, and the PCB rework process.



**FIGURE 1.** 3D View of MICRO FOOT Products Si8902EDB and Si8900EDB



**FIGURE 2.** Outline of MICRO FOOT CSP & Analog Switch DG3000DB



TABLE 1 Main Parameters of Solder Bumps in MICRO FOOT Designs				
MICRO FOOT CSP	Bump Material	Bump Pitch*	Bump Diameter*	Bump Height*
MICRO FOOT CSP MOSFET	Eutectic Solder: 63Sm/37Pb	0.8	0.37-0.41	0.26-0.29
MICRO FOOT CSP Analog Switch		0.5	0.18-0.25	0.14-0.19
MICRO FOOT UCSP Analog Switch		0.5	0.32-0.34	0.21-0.24

\* All measurements in millimeters

## MICRO FOOT'S DESIGN AND RELIABILITY

As a mechanical, electrical, and thermal connection between the device and PCB, the solder bumps of MICRO FOOT products are mounted on the top active surface of the die. Table 1 shows the main parameters for solder bumps used in MICRO FOOT products. A silicon nitride passivation layer is applied to the active area as the last masking process in fabrication, ensuring that the device passes the pressure pot test. A green laser is used to mark the backside of the die without damaging it. Reliability results for MICRO FOOT products mounted on a FR-4 board without underfill are shown in Table 2.

TABLE 2 MICRO FOOT Reliability Results	
Test Condition C: -65° to 150°C	>500 Cycles
Test condition B: -40° to 125°C	>1000 Cycles
121°C @ 15PSI 100% Humidity Test	96 Hours

The main failure mechanism associated with wafer-level chip-scale packaging is fatigue of the solder joint. The results shown in Table 2 demonstrate that a high level of reliability can be achieved with proper board design and assembly techniques.

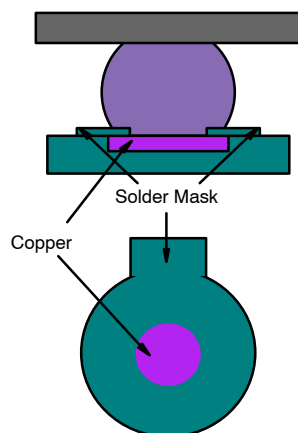


FIGURE 3. SMD

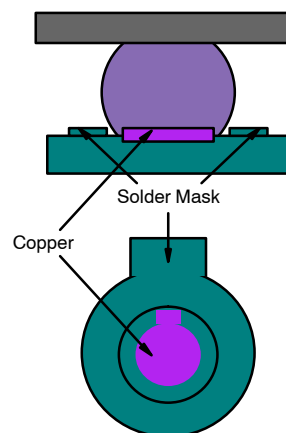


FIGURE 4. NSMD

## BOARD LAYOUT GUIDELINES

**Board materials.** Vishay Siliconix MICRO FOOT products are designed to be reliable on most board types, including organic boards such as FR-4 or polyamide boards. The package qualification information is based on the test on 0.5-oz. FR-4 and polyamide boards with NSMD pad design.

**Land patterns.** Two types of land patterns are used for surface-mount packages. Solder mask defined (SMD) pads have a solder mask opening smaller than the metal pad (Figure 3), whereas on-solder mask defined (NSMD) pads have a metal pad smaller than the solder-mask opening (Figure 4).

NSMD is recommended for copper etch processes, since it provides a higher level of control compared to SMD etch processes. A small-size NSMD pad definition provides more area (both lateral and vertical) for soldering and more room for escape routing on the PCB. By contrast, SMD pad definition introduces a stress-concentration point near the solder mask on the PCB side that may result in solder joint cracking under extreme fatigue conditions.

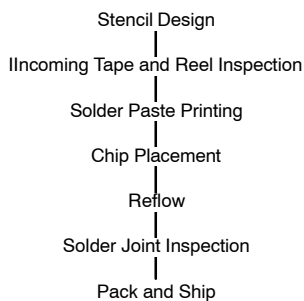
Copper pads should be finished with an organic solderability preservative (OSP) coating. For electroplated nickel-immersion gold finish pads, the gold thickness must be less than 0.5  $\mu\text{m}$  to avoid solder joint embrittlement.

**Board pad design.** The landing-pad size for MICRO FOOT products is determined by the bump pitch as shown in Table 3. The pad pattern is circular to ensure a symmetric, barrel-shaped solder bump.

<b>TABLE 3</b> <b>Dimensions of Copper Pad and Solder Mask Opening in PCB and Stencil Aperture</b>			
<b>Pitch</b>	<b>Copper Pad</b>	<b>Solder Mask Opening</b>	<b>Stencil Aperture</b>
0.80 mm	0.30 ± 0.01 mm	0.41 ± 0.01 mm	0.33 ± 0.01 mm in circle aperture
0.50 mm	0.17 ± 0.01 mm	0.27 ± 0.01 mm	0.30 ± 0.01 mm in square aperture

## ASSEMBLY PROCESS

MICRO FOOT products' surface-mount-assembly operations include solder paste printing, component placement, and solder reflow as shown in the process flow chart (Figure 5).



**FIGURE 5.** SMT Assembly Process Flow

**Stencil design.** Stencil design is the key to ensuring maximum solder paste deposition without compromising the assembly yield from solder joint defects (such as bridging and extraneous solder spheres). The stencil aperture is dependent on the copper pad size, the solder mask opening, and the quantity of solder paste.

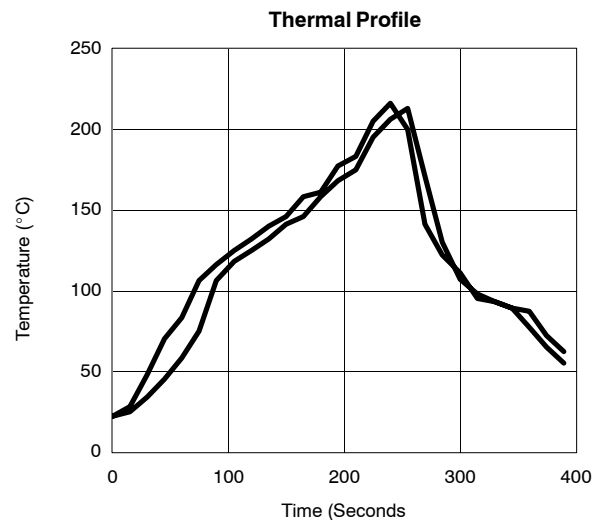
In MICRO FOOT products, the stencil is 0.125-mm (5-mils) thick. The recommended apertures are shown in Table 3 and are fabricated by laser cut.

**Solder-paste printing.** The solder-paste printing process involves transferring solder paste through pre-defined apertures via application of pressure.

In MICRO FOOT products, the solder paste used is UP78 No-clean eutectic 63 Sn/37Pb type3 or finer solder paste.

**Chip pick-and-placement.** MICRO FOOT products can be picked and placed with standard pick-and-place equipment. The recommended pick-and-place force is 150 g. Though the part will self-center during solder reflow, the maximum placement offset is 0.02 mm.

**Reflow Process.** MICRO FOOT products can be assembled using standard SMT reflow processes. Similar to any other package, the thermal profile at specific board locations must be determined. Nitrogen purge is recommended during reflow operation. Figure 6 shows a typical reflow profile.



**FIGURE 6.** Reflow Profile

## PCB REWORK

To replace MICRO FOOT products on PCB, the rework procedure is much like the rework process for a standard BGA or CSP, as long as the rework process duplicates the original reflow profile. The key steps are as follows:

1. Remove the MICRO FOOT device using a convection nozzle to create localized heating similar to the original reflow profile. Preheat from the bottom.
2. Once the nozzle temperature is +190°C, use tweezers to remove the part to be replaced.
3. Resurface the pads using a temperature-controlled soldering iron.
4. Apply gel flux to the pad.
5. Use a vacuum needle pick-up tip to pick up the replacement part, and use a placement jig to place it accurately.
6. Reflow the part using the same convection nozzle, and preheat from the bottom, matching the original reflow profile.



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**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.**

**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**