Six Output Peak Reducing EMI Solution

Features

- IC WORKS PREMIS™ family offering
- Generates an EMI optimized clocking signal at the output
- Selectable input to output frequency
- Six -1.25%, -3.75%, or 0% down spread outputs
- One non-Spread reference output
- Integrated loop filter components
- Operates with a 3.3 or 5V supply
- Low power CMOS design
- Available in 24-pin SSOP (Shrunk Small Outline Package)
- Outputs may be selectively disabled

Key Specifications

Supply Voltages:	VDD = 3.3V±0.3% or VDD = 5V±10%
Frequency range:	8MHz≤F_{in}≤28MHz
Crystal Reference range	8MHz≤F_{in}≤28MHz
Cycle to Cycle Jitter:	300ps (max)
Selectable spread percentage:	-1.25% or -3.75%
Output duty cycle:	40/60% (worst case)
Output rise and fall time:	5ns (max)

Figure 1 Simplified Block Diagram

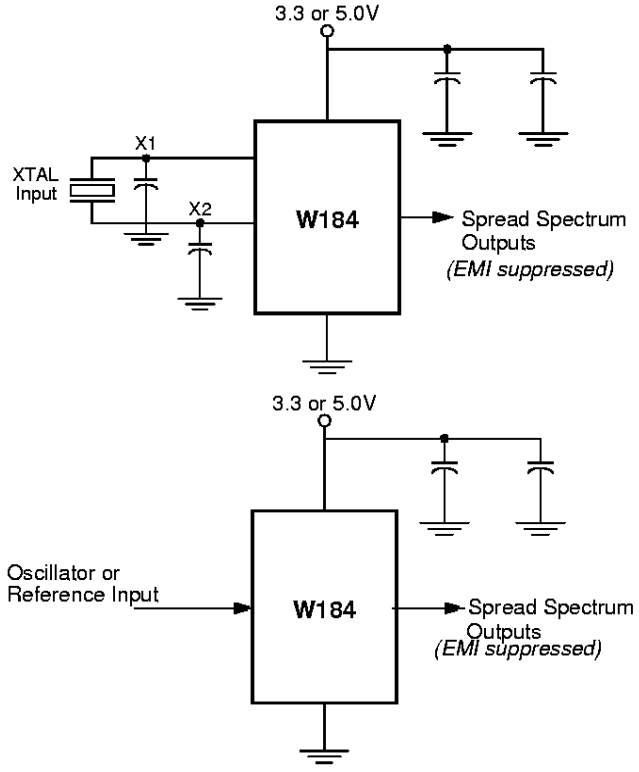


Table 1 Modulation width selection

SS%	Output
0	F_{in}≥F_{out}≥F_{in}-1.25%
1	F_{in}≥F_{out}≥F_{in}-3.75%

Table 2 Frequency Range Selection

FS2	FS1	Frequency range
0	0	8 MHz≤F_{IN} ≤10 MHz
0	1	10 MHz≤F_{IN} ≤15 MHz
1	0	15 MHz≤F_{IN} ≤18 MHz
1	1	18MHz≤F_{IN} ≤28 MHz

Figure 2 Pin Diagrams

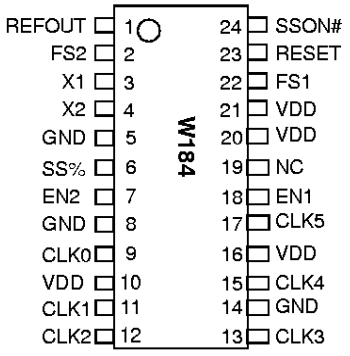


Table 3 Output Enable table

EN1	EN2	CLK0:4	CLK5
0	0	Low	Low
0	1	Low	Active
1	0	Active	Low
1	1	Active	Active

Table 4 Order Information

Part Number	Package
W184	H = Plastic SSOP (209 mil)

Overview

The W184 products are one series of devices in the IC WORKS PREMIS family. The PREMIS family incorporates the latest advances in PLL spread spectrum frequency synthesizer techniques. By frequency modulating the output with a low frequency carrier, peak EMI is greatly reduced. Use of this technology allows systems to pass increasingly difficult EMI testing without resorting to costly shielding or re-design.

In a system, not only is EMI reduced in the various clock lines, but also in all signals which are synchronized to the clock. Therefore, the benefits of using this technology increase with the number of address and data lines in the system. Figure 1 shows a simple implementation.

Functional Description

The W184 uses a phase locked loop (PLL) to frequency modulate an input clock. The result is an output clock whose frequency is slowly swept over a narrow band near the input signal. The basic circuit topology is shown in Figure 3. The input reference signal is divided by N and fed to the phase detector. A signal from the VCO is divided by M and fed back to the phase detector also. The PLL will force the frequency of the VCO output signal to change until the divided output signal and the divided reference signal match at the phase detector input. The output frequency is then equal to the ratio of M/N times the reference frequency. (Note: For the W184 the output frequency is nominally equal to the input frequency.) The unique feature of the Spread Spectrum Frequency Timing Generator is that a modulating waveform is superimposed at the input to the VCO. This causes the VCO output to be slowly swept across a predetermined frequency band.

Because the modulating frequency is typically 1000 times slower than the fundamental clock, the spread spectrum process has little impact on system performance.

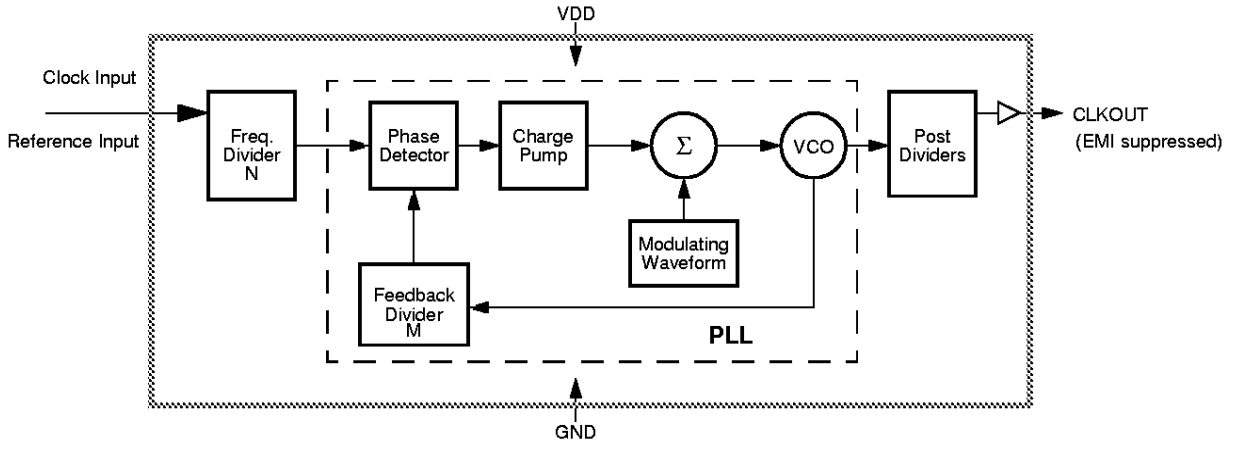
Frequency Selection With SSFTG

In Spread Spectrum Frequency Timing Generation, EMI reduction depends on the shape, modulation percentage, and frequency of the modulating waveform. While the shape and frequency of the modulating waveform are fixed for a given frequency, the modulation percentage may be varied.

Using frequency select bits (FS1:2 pins), the frequency range can be set. Spreading percentage may be selected to -1.25% or -3.75% (see Table 1).

A larger spreading percentage improves EMI reduction. However, large spread percentages may either exceed system maximum frequency ratings or lower the average frequency to a point where performance is affected. For these reasons, spreading percentage options are provided.

Figure 3 Functional Block Diagram

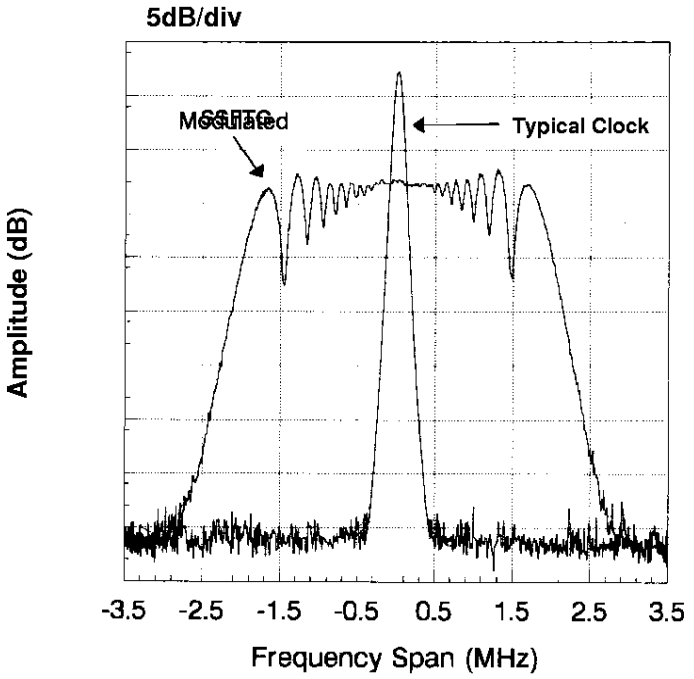


Spread Spectrum Frequency Timing Generation

The benefits of using Spread Spectrum Frequency Timing Generation are depicted in Figure 4. An EMI emission profile of a clock harmonic is shown.

Contrast the typical clock EMI with the IC WORKS Spread Spectrum Frequency Timing Generation EMI. Notice the spike in the typical clock. This spike can make systems fail quasi-peak EMI testing. The FCC and other regulatory agencies test for peak emissions. With spread spectrum enabled, the peak energy is much lower (at least 8dB) because the energy is spread out across a wider bandwidth.

Figure 4 Typical Clock and SSFTG Comparison



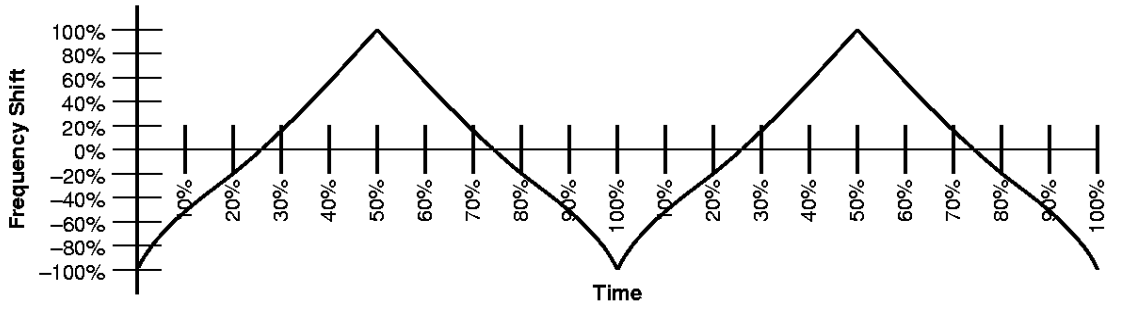
Modulating Waveform

The shape of the modulating waveform is critical to EMI reduction. The modulation scheme used to accomplish the maximum reduction in EMI is shown in Figure 5. The period of the modulation is shown as a percentage of the period length along the X axis. The amount that the frequency is varied is shown along the Y axis, also shown as a percentage of the total frequency spread.

IC WORKS frequency selection tables express the modulation percentage in two ways. The first method displays the spreading frequency band as a percent of the programmed average output frequency, symmetric about the programmed average frequency. This method is always shown using the expression $f_{Center} \pm X_{MOD}\%$ in the frequency spread selection table.

The second approach is to specify the maximum operating frequency and the spreading band as a percentage of this frequency. The output signal is swept from the lower edge of the band to the maximum frequency. The expression for this approach is f_{MAX} - $X_{MOD}\%$. Whenever this expression is used, IC WORKS has taken care to ensure that f_{MAX} will never be exceeded. This is important in applications where the clock drives components with tight maximum clock speed specifications.

Figure 5 Modulation Waveform Profile



SSON# Pin

An internal pull-down resistor defaults the chip into spread spectrum mode. When the SSON# pin is asserted (active low) the spreading feature is enabled. Spreading feature is disabled when SSON# is set high (V_{DD}).

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CLK0:5	9, 11, 12, 13, 15, 17	O	***Modulated Frequency Outputs:*** Frequency modulated copies of the unmodulated input clock (SSON# asserted).
CLKIN or X1	3	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It may either be connected to an external crystal, or to an external reference clock.
NC or X2	4	I	***Crystal Connection:*** If using an external reference, this pin must be left unconnected.
SS%	6	I	***Modulation Width Selection:*** When Spread Spectrum feature is turned on, this pin is used to select the amount of variation and peak EMI reduction that is desired on the output signal. This pin has an internal pull-up resistors.
Reset	23	I	***Modulation profile restart:*** A rising edge on this input restarts the modulation pattern at the beginning of its defined path.
REFOUT	14	O	***Non-Modulated Output:*** This pin provides a copy of the reference frequency. This output will not have the Spread Sepcturm feature enabled regardless of the state of logic input SSON#.
EN1:2	18, 7	I	***Output Enable Select Pins:*** These pins control the activity of specific output buffers. Set them to disable unused outputs using Table 3 on page 1 as a guide.
SSON#	24	I	***Spread Spectrum Control (Active Low):*** Asserting this signal (active low) turns the internal modulation waveform on. This pin has an internal pull-down resistor.
FS1:2	22, 2	I	***Frequency Selection Bit 1 and 2:*** These pins select the frequency of operation. Refer to Table 1. These pins have internal pull-up resistors.
VDD	10, 16, 20, 21	P	***Power Connection:*** Connected to 3.3V or 5V power supply.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Operating at maximum conditions for extended periods may affect reliability.

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	℃
T_A	Operating Temperature	0 to +70	℃
T_B	Ambient Temperature under Bias	–55 to +125	℃
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: $0℃ < T_A < 70℃$, $V_{DD} = 3.3V \pm 0.3V$

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{DD}	Supply Current		18	32	mA	
t_{ON}	Power Up Time			5	ms	First locked clock cycle after Power Good
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	
V_{OH}	Output High Voltage	2.4			V	
I_{IL}	Input Low Current	-50			µA	Note 1
I_{IH}	Input High Current			50	µA	Note 1
I_{OL}	Output Low Current		15		mA	@ 0.4V, $V_{DD} = 3.3V$
I_{OH}	Output High Current		15		mA	@ 2.4V, $V_{DD} = 3.3V$
C_I	Input Capacitance			7	pF	All pins except CLKIN
C_I	Input Capacitance		6	10	pF	CLKIN pin only
R_P	Input Pull-Up Resistor		500		kΩ	
Z_{OUT}	Clock Output Impedance		25		Ω	

Note 1: Inputs FS1:2, SS% have a pull-up resistor, Input SSON# has a pull-down resistor.

DC Electrical Characteristics: $0°C < T_A < 70°C$, $V_{DD} = 5V \pm 10\%$

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{DD}	Supply Current		30	50	mA	
t_{ON}	Power Up Time			5	ms	First locked clock cycle after Power Good
V_{IL}	Input Low Voltage			$0.15V_{DD}$	V	
V_{IH}	Input High Voltage	$0.7V_{DD}$			V	
V_{OL}	Output Low Voltage			0.4	V	
V_{OH}	Output High Voltage	2.4			V	
I_{IL}	Input Low Current	–50			µA	Note 1
I_{IH}	Input High Current			50	µA	Note 1
I_{OL}	Output Low Current		24		mA	@ 0.4V, V_{DD} = 5V
I_{OH}	Output High Current		24		mA	@ 2.4V, V_{DD} = 5V
C_I	Input Capacitance			7	pF	All pins except CLKIN
C_I	Input Capacitance		6	10	pF	CLKIN pin only
R_P	Input Pull-Up Resistor		500		kΩ	
Z_{OUT}	Clock Output Impedance		25		Ω	

Note 1: Inputs FS1:2 have a pull-up resistor, Input SSON# has a pull-down resistor.

AC Electrical Characteristics: $T_A = 0°C$ to $+70°C$, $V_{DD} = 3.3V \pm 0.3V$ or $5V \pm 10\%$

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
f_{IN}	Input Frequency	8		28	MHz	Input Clock
f_{OUT}	Output Frequency	8		28	MHz	Spread Off
t_R	Output Rise Time		2	5	ns	V_{DD}, 15pF load 0.8V - 2.4V
t_F	Output Fall Time		2	5	ns	V_{DD}, 15pF load 2.4V - 0.8V
t_{OD}	Output Duty Cycle	40		60	%	15pF load
t_{ID}	Input Duty Cycle	40		60	%	
t_{JCYC}	Jitter, Cycle-to-Cycle		250	300	ps	
EMI_{RED}	Harmonic Reduction	8			dB	f_{out} = 40MHz, third harmonic measured, reference board, 15pF load
t_{SK}	Output to Output Skew			200	ps	

Application Information

Recommended Circuit Configuration

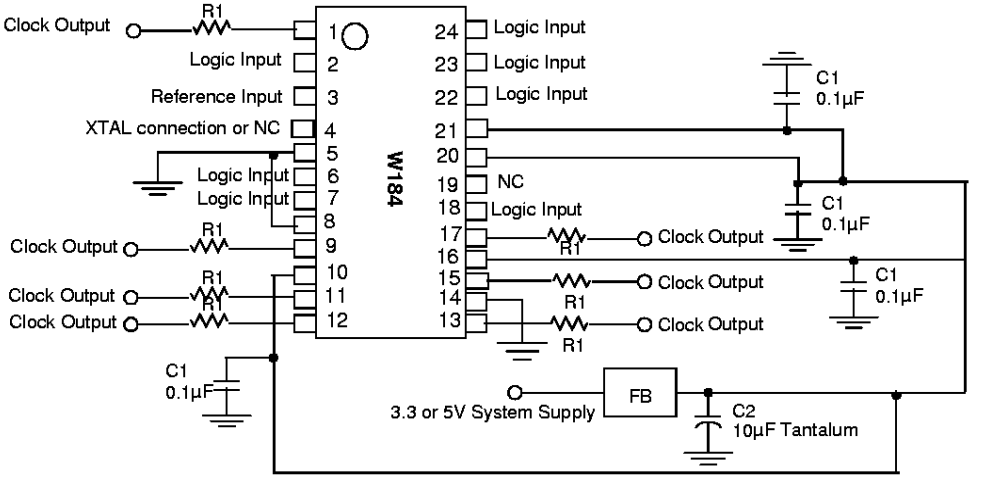
For optimum performance in system applications the power supply decoupling scheme shown in Figure 6 should be used.

VDD decoupling is important to both reduce phase jitter and EMI radiation. The 0.1µF decoupling capacitor should be placed as close to the V_{DD} pin as possible, otherwise the increased trace inductance will negate its decoupling capability. The 10µF decoupling capacitor shown should be a tantalum type. For further EMI protection, the V_{DD} connection can be made via a ferrite bead, as shown.

Recommended Board Layout

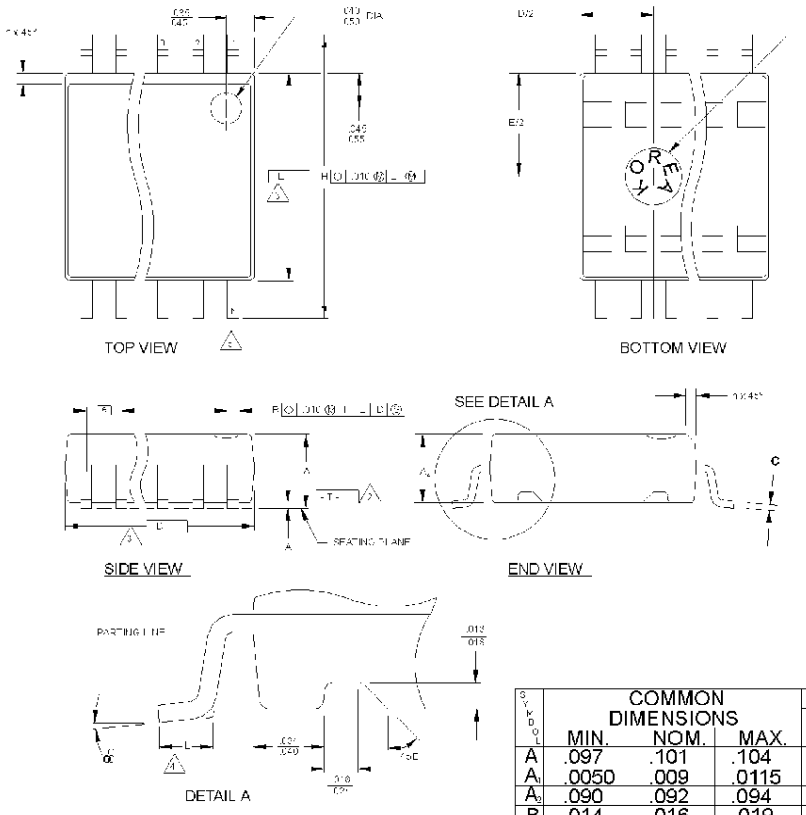
Figure 7 shows a recommended 2-layer board layout.

Figure 6 Recommended Circuit Configuration



Mechanical Package Outline

Figure 7 Shrink Small Outline Package, (SSOP, 209mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCES PER ANSI. Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
10. THE POCKETS ON THE BOTTOM ARE OPTIONAL.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	NOTE VARIATIONS	3 D MIN.	NOM.	MAX.	5 N
A	.097	.101	.104		AA	.402	.407	.412	16
A_1	.0050	.009	.0115		AB	.451	.456	.461	18
A_2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e	.050 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
∅	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	NOTE VARIATIONS	3 D MIN.	NOM.	MAX.	5 N
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A_1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A_2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e	1.27 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
∅	0°	5°	8°						
X	2.16	2.36	2.54						