Standard Products

UT8ER512K32 Monolithic 16M RadHard SRAM

Preliminary Data Sheet

May 21, 2007
www.aeroflex.com/radhardsram

FEATURES

- 20ns read, 10ns write maximum access times
- Functionally compatible with traditional 512K x 32 SRAM devices
- CMOS compatible inputs and output levels, three-state bidirectional data bus
  - 3.3 volt I/O, 1.8 volt core
- Radiation performance
  - Total-dose: >100Krad(Si)
  - SEL Immune: 100MeV-cm^2/mg
  - SEU error rate = 6.01x10^{-16} errors bit/day assuming geosynchronous orbit, Adam's 90% worst environment, and 156KHz default scrub rate (=99.4% SRAM availability)
  - Neutron Fluence: 3.0E14n/cm^2
  - Dose Rate
    - Upset TBD rad(Si)/sec
    - Latchup TBD rad(Si)/sec
- Packaging options:
  - 68-lead ceramic quad flatpack (6.898 grams)
- Standard Microcircuit Drawing 5962-06261
  - QML compliant part

INTRODUCTION

The UT8ER512K32 is a high-performance CMOS static RAM organized as 524,288 words by 32 bits. Easy memory expansion is provided by active LOW and HIGH chip enables ($\overline{E1}$, E2), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to the device is accomplished by driving chip enable one ($\overline{E1}$) input LOW, chip enable two (E2) HIGH and write enable ($\overline{W}$) input LOW. Data on the 32 I/O pins (DQ0 through DQ31) is then written into the location specified on the address pins (A0 through A18). Reading from the device is accomplished by taking chip enable one ($\overline{E1}$) and output enable ($\overline{G}$) LOW while forcing write enable ($\overline{W}$) and chip enable two (E2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The 32 input/output pins (DQ0 through DQ31) are placed in a high impedance state when the device is deselected ($\overline{E1}$ HIGH or E2 LOW), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E1}$ LOW, E2 HIGH and $\overline{W}$ LOW).

UT8ER512K32 Master or Slave Options

To reduce bit error rates caused by single event phenomenon in space, the UT8ER512K32 employs an embedded EDAC (error detection and correction) with code engine with auto scrubbing. When a double bit error occurs in a word, the UT8ER512K32 asserts an $\overline{MBE}$ output to the host.

The UT8ER512K32 is offered in two options: Master or Slave. The UT8ER512K32M (Master) is a full function device capable of autonomous EDAC scrubbing which can also be used to demand scrub cycles on the UT8ER512K32S (Slave) by connecting the SCRUB pins on each device. The UT8ER512K32S (Slave) only performs EDAC scrub cycles when its SCRUB pin is driven by an external controller. The scrub-on-demand feature allows multiple UT8ER512K32S (Slave) devices to be controlled by one UT8ER512K32M (Master) device. The $\overline{SCRUB}$ function is a no connect (NC) on the UT8ER512K32S (Slave), and is used by the UT8ER512K32M (Master) to generate wait states in the memory controller. The $\overline{BUSY}$ function is an output on the Master device while on the Slave device it is an input.

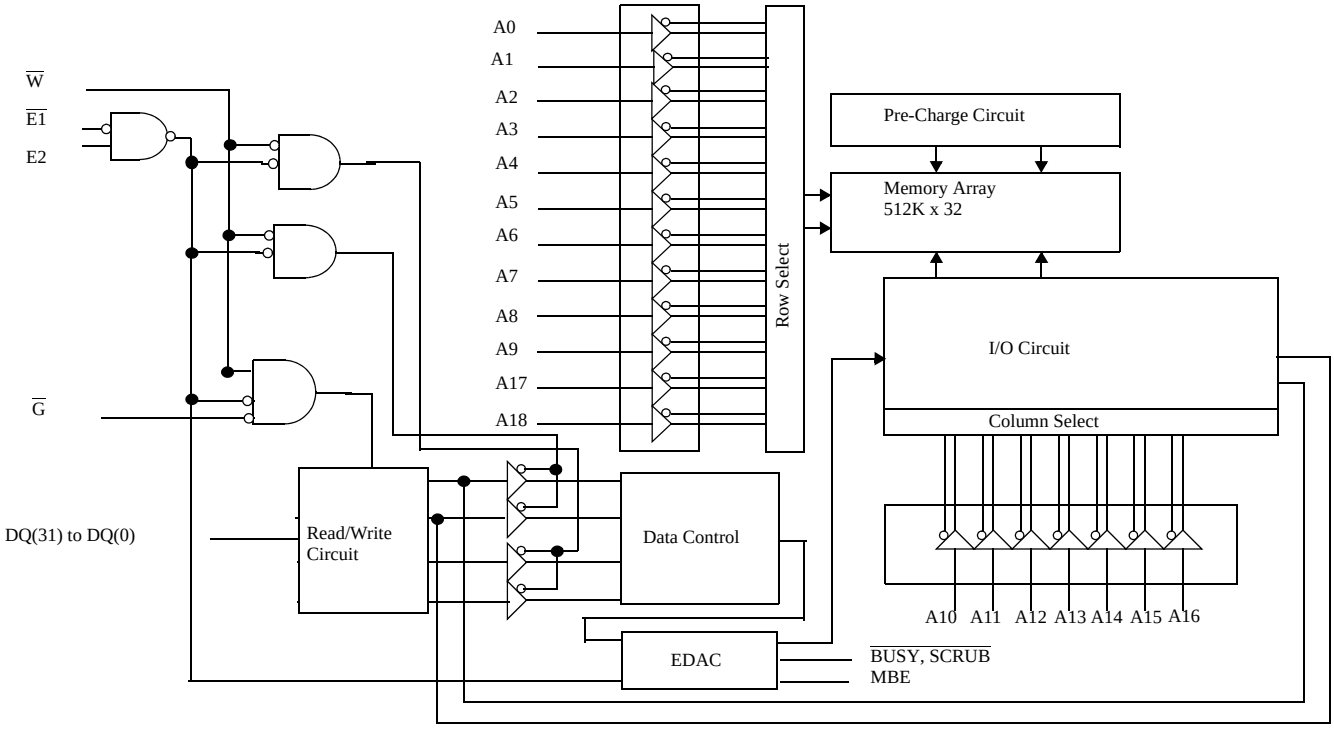


Figure 1. UT8ER512K32 SRAM Block Diagram

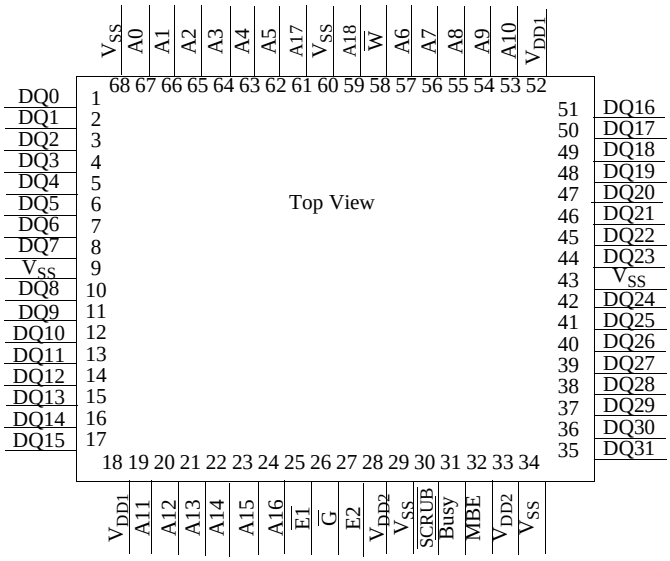


Figure 2. 20ns SRAM Pinout (68)

Note: Pin 30 on the UT8ER512K32S (Slave) is a no connect (NC).

PIN DESCRIPTIONS

Pins	Type	Description
A(18:0)	I	Address
DQ(31:0)	BI	Data Input/Output
$\overline{E1}$	I	Enable (Active Low)
E2	I	Enable (Active High)
$\overline{W}$	I	Write Enable
$\overline{G}$	I	Output Enable
V_{DD1}	P	Power (1.8)
V_{DD2}	P	Power (3.3V)
V_{SS}	P	Ground
MBE	TTO	Multiple Bit Error
$\overline{SCRUB}$	I	Slave SCRUB Input
$\overline{SCRUB}$	O	Master SCRUB Output
$\overline{BUSY}$	NC	Slave No Connect
$\overline{BUSY}$	O	Master Wait State Control

DEVICE OPERATION

The UT8ER512K32 has four control inputs called Enable 1 ($\overline{E1}$), Enable 2 (E2), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); 19 address inputs, A(18:0); and 32 bidirectional data lines, DQ(31:0). $\overline{E1}$ and E2 device enables control device selection, active, and standby modes. Asserting $\overline{E1}$ and E2 enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. SRAM Device Control Operation Truth Table

$\overline{G}$	$\overline{W}$	E2	$\overline{E1}$	I/O Mode	Mode
X	X	X	H	DQ(31:0) 3-State	Standby
X	X	L	X	DQ(31:0) 3-State	Standby
L	H	H	L	DQ(31:0) Data Out	Word Read
X	L	H	L	DQ(31:0) Data In	Word Write
H	X	X	L	DQ(31:0) All 3-State	3-State

Notes:
1. “X” is defined as a “don’t care” condition.
2. Device active; outputs disabled.

Table 2. EDAC Control Pin Operation Truth Table

MBE	$\overline{SCRUB}$	$\overline{BUSY}$	I/O Mode	Mode
H	H	H	Read	Uncorrectable Bit Error
L	H	H	Read	Valid Data Out
X	H	H	X	Device Ready
X	H	L	X	Device Ready / Early Scrub Request Coming
X	L	X	Not Accessible	Device Busy

Notes:
1. “X” is defined as a “don’t care” condition

READ CYCLE

A combination of $\overline{W}$ and E2 greater than V_{IH} (min) and $\overline{E1}$ and $\overline{G}$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(31:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the minimum time between valid address changes is specified by the read cycle time (t_{AVAV}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b, is initiated by the latter of either $\overline{E1}$and E2 going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the 32-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(31:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by $\overline{G}$ going active while $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} (reference Figure 3b) have not been satisfied.

SRAM EDAC Status Indications during a Read Cycle, if MBE is Low, the data is good. If MBE is High the data is corrupted.

WRITE CYCLE

A combination of $\overline{W}$ and $\overline{E1}$ less than V_{IL}(max) and E2 greater than V_{IH}(min) defines a write cycle. The state of $\overline{G}$ is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 4a, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ and E2 still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{E1}$ and E2. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the t_{WLQZ} before applying data to the 32 bidirectional pins DQ(31:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 4b, is defined by a write terminated by the latter of $\overline{E1}$ or E2 going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by either $\overline{E1}$or E2 going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the thirty-two bidirectional pins DQ(31:0) to avoid bus contention.

MEMORY SCRUBBING/CYCLE STEALING

The UT8ER512K32 SRAM uses architectural improvements and embedded error detection and correction to maintain unsurpassed levels of SEU protection. This is accomplished by what Aeroflex refers to as Cycle Stealing. To minimize the system design impact for reduced speed operation, the edge relationship between $\overline{BUSY}$ and $\overline{SCRUB}$ is programmable via the sequence described in figure 5a.

The effective error rate will be flux dependent (rate at which radiation is applied) and not simply LET dependent. As a result, some users may desire an increased scrub rate to lower the error rate at the sacrifice of reduced total throughput, while others may desire a lower scrub rate to increase the total throughput and accept a higher error rate in a low flux environment. This rate at which the SRAM controller will correct errors from the memory is user programmable. The required sequence is described in figure 5a.

Data is corrected not only during the internal scrub, but again during a user requested read cycle. The MBE signal is asserted once the data is valid (t_{AVAV}), if the data presented contains at least two errors and should be considered corrupt. (Note: Reading un-initialized memory locations may result in un-intended MBE assertions.)

RADIATION HARDNESS

The UT8ER512K32 SRAM incorporates special design, layout, and process features which allows operation in a limited radiation environment.

Table 3. Radiation Hardness Design Specifications[1]

Total Dose	100K	rad(Si)
Heavy Ion Error Rate[2]	TBD	Errors/Bit-Day

Notes:

1. The SRAM is immune to latchup to particles >100MeV-cm^2/mg.
2. 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum.

SUPPLY SEQUENCING

No supply voltage sequencing is required between V_{DD1} and V_{DD2}.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage (Core)	-0.3 to 2.0V
V_{DD2}	DC supply voltage (I/O)	-0.3 to 3.8V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.8V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.2W
T_J	Maximum junction temperature	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[2]	5°C/W
I_I	DC input current	±5 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage (Core)	1.7 to 1.9V
V_{DD2}	DC supply voltage (I/O)	3.0 to 3.6V
T_C	Case temperature range	(C) Screening: -55 to +125°C (W) Screening: -40 to +125°C
V_{IN}	DC input voltage	0V to V_{DD2}

DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)*

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage		0.7*V_{DD2}		V
V_{IL}	Low-level input voltage			0.3*V_{DD2}	V
V_{OL}	Low-level output voltage	I_{OL} = 8mA,V_{DD2} =V_{DD2} (min)		0.2*V_{DD2}	V
V_{OH}	High-level output voltage	I_{OH} = -4mA,V_{DD2} =V_{DD2} (min)	0.8*V_{DD2}		V
C_{IN}[1]	Input capacitance	*f* = 1MHz @ 0V		12	pF
C_{IO}[1]	Bidirectional I/O capacitance	*f* = 1MHz @ 0V		12	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD2} and V_{SS}	-2	2	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD2} and V_{SS} V_{DD2} = V_{DD2} (max), $\overline{G}$ = V_{DD2} (max)	-2	2	µA
I_{OS}[2, 3]	Short-circuit output current	V_{DD2} = V_{DD2} (max), V_O = V_{DD2} V_{DD2} = V_{DD2} (max), V_O = V_{SS}	-100	+100	mA
$I_{DD1}(OP_1)$	V_{DD1} Supply current operating @ 1MHz	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		25	mA
$I_{DD1}(OP_2)$	V_{DD1} Supply current operating @ 50MHz,	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		200	mA
$I_{DD2}(OP_1)$	V_{DD2} Supply current operating @ 1MHz	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		1	mA
$I_{DD2}(OP_2)$	V_{DD2} Supply current operating @ 50MHz,	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		12	mA
$I_{DD1}(SB)$[4]	Supply current standby @ 0Hz	CMOS inputs , I_{OUT} = 0 $\overline{E1}$ = V_{DD2} -0.2, E2 = GND V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		25	mA
$I_{DD2}(SB)$[4]				100	µA
$I_{DD1}(SB)$[4]	Supply current standby A(16:0) @ 50MHz	CMOS inputs , I_{OUT} = 0 $\overline{E1}$ = V_{DD2} - 0.2, E2 = GND, V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		25	mA
$I_{DD2}(SB)$[4]				100	µA

Notes:

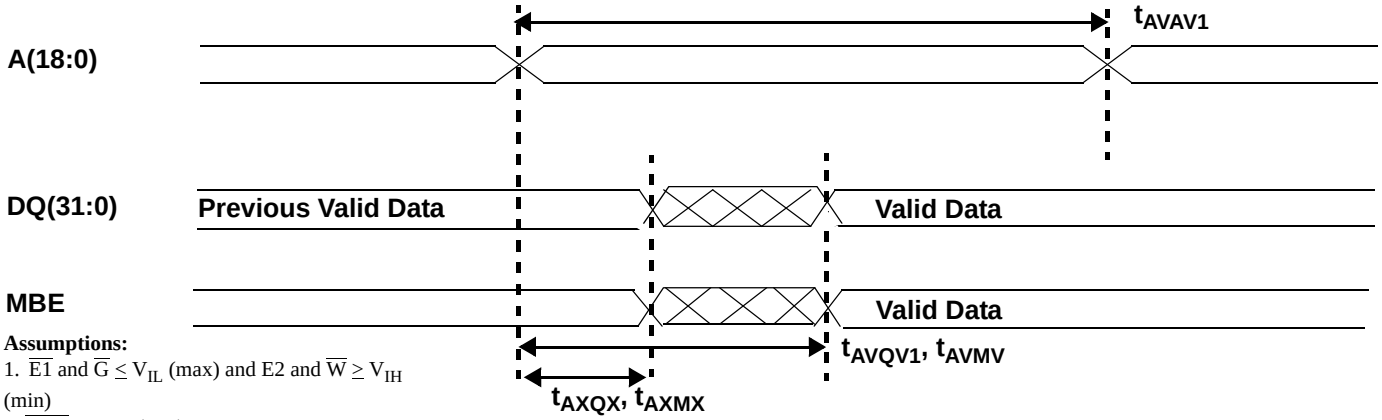
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 3.0E5 rad(Si).
1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. V_{IH} = V_{DD2} (max), V_{IL} = 0V.

AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)*

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, $V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min))

SYMBOL	PARAMETER	UT8ER512		UNIT	FIGURE
		MIN	MAX		
t_{AVAV1}[1]	Read cycle time	20		ns	3a
t_{AVQV1}	Address to data valid from address change		20	ns	3c
t_{AXQX}[2]	Output hold time	5		ns	3a
t_{GLQX1}[1,2]	$\overline{G}$-controlled output enable time	2		ns	3c
t_{GLQV}	$\overline{G}$-controlled output data valid		8	ns	3c
t_{GHQZ1}[2]	$\overline{G}$-controlled output three-state time	2	6	ns	3c
t_{ETQX}[2,3]	E-controlled output enable time	5		ns	3b
t_{ETQV}[3]	E-controlled access time		20	ns	3b
t_{EFQZ}[4]	E-controlled output three-state time[2]	3	7	ns	3b
t_{ETMV}	E-controlled error flag time		20	ns	3b
t_{AVMV}	Address to error flag valid		20	ns	3a
t_{AXMX}	Address to error flag hold time from address change	3		ns	3a
t_{GLMV}	$\overline{G}$-controlled error flag valid		7	ns	3c
t_{GLMX}	$\overline{G}$-controlled error flag enable time	5		ns	3c
t_{ETMX}	E-controlled error flag enable time	5		ns	3b

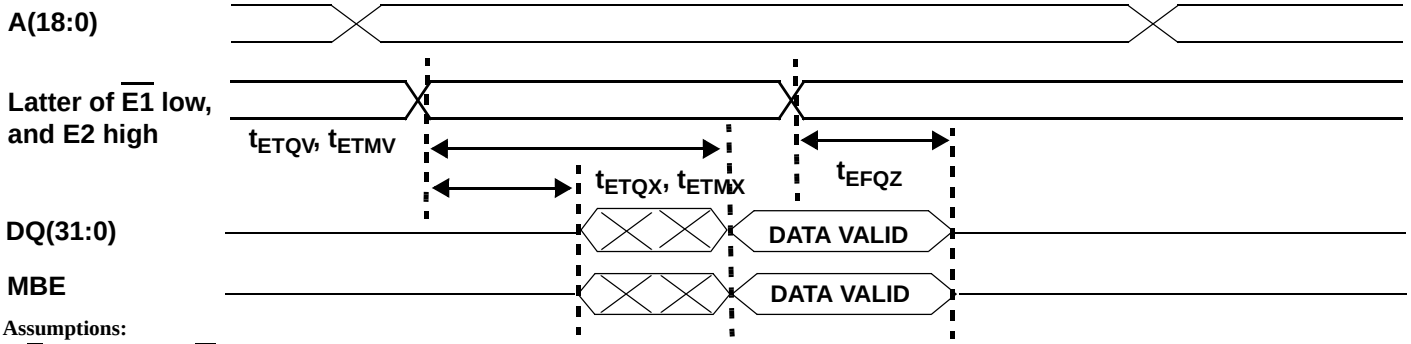
Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Guaranteed by characterization, but not tested.
2. Three-state is defined as a 200mV change from steady-state output voltage.
3. The ET (enable true) notation refers to the latter falling edge of $\overline{E1}$ or rising edge of E2.
4. The EF (enable false) notation refers to the latter rising edge of $\overline{E1}$ or falling edge of E2.



Assumptions:

1. $\overline{E1}$ and $\overline{G} \leq V_{IL}$ (max) and E2 and $\overline{W} \geq V_{IH}$ (min)
2. $\overline{Busy} \geq V_{OH}$ (min)
3. Reading uninitialized addresses will cause MBE to be asserted.

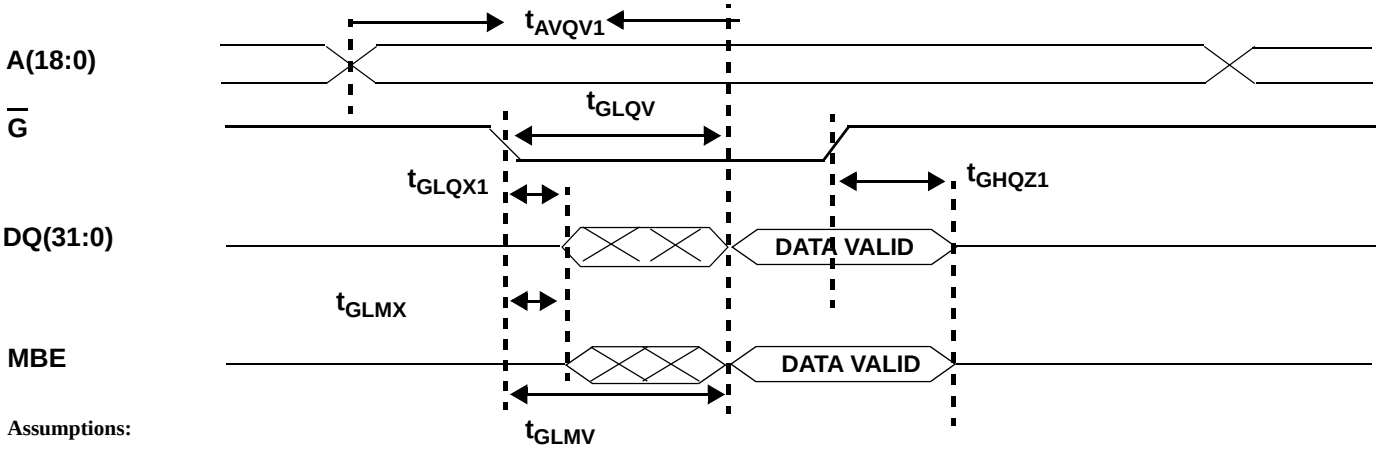
Figure 3a. SRAM Read Cycle 1: Address Access



Assumptions:

1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)
2. $\overline{Busy} \geq V_{OH}$ (min)
3. Reading uninitialized addresses will cause MBE to be asserted.

Figure 3b. SRAM Read Cycle 2: Chip Enable Access



Assumptions:

1. $\overline{E1} \leq V_{IL}$ (max), E2 and $\overline{W} \geq V_{IH}$ (min)
2. $\overline{Busy} \geq V_{OH}$ (min)
3. Reading uninitialized addresses will cause MBE to be asserted.

Figure 3c. SRAM Read Cycle 3: Output Enable Access

AC CHARACTERISTICS WRITE CYCLE (Pre and Post-Radiation)*

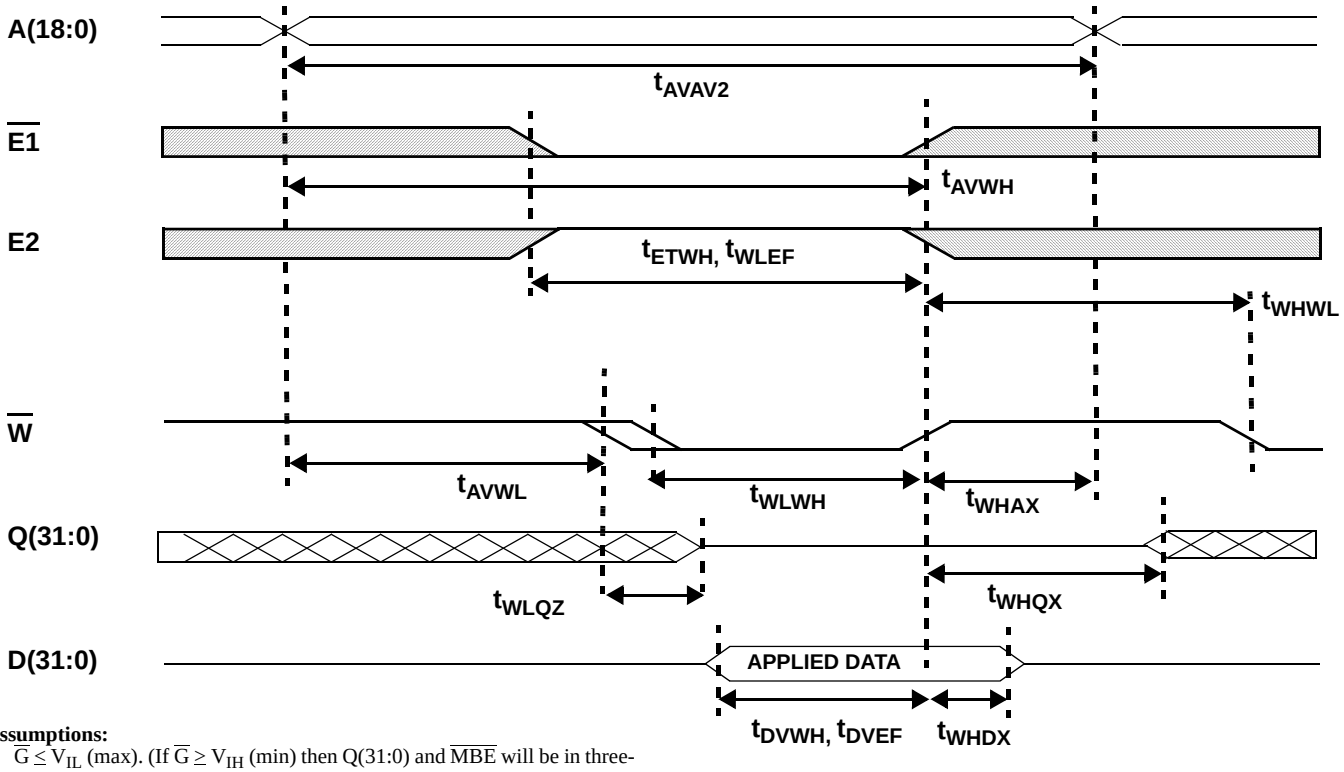
(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, $V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min))

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{AVAV2}[1]	Write cycle time	10		ns	4a/4b
t_{ETWH}	Device enable to end of write	17		ns	4a
t_{AVET}	Address setup time for write ($\overline{E1}$/E2- controlled)	0		ns	4b
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	0		ns	4a
t_{WLWH}	Write pulse width	7		ns	4a
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	0		ns	4a
t_{EFAX}	Address hold time for device enable ($\overline{E1}$/E2- controlled)	0		ns	4b
t_{WLQZ}[2]	$\overline{W}$ - controlled three-state time		7	ns	4a/4b
t_{WHQX}[2]	$\overline{W}$ - controlled output enable time	6		ns	4a
t_{ETEF}	Device enable pulse width ($\overline{E1}$/E2 - controlled)	17		ns	4b
t_{DVWH}	Data setup time	5		ns	4a
t_{WHDX}	Data hold time	0		ns	4a
t_{WLEF}	Device enable controlled write pulse width	17		ns	4b
t_{DVEF}	Data setup time	5		ns	4a/4b
t_{EFDX}	Data hold time	0		ns	4b
t_{AVWH}	Address valid to end of write	10		ns	4a
t_{WHWL}[1]	Write disable time	1		ns	4a
t_{ETQZ}	Enable Q to output Tri-State		7	ns	4b

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

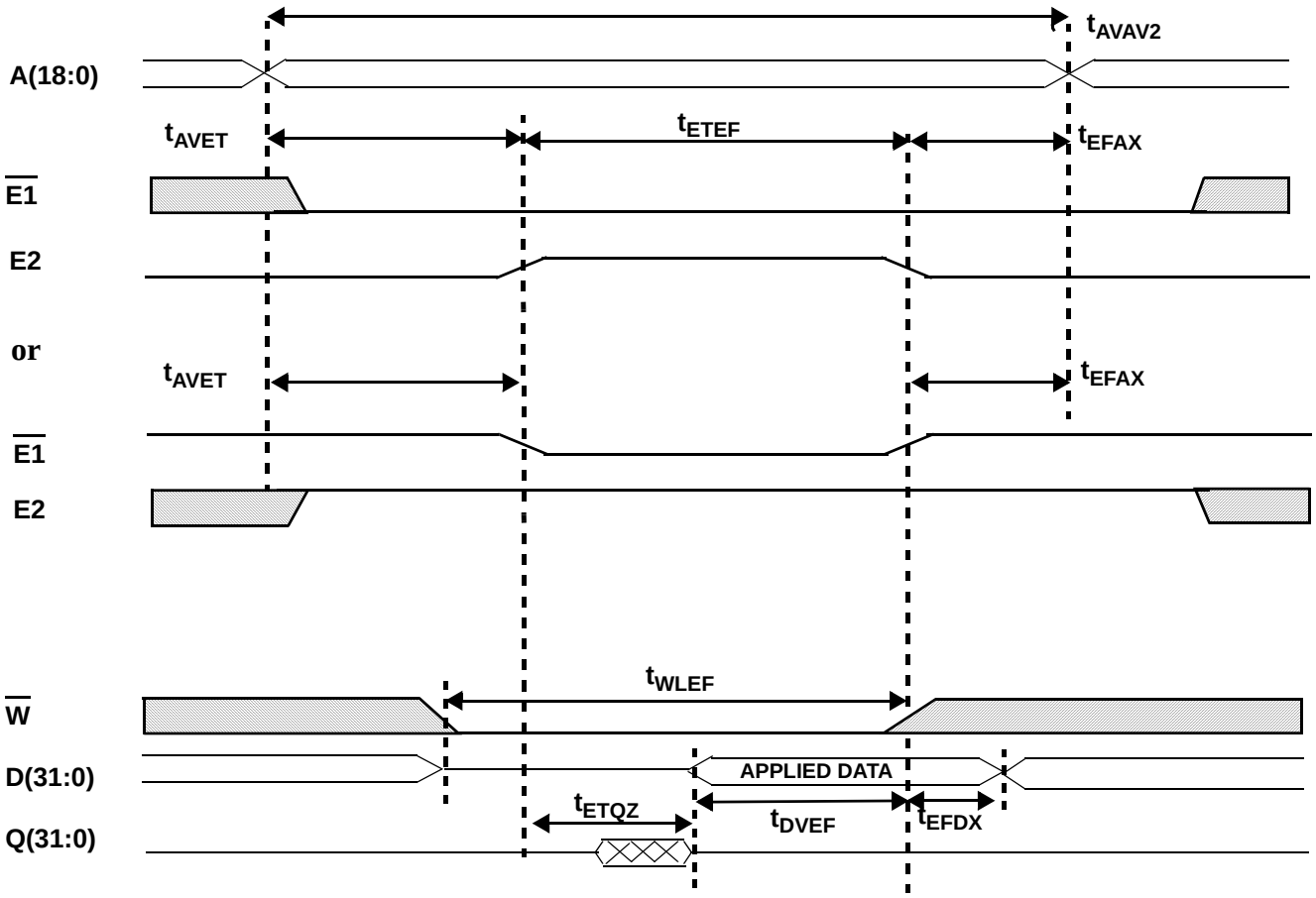
1. Tested with $\overline{G}$ high.
2. Three-state is defined as 200mV change from steady-state output voltage.



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) and $\overline{MBE}$ will be in three-state for the entire cycle.)

2. $\overline{Busy} \geq V_{OH}$ (min)

Figure 4a. SRAM Write Cycle 1: $\overline{W}$ - Controlled Access

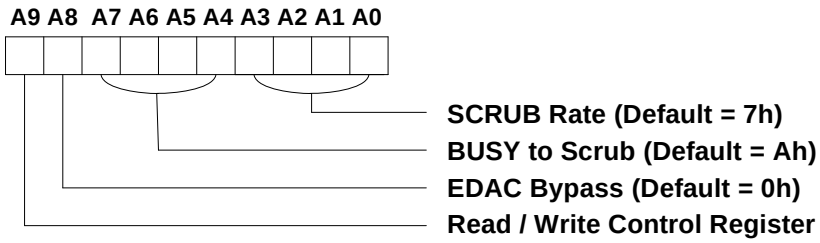


Assumptions & Notes:
1. $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) and $\overline{MBE}$ will be in three-state for the entire cycle.)

2. Either $\overline{E1}$ / E2 scenario can occur.

3. $\overline{Busy} \geq V_{OH}$ (min)

Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access



Note:
1. See Table 4 for Control Register Definitions

Table 4: EDAC Programming Configuration Table

ADDR BIT	PARAMETER	VALUE	FUNCTION
A (0 - 3)	Scrub Rate [1]	0-15	As Scrub Rate changes from 0 - 15, then the interval between Scrub cycles will change as follows: 0 = 20 MHz 6 = 312 kHz 11 = 9.76 kHz 1 = 10 MHz 7 = 156 kHz 12 = 4.88 kHz 2 = 5 MHz 8 = 78 kHz 13 = 2.44 kHz 3 = 2.5 MHz 9 = 39 kHz 14 = 1.22 kHz [4] 4 = 1.25 MHz 10 = 19.5 kHz 15 = .61 kHz [4] 5 = 625 kHz
A (4 - 7)	$\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$[2]	0-15	If $\overline{\text{BUSY}}$ changes from 0 - 15, then the interval t_{BLSL} between $\overline{\text{SCRUB}}$ and BUSY will change as follows: 0 = 0 ns 6 = 300 ns 11 = 550 ns 1 = 50 ns 7 = 350 ns 12 = 600 ns 2 = 100 ns 8 = 400 ns 13 = 650 ns 3 = 150 ns 9 = 450 ns 14 = 700 ns 4 = 200 ns 10 = 500 ns 15 = 750 ns 5 = 250 ns
A (8)	Bypass EDAC Bit [3]	0, 1	If 0, then normal EDAC operation will occur. If 1, then EDAC will be bypassed.
A (9)	Read / Write Control Register	0, 1	0 = A0 to A8 will be written to the control register 1 = Control register will be asserted to the data bus

Notes:
1. Default Scrub Rate is 156KHz.
2. The default for t_{BLSL} is 500 ns.
3.The default state for A8 is 0.
4. Below testing capability.

AC CHARACTERISTICS for EDAC FUNCTION (Pre and Post-Radiation)*

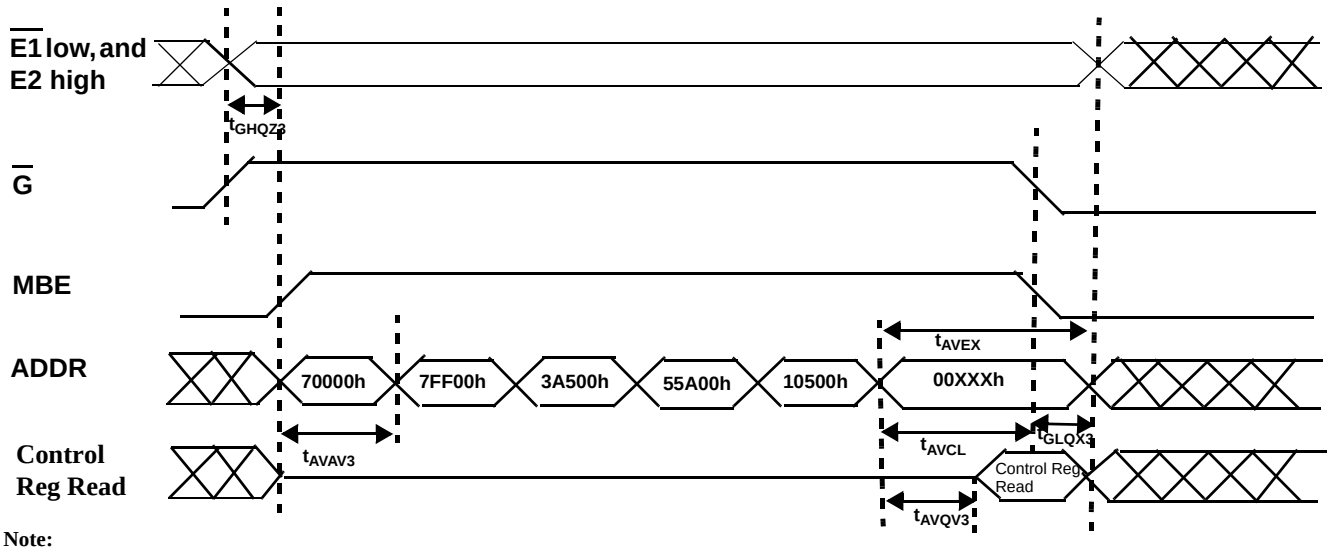
(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, $V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min))

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{AVAV3}	Address valid to address valid for control register cycle	100		ns	5a
t_{AVCL}	Address valid to control low	200		ns	5a
t_{AVEX}	Address valid to enable valid	200		ns	5a
t_{BLSL}	User Programmable - $\overline{BUSY}$ low to $\overline{SCRUB}$	See Table 4			5b
t_{SLSH1}	$\overline{SCRUB}$ low to $\overline{SCRUB}$ high	200	300	ns	5b
t_{SLSH2}	$\overline{SCRUB}$ low to $\overline{SCRUB}$ high	200		ns	5c
t_{SHBH}	$\overline{SCRUB}$ high to $\overline{BUSY}$ high	50	75	ns	5b
t_{AVQV3}	Address to data valid control register read		200	ns	5a
t_{GLQX3}	Output control output time	3		ns	5a
t_{GHQZ3}	Output tri-state time		7	ns	5a

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

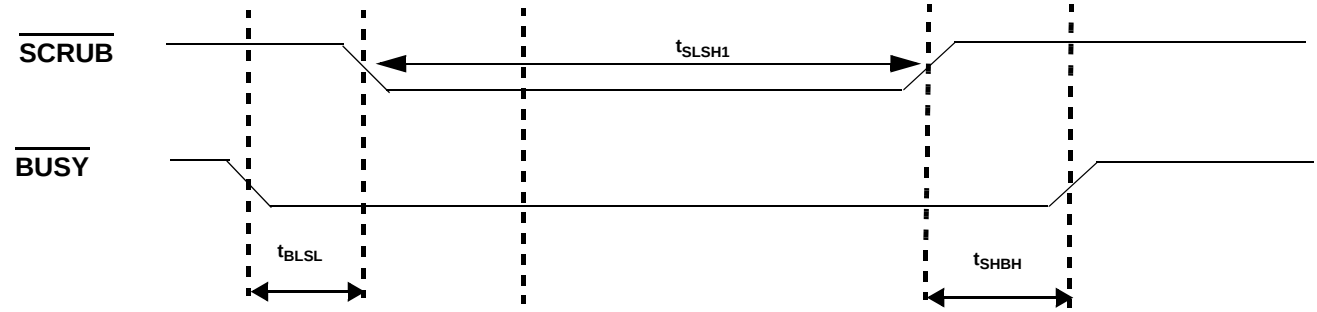
1. See Table 4 for User Programmable information.



Note:
1. MBE is driven high by the user.
2. Lower 9 bits of the last address are used to configure the control register.

Assumptions:
1. $\overline{SCRUB} \geq V_{OH}$ before the start of the configuration cycle. Ignore $\overline{SCRUB}$ during configuration cycle.

Figure 5a. Control Register Cycle

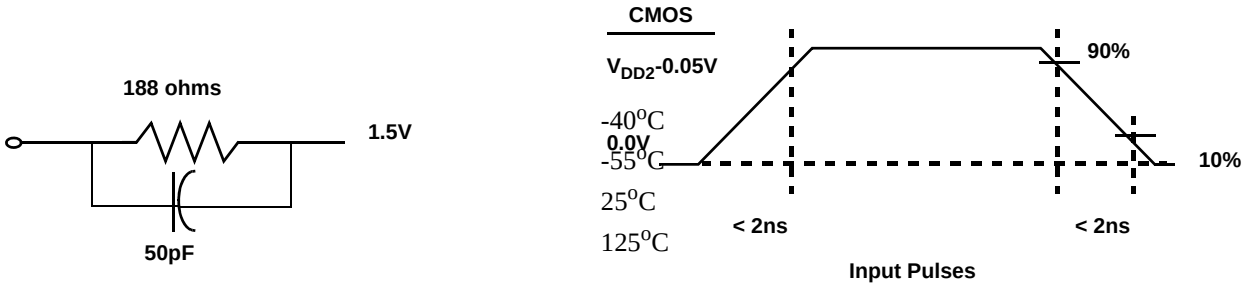


Assumptions:
1. The conditions pertain to both a Read or Write.

Figure 5b. Master Mode Scrub Cycle

Assumptions:
1. The conditions pertain to both a Read or Write.

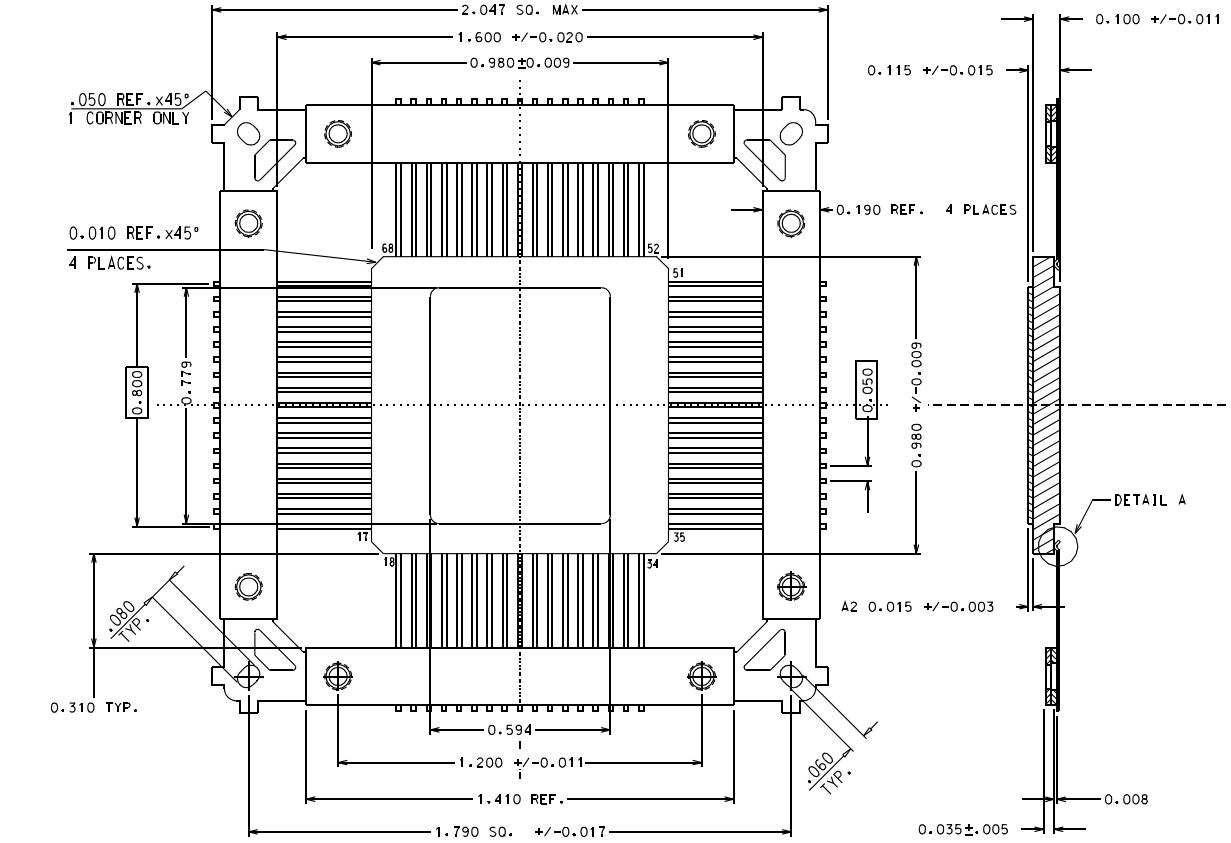
Figure 5c. Slave Mode Scrub Cycle

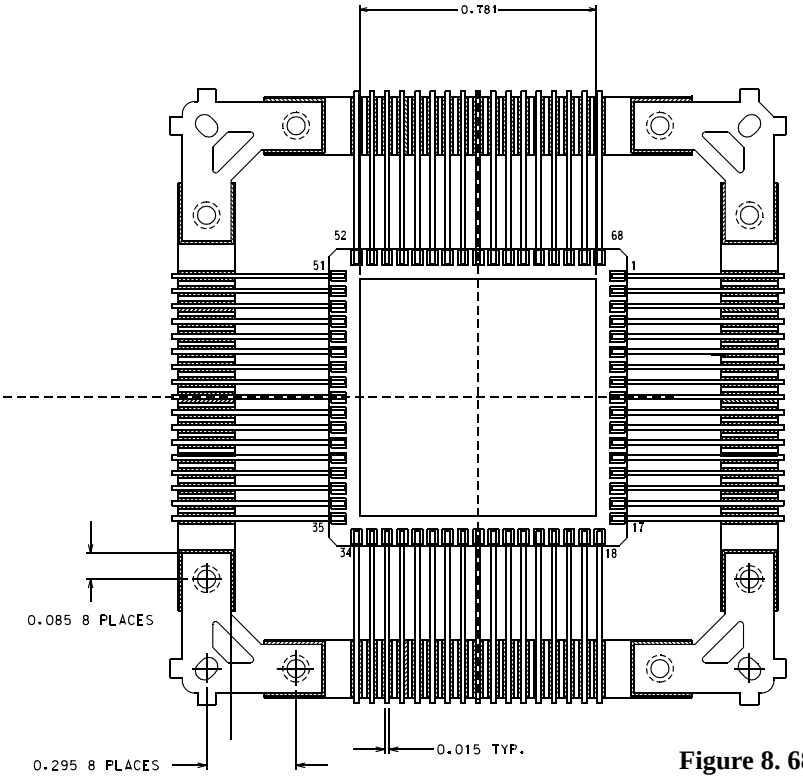


Notes:
1. 50pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = V_{DD2}/2).

Figure 7. AC Test Loads and Input Waveforms

PACKAGING





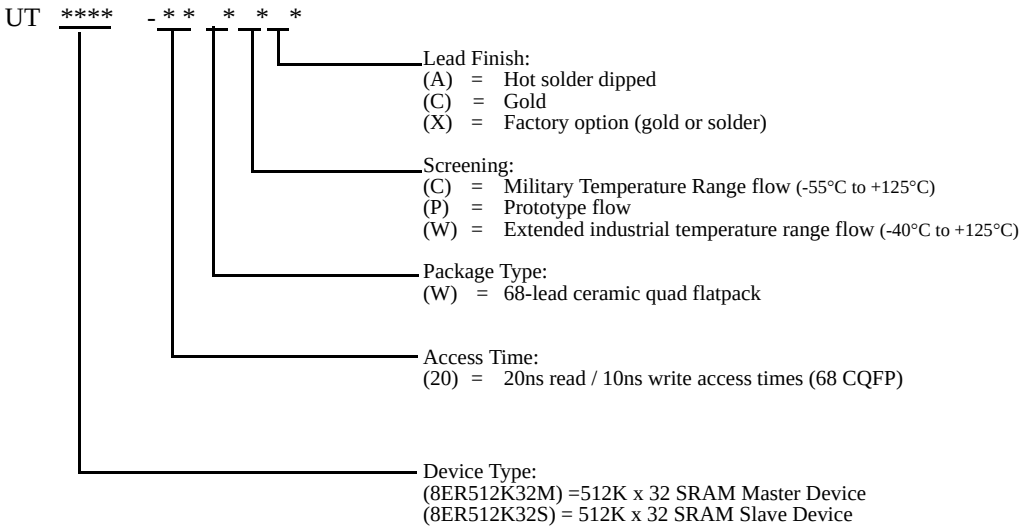
Notes:

1. All exposed metallized areas are gold plated over nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.

Figure 8. 68-Lead Ceramic Quad Flatpack

ORDERING INFORMATION

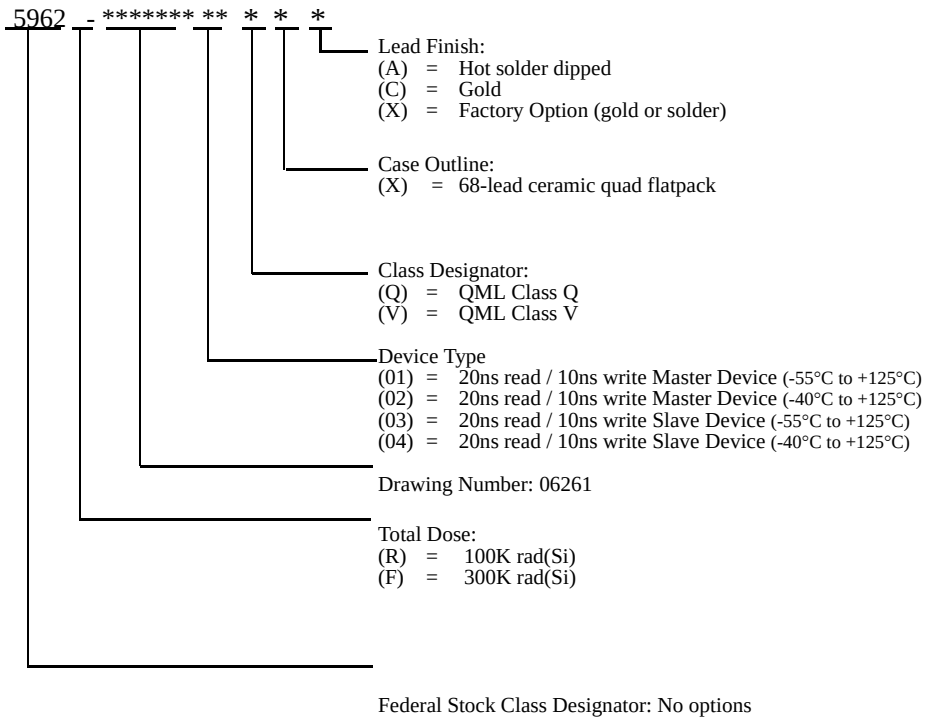
512K x 32 SRAM



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

512K x 32 SRAM: SMD



Notes:

1.Lead finish (A,C, or X) must be specified.

2.If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

3.Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

NOTES

Aeroflex Colordo Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

COLORADO
Toll Free: 800-645-8862
Fax: 719-594-8468

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

SE AND MID-ATLANTIC
Tel: 321-951-4164
Fax: 321-951-4254

WEST COAST
Tel: 949-362-2260
Fax: 949-362-2266

CENTRAL
Tel: 719-594-8017
Fax: 719-594-8468

www.aeroflex.com info-ams@aeroflex.com

AEROFLEX
A passion for performance.

Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused