# MD32256FKX

## 256K x 32 CMOS DRAM Module

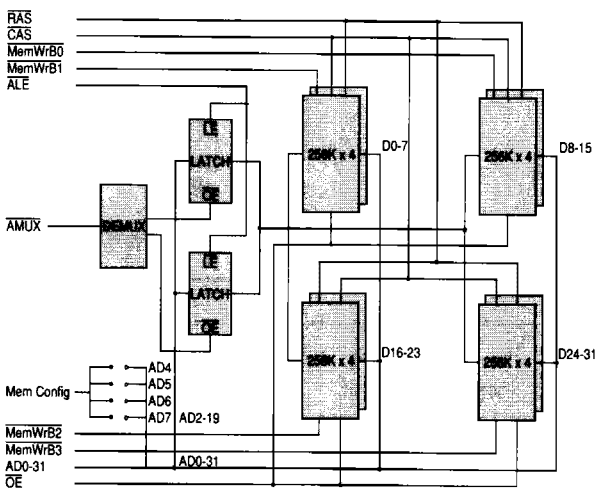
262,144 x 32 CMOS High Speed Dynamic RAM

## ADVANCE PRODUCT NFORMATION

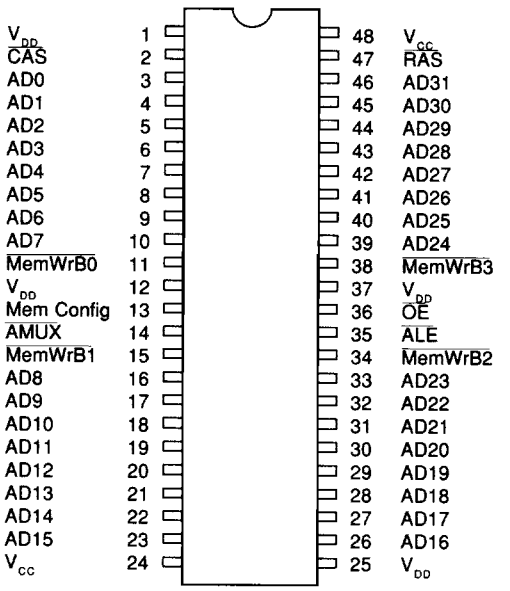
### Features

- Row Access Times of 100/120/150 ns
- Onboard Address Latching
- Onboard Address Multiplexing
- Byte Write Facility
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- $\overline{RAS}$ Only Refresh
- Directly TTL Compatible
- MemConfig Option for Transputer Applications
- 512 Cycle Refresh in 8 ms (max)

### Block Diagram




### Pin Definition

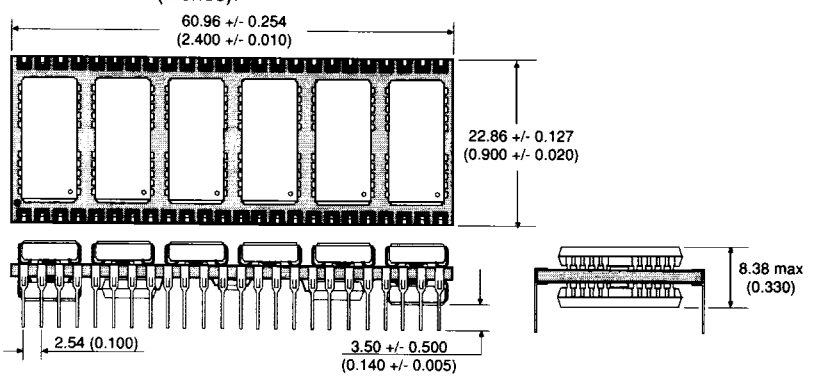



### Pin Functions

| | |
|---|---|
| AD0-AD31 | Address/Data I/O |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{MemWrB0-3}$ | Byte Write |
| $\overline{OE}$ | Output Enable |
| $\overline{AMUX}$ | Address Multiplex |
| $\overline{ALE}$ | Address Latch Enable |
| Mem Config | Configure Memory |
| $V_{CC}$ | Power (+5V) |
| $V_{DD}$ | Ground |

5

### Package Details Dimensions in mm (inches).



## Absolute Maximum Ratings

| | | |
|---|---|---|
| Voltage Range on any pin | -1 to $V_{CC}^{+0.3}$ | V |
| Voltage Range on $V_{CC}$ | 0 to 7 | V |
| Short Circuit Output Current | 50 | mA |
| Power Dissipation | 8 | W |
| Operating Free-air Temperature Range | 0 to 70 | °C |
| Storage Temperature | -65 to +150 | °C |

## Recommended Operating Conditions

| | | min | typ | max | |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.4 | - | 6.5 | V |
| Input Low Voltage | $V_{IL}$ | -2.0 | - | 0.8 | V |
| Output High Voltage | $V_{OH}$ | 2.4 | - | $V_{CC}$ | V |
| Output Low Voltage | $V_{OL}$ | 0 | - | 0.4 | V |
| Operating Temperature | $T_a$ | 0 | - | 70 | °C |
| | $T_{al}$ | -40 | - | 85 | °C (32256FKXI) |

## Capacitance ($V_{cc}$=5V±10%,$T_a$=25°C)

| *Parameter* | *Symbol* | *Test Condition* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|
| I/P Capacitance | | | | | |
| $\overline{CAS}$, $\overline{RAS}$, $\overline{OE}$ | $C_{IN1}$ | $V_{IN1}$ = 0V | - | 56 | pF |
| $\overline{MemWrB0-3}$ | $C_{IN2}$ | $V_{IN2}$ = 0V | - | 14 | pF |
| $\overline{ALE}$ | $C_{IN3}$ | $V_{IN3}$ = 0V | - | 10 | pF |
| $\overline{AMUX}$ | $C_{IN4}$ | $V_{IN4}$ = 0V | - | 15 | pF |
| I/O Capacitance, AD0 - AD31 | $C_{I/O}$ | $V_{I/O}$ = 0V | - | 17 | pF |

## DC Electrical Characteristics

| *Parameter* | *Symbol* | *Test Condition* | *-10* | | *-12 & -15* | | *Unit* |
|---|---|---|---|---|---|---|---|
| | | | *min* | *max* | *min* | *max* | |
| Input Leakage Current | | | | | | | |
| $\overline{CAS}$, $\overline{RAS}$, $\overline{MemWrB0-3}$, $\overline{OE}$ | $I_{Li1}$ | | - | +/-80 | - | +/-80 | µA |
| AD2 - AD19 | $I_{Li2}$ | | -600 | 20 | -600 | 20 | µA |
| $\overline{ALE}$ | $I_{Li3}$ | | -1200 | 40 | -1200 | 40 | µA |
| $\overline{AMUX}$ | $I_{Li4}$ | | -1800 | 60 | -1800 | 60 | µA |
| I/O Leakage Current | $I_{Lio}$ | | - | +/-80 | - | +/-80 | µA |
| Read/Write Cycle Current | $I_{cc1}$ | | - | 685 | - | 645 | mA |
| Standby Current | $I_{cc2}$ | $V_{IH}$=5.5V | - | 110 | - | 110 | mA |
| Average Refresh Current | $I_{cc3}$ | | - | 645 | - | 605 | mA |

## AC Test Conditions

* Input pulse levels: Gnd to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* Vcc=5V±10%

## Description

The MD32256FKX is a high speed 8,388,608 bit Dynamic Random Access Memory organised as 262,144 words of 32 bits each. Although designed primarily for use with Transputers, it can be used with any system which supports Dynamic Memory and a 32 bit Multiplexed Address / Data Bus. Information on interfacing this part with both Transputers and other systems is given below.

## Transputer Operation

Four different Memory Configuration options are provided via the MemConfig pin. This pin is connected, at the manufacturing stage, to one of the Address / Data pins AD4, AD5, AD6, AD7, the particular option specified by the customer when ordering. This allows for a wide range of memory speed and Transputer speed configurations to be used, depending on the application, as shown in the table below.

| Memory Speed (nS) | Transputer Speed (MHz) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 15 | | | | 17 | | | | 20 | | | |
| | AD LINK | | | | AD LINK | | | | AD LINK | | | |
| | 4 | 5 | 6 | 7 | 4 | 5 | 6 | 7 | 4 | 5 | 6 | 7 |
| 100 | ● | ● | ● | ● | | ● | ● | ● | | | ● | ● |
| 120 | | ● | ● | ● | | | ● | ● | | | ● | ● |
| 150 | | | ● | ● | | | ● | ● | | | | ● |

● Indicates allowable combination

Connections to the Transputer are as follows :

| Transputer Pin | MD32256 Pin |
|---|---|
| MemnotWrD0 | AD0 |
| MemnotRfD1 | AD1 |
| MemAD2-MemAD31 | AD2-AD31 |
| notMemS0 | ALE |
| notMemS1 | RAS |
| notMemS2 | AMUX |
| notMemS3 | CAS |
| MemConfig | MemConfig |
| notMemRd | OE |
| notMemWrB0-3 | MemWrB0-3 |

## General Operation

The MD32256 is a 256K x 32 bit Dynamic Memory with a multiplexed Address / Data bus. This device has on board address latches and address multiplexing, which reduces the complexity of external circuitry. This data sheet descibes the use of this memory in normal READ and WRITE modes and EARLY WRITE mode, as well as two types of REFRESH.

### Address AD2 - AD19

18 Address bits are required to decode 1 of 256K locations. This 18 bit address is converted by the on board circuitry to two 9 bit addresses for use by the 256K x 4 DRAMS used, and strobed into the DRAMS by using the RAS and CAS control inputs.

### MemWrB0 - MemWrB3

The READ or WRITE mode is selected by these inputs, a separate input provided for each byte, the least significant byte controlled by MemWrB0. A logic high on these inputs selects the READ mode and a logic low selects the WRITE mode. The data input is disabled when the READ mode selected. When MemWrB0 - 3 go low prior to CAS (early write), data out will remain in the high impedance state for the entire cycle, permitting a WRITE operation with OE grounded.

### Data IN AD0 - AD31

Data is written during a WRITE or EARLY WRITE cycle. In an EARLY WRITE cycle, MemWrB0-3 are brought low before CAS and the data is strobed by CAS. In a WRITE cycle, CAS is already low so the data is strobed in by MemWrB0-3; note that OE must be high to put the output buffers into a high impedance state before placing data onto AD0 - AD31.

See diagrams showing WRITE and EARLY WRITE waveforms for detailed timing.

### Data OUT AD0 - AD31

The three state output buffer is in the high impedance state until both CAS and RAS are brought low. In a READ cycle the output becomes valid after the access time interval $t_{CAC}$, and remains valid while CAS and OE are low. Either CAS or OE going high returns it to the high impedance state.

See diagram showing READ waveform for detailed timing.

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## Output Enable $\overline{OE}$

When $\overline{OE}$ is high the output buffers are in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will place the output buffers in the low impedance state, as long as $\overline{RAS}$ and $\overline{CAS}$ are low as well. If either $\overline{OE}$ or $\overline{CAS}$ are brought high the buffers will return to the high impedance state.

## Address Latch Enable $\overline{ALE}$

On the high to low transition of $\overline{ALE}$ the address on the lines AD2 - AD19 is latched, and remains latched until $\overline{ALE}$ goes high. With $\overline{ALE}$ low these latches operate transparently i.e. the data on the outputs follows the inputs.

## Address Latch Multiplex $\overline{AMUX}$

When $\overline{AMUX}$ is high the address on AD2 - AD10 (row address) is presented to the DRAMS and is latched onto them when $\overline{RAS}$ goes low. When $\overline{AMUX}$ is low the address on AD11 - AD19 is used, and latched onto the DRAMS when $\overline{CAS}$ goes low.

## Refresh $\overline{RAS}$ Only

A refresh operation must be performed once every 8 ms to retain stored data, achieved by strobing one of the 512 rows. A normal READ or WRITE cycle will refresh all of the bits in each row that is selected. For $\overline{RAS}$ only refresh, $\overline{CAS}$ is held high and an externally generated row address must be supplied on AD2 - AD10.

See diagram showing $\overline{RAS}$ only refresh for detailed timing.

## Refresh $\overline{CAS}$ Before $\overline{RAS}$

The refresh address can be generated automatically by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ and holding it low while cycling $\overline{RAS}$. In this mode the external address is ignored.

## Power Up

To achieve correct device operation, after $V_{CC}$ has reached its full level a delay of 200us is required followed by eight initialisation cycles (READ, WRITE or REFRESH).

## Electrical Characteristics & Recommended AC Operating Conditions

| Parameter | Symbol | -10 min | -10 max | -12 min | -12 max | -15 min | -15 max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 190 | - | 220 | - | 260 | - | ns | 2 |
| Transition Time | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | |
| Non-static Column Decode Mode | | | | | | | | | |
| Pulse Duration, $\overline{RAS}$ Low | $t_{RAS}$ | 100 | 10000 | 120 | 10000 | 150 | 10000 | ns | |
| Delay Time, $\overline{RAS}$ Low to $\overline{CAS}$ Low | $t_{RCD}$ | 25 | 50 | 25 | 60 | 30 | 75 | ns | 8 & 10 |
| Delay Time, $\overline{CAS}$ Low to $\overline{RAS}$ High | $t_{RSH}$ | 50 | - | 60 | - | 75 | - | ns | 8 |
| Pulse Duration, $\overline{RAS}$ High (Precharge) | $t_{RP}$ | 80 | - | 90 | - | 100 | - | ns | |
| Delay Time, $\overline{RAS}$ Low to $\overline{CAS}$ High | $t_{CSH}$ | 100 | - | 120 | - | 150 | - | ns | |
| Delay Time, $\overline{CAS}$ High to $\overline{RAS}$ Low | $t_{CRP}$ | 10 | - | 10 | - | 10 | - | ns | |
| Pulse Duration, $\overline{CAS}$ Low | $t_{CAS}$ | 50 | 10000 | 60 | 10000 | 75 | 10000 | ns | |
| Column Address Setup Time Before $\overline{CAS}$ Low | $t_{ASC}$ | 0 | - | 0 | - | 0 | - | ns | |
| Pulse Duration, $\overline{CAS}$ High | $t_{CP}$ | 10 | - | 15 | - | 20 | - | ns | |
| Row Address Hold Time After $\overline{RAS}$ Low | $t_{RAH}$ | 15 | - | 15 | - | 20 | - | ns | |
| Delay Time, Column Address to $\overline{CAS}$ High | $t_{CAL}$ | 70 | - | 80 | - | 95 | - | ns | |
| Row Address Setup Time Before $\overline{RAS}$ Low | $t_{ASR}$ | 10 | - | 10 | - | 10 | - | ns | |
| Delay Time, Column Address to $\overline{RAS}$ High | $t_{RAL}$ | 70 | - | 80 | - | 95 | - | ns | |
| Column Address Hold Time After $\overline{RAS}$ Low | $t_{AR}$ | 75 | - | 85 | - | 110 | - | ns | 7 |
| Read Hold Time After $\overline{RAS}$ High | $t_{RRH}$ | 10 | - | 10 | - | 10 | - | ns | |
| Read Setup Time Before $\overline{CAS}$ Low | $t_{RCS}$ | 0 | - | 0 | - | 0 | - | ns | |
| Column Address Hold Time After $\overline{CAS}$ Low | $t_{CAH}$ | 20 | - | 20 | - | 25 | - | ns | |
| Read Hold Time After $\overline{CAS}$ High | $t_{RCH}$ | 0 | - | 0 | - | 0 | - | ns | |
| Access Time From $\overline{CAS}$ Low | $t_{CAC}$ | - | 50 | - | 60 | - | 75 | ns | |
| Access Time From Column Address | $t_{CAA}$ | - | 70 | - | 80 | - | 95 | ns | |
| Output Disable Time After $\overline{CAS}$ High | $t_{OFF}$ | 0 | 25 | 0 | 30 | 0 | 35 | ns | 1 |
| Access Time From $\overline{RAS}$ Low | $t_{RAC}$ | - | 100 | - | 120 | - | 150 | ns | |
| Access Time From $\overline{OE}$ Low | $t_{GAC}$ | - | 25 | - | 30 | - | 40 | ns | |
| Output Disable Time After $\overline{OE}$ High | $t_{GOFF}$ | 0 | 25 | 0 | 30 | 0 | 40 | ns | 1 |
| Write Cycle Time | $t_{WC}$ | 190 | - | 220 | - | 260 | - | ns | |
| Write Pulse Duration | $t_{WP}$ | 15 | - | 20 | - | 25 | - | ns | |
| Write Hold Time After $\overline{RAS}$ Low | $t_{WCR}$ | 70 | - | 85 | - | 110 | - | ns | 6 & 7 |
| MemWr Low Setup Time Before $\overline{CAS}$ High | $t_{CWL}$ | 35 | - | 40 | - | 45 | - | ns | |
| MemWr Low Setup Time Before $\overline{CAS}$ Low | $t_{WCS}$ | 0 | - | 0 | - | 0 | - | ns | 6 |
| Write Hold Time After $\overline{CAS}$ Low | $t_{WCH}$ | 20 | - | 25 | - | 30 | - | ns | |
| MemWr Low Setup Time Before $\overline{RAS}$ High | $t_{RWL}$ | 35 | - | 40 | - | 45 | - | ns | |
| Data Setup Time Before $\overline{CAS}$ Low | $t_{DSC}$ | 0 | - | 0 | - | 0 | - | ns | 5 |
| Data Hold Time After $\overline{CAS}$ Low | $t_{DHC}$ | 25 | - | 30 | - | 40 | - | ns | 5 |
| Data Hold Time After $\overline{RAS}$ Low | $t_{DHR}$ | 75 | - | 90 | - | 120 | - | ns | 7 |
| Data Setup Time Before $\overline{MemWr}$ Low | $t_{DSW}$ | 0 | - | 0 | - | 0 | - | ns | 5 |
| Data Hold Time After $\overline{MemWr}$ Low | $t_{DHW}$ | 25 | - | 30 | - | 40 | - | ns | 5 |
| Delay Time, $\overline{OE}$ High Before Data valid | $t_{GDD}$ | 30 | - | 35 | - | 45 | - | ns | |
| Delay Time $\overline{RAS}$ high to $\overline{CAS}$ low | $t_{RPC}$ | 5 | - | 5 | - | 5 | - | ns | 3 |
| Delay Time $\overline{CAS}$ low to $\overline{RAS}$ low | $t_{CSR}$ | 10 | - | 10 | - | 15 | - | ns | 3 |
| Delay Time $\overline{RAS}$ low to $\overline{CAS}$ high | $t_{CHR}$ | 20 | - | 25 | - | 30 | - | ns | 3 |
| Delay Time Address valid to $\overline{ALE}$ low | $t_{LAL}$ | 10 | - | 10 | - | 10 | - | ns | |
| Delay Time $\overline{ALE}$ low to Address not valid | $t_{LHL}$ | 13 | - | 13 | - | 13 | - | ns | |
| Delay Time $\overline{ALE}$ high to Address valid | $t_{LHH}$ | 13 | - | 13 | - | 13 | - | ns | |
| $\overline{ALE}$ Pulse Duration, High | $t_{LP}$ | 4 | - | 4 | - | 4 | - | ns | |
| Address Latch Setup Time | $t_{LRS}$ | 13 | - | 13 | - | 13 | - | ns | |

Notes :
1. $t_{OFF}$ and $t_{GOFF}$ are specified when the output is no longer driven.
2. All cycle times assume $t_T$=5ns.
3. $\overline{CAS}$ before $\overline{RAS}$ refresh only.
4. Later of $\overline{CAS}$ or $\overline{MemWr}$ in write operation.
5. Early write operation only.
6. The minimum value is measured when $t_{RAD}$ is set to $t_{RAD}$ min as a reference.
7. Read cycle only.
8. Write cycle only.
9. Maximum value specified only to guarantee access time.

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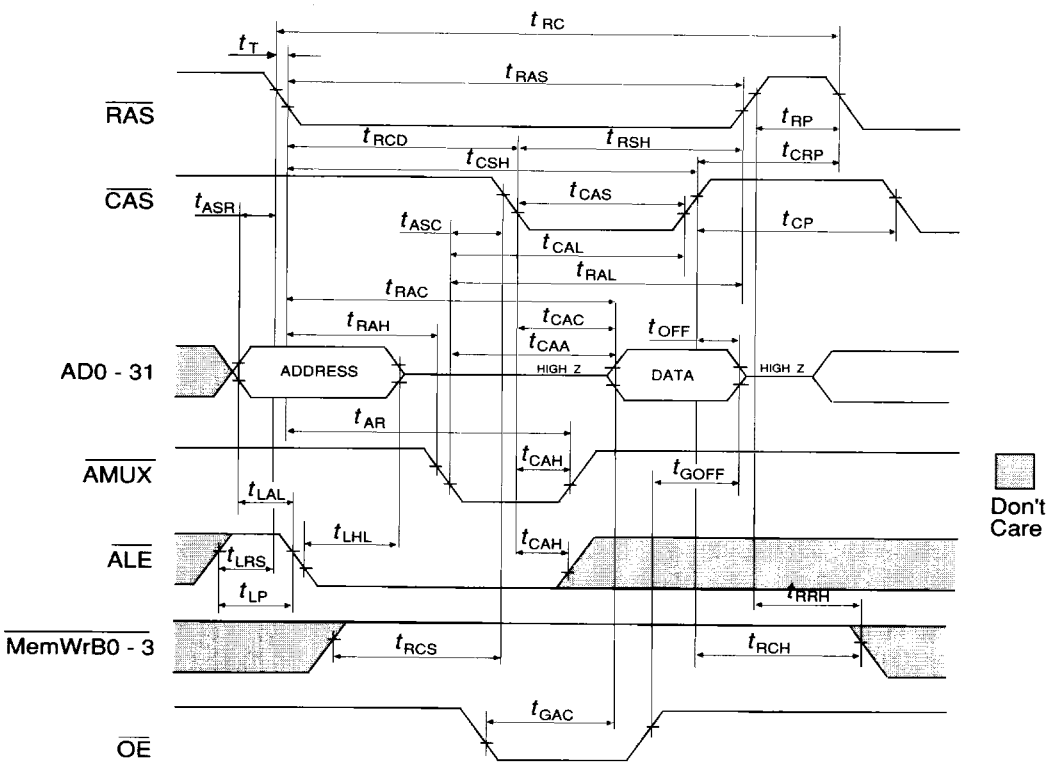
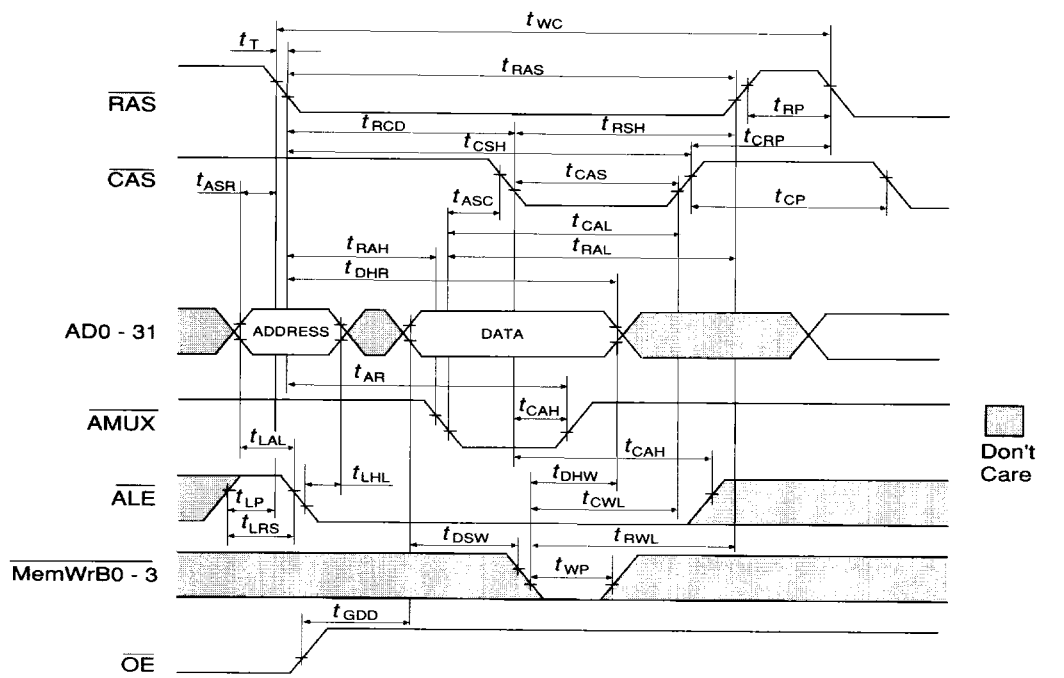
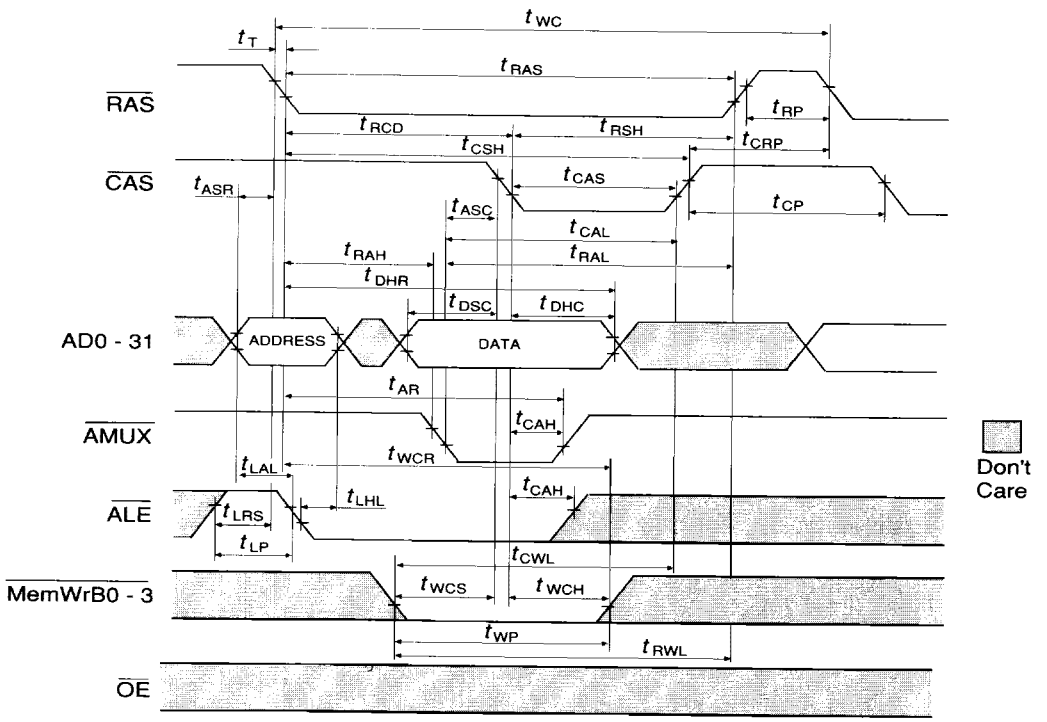
## Read Cycle Timing Waveform



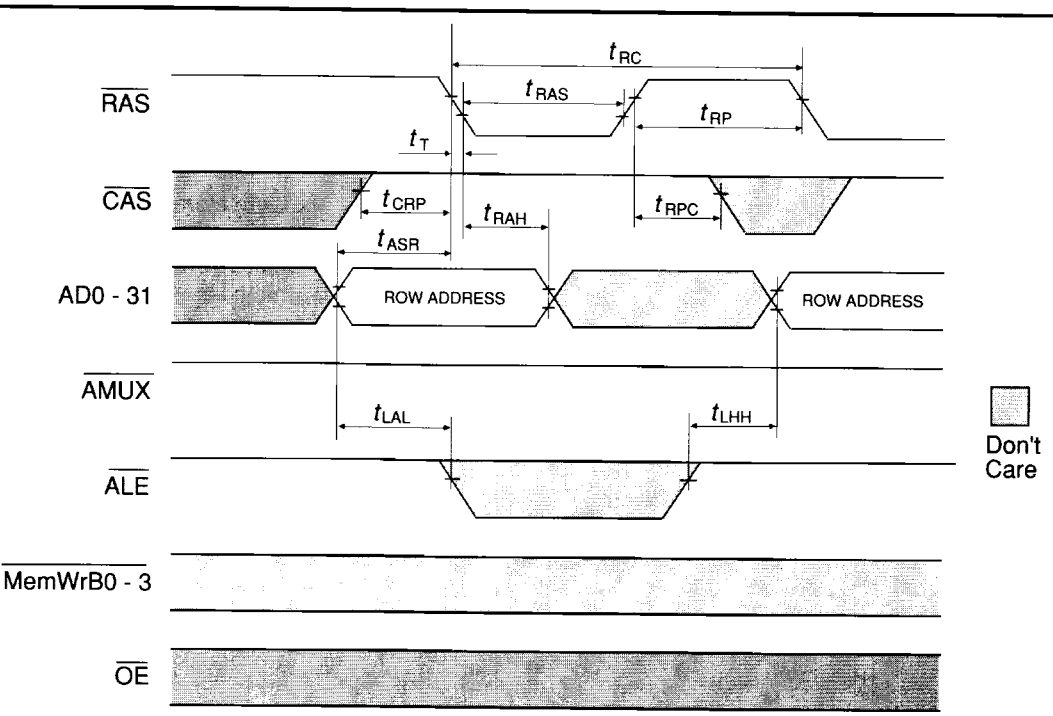

## Write Cycle Timing Waveform



## Early Write Cycle Timing Waveform




## Refresh RAS Only

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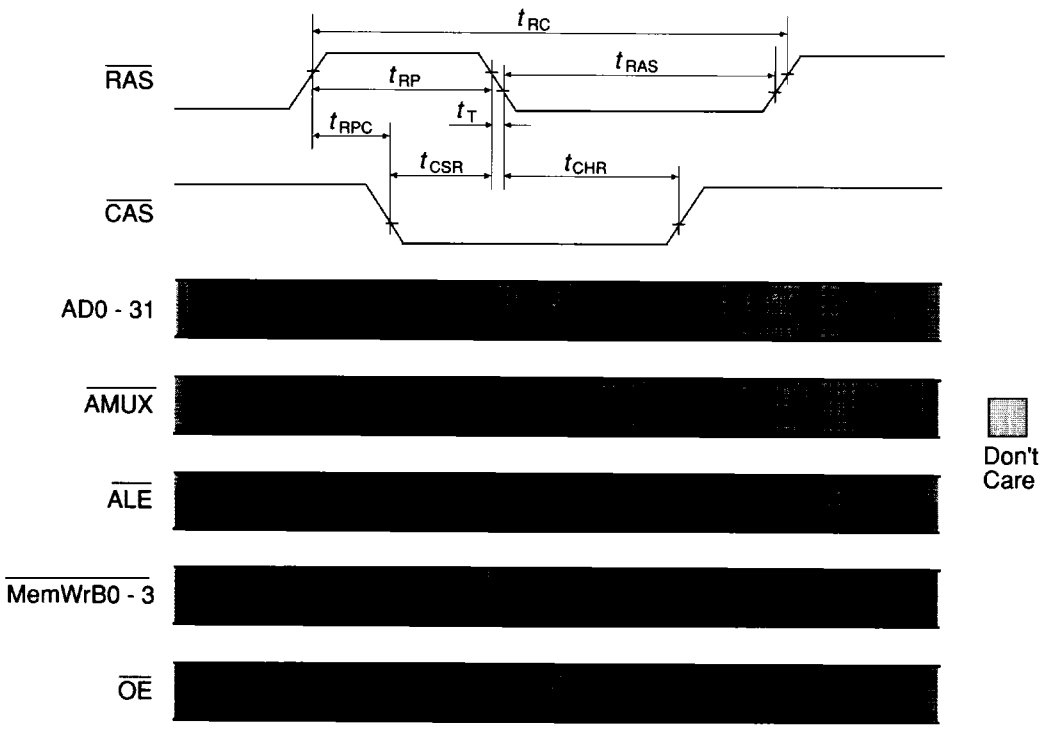
## Refresh $\overline{CAS}$ Before $\overline{RAS}$




## Ordering Information

**MD32256FKXI-10/AD4**

| | | |
|---|---|---|
| Transputer Option | AD4 | = Link to MemAD4 |
| | AD5 | = Link to MemAD5 |
| | AD6 | = Link to MemAD6 |
| | AD7 | = Link to MemAD7 |
| Speed | 100,120,150 ns | |
| Temp.range/screening | Blank | = Commercial Temp. |
| | I | = Industrial Temp. |
| Pinout | X | = ASIC |
| Package Type | FK | = 48 Pin 900 mil Plastic DIP |