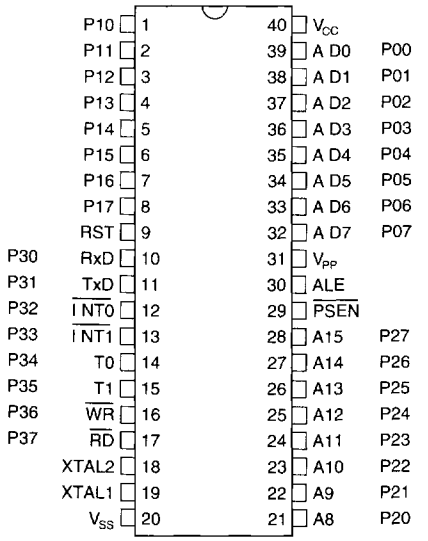


FIGURE 1 – Pin Configuration

PIN DESCRIPTION

V_{SS} (Pin 20) Circuit ground potential.

V_{CC} (Pin 40)

Supply voltage during normal, Idle and Power Down operation.

Port 0 (Pins 32–39) AD0 - AD7

Port 0 is the multiplexed low-order address and data bus during access to Program and Data Memory. It uses strong internal pullups when emitting 1's.

Port 1 (Pins 1–8)

Port 1 is an 8-bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. P10 also has a special programming function. See Erase Algorithm (page 6)

Port 2 (Pins 21–28) A8 - A15

Port 2 emits the high-order address byte during fetches from program memory and during accesses to data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to data memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 3 (Pins 10–17)

Port 3 is an 8-bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups. It also serves the functions of various special features of the MCS-51 family, as listed below.

WC8-P31F-64X

80C31 Based Microcontroller Module With 64K Flash and 8K SRAM

FEATURES

- **80C31 - Based**
  MCS-51 architecture
  Speed to 16MHz
  200nS write cycle time
- **Memory**
  64K Bytes of FLASH, program memory
  8K Bytes of SRAM, data memory
- **Open System Architecture**
  Allows additional peripherals
  Allows additional memory
- **100% CMOS design**
- **Idle and power down modes**
- **12.0 V_{PP}, 5.0 V_{CC} Supplies**
- **Low Power Consumption**
  35mA operating current, maximum
  500uA power down current, maximum
- **Temperature ranges**
  -40°C to +85°C Industrial
  -55°C to +125°C Military
- **Screening and burn in to military standards are available options**
- **Intended for use in very high density systems, where space and power are at a premium.**
- **Packaging and construction is a compact 2.1"x0.75"x0.185" 40-pin hermetically sealed metal DIP well suited to military and severe industrial applications**

WHITS015

Port Pin	Alternate Function	
P30	RxD	(serial input port)
P31	TxD	(serial output port)
P32	INT0	(external interrupt 0)
P33	INT1	(external interrupt 1)
P34	T0	(Timer 0 external input)
P35	T1	(Timer 1 external input)
P36	WR	(external Data Memory write strobe)
P37	RD	(external Data Memory read strobe)

RST (Pin 9)

A high level on this for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{CC}. This pin does not receive the power-down voltage as is the case for other MCS-51 family members. This function has been transferred to the V_{CC} pin.

ALE (Pin 30)

Address Latch Enable output for latching the low byte of the address during accesses to external memory. It is also the ALE input when programming the internal FLASH memory.

$\overline{PSEN}$ (Pin 29)

Program Store Enable output is the read strobe to external Program Memory. $\overline{PSEN}$ is activated twice each machine cycle during fetches from external Program Memory. (Two activations of $\overline{PSEN}$ are skipped during each access to external Data Memory). $\overline{PSEN}$ is also the read strobe input when programming the internal FLASH memory.

V_{PP} (Pin 31)

Erase/Program Power Supply for writing the command register, erasing, or programming the internal FLASH memory.

XTAL1 (Pin 19)

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2 (Pin 18)

Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. This pin should be floated when an external oscillator is used.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

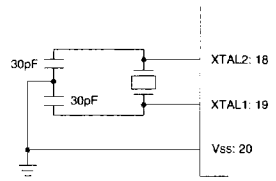


FIGURE 2 – Crystal Oscillator

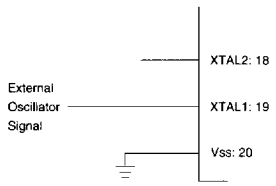


FIGURE 3 – External Drive Configuration

IDLE AND POWER DOWN OPERATION

Figure 4 shows the internal Idle and Power Down Clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to function while the clock to the CPU is gated off.

These special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

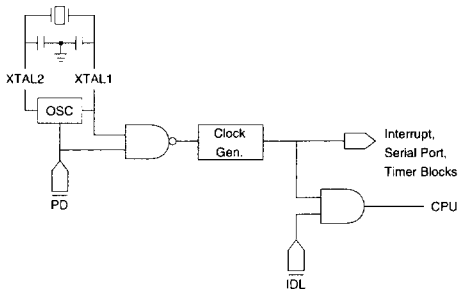


FIGURE 4 – Idle and Power Down Hardware

Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM (internal), and all other registers maintain their data during Idle.

There are two ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote a 1 to PCON.0.

PCON: Power Control Register

(MSB) (LSB)

SMOD---------- GF1 GF0 PD IDL

Symbol	Pos	Function
SMOD	PCON.7	Double baud rate bit. Is set to a 1. The baud rate is doubled when the serial port is being used in either modes 1, 2, or 3
	PCON.6	(Reserved)
	PCON.5	(Reserved)
	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1's are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XXX0000).

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

Power Down Mode

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during Power Down mode. A hardware reset is the only way of exiting the Power Down mode.

In the Power Down mode, V_{CC} may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the Power Down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

MEMORY FUNCTIONS

Internal Memory

The internal memory of the WC8-P31F-64X consists of 64K bytes of FLASH located in program memory at 0000H-FFFFH and 8K bytes of SRAM located in data memory at 8000H-9FFFH.

Flash Memory Programming

Internal Flash program memory erasure and programming are accomplished via the command register, when high voltage is applied to the V_{PP} pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command. The command register is written by bringing Write-Enable to a logic-low level (V_{IL}) while ALE is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

The three high-order register bits (R7, R6, R5) encode the control functions. All other register bits, R4 to R0, must be zero. The only exception is the reset command when FFH is written to the register. Register bits R7 - R0 correspond to data inputs D7 - D0. Refer to Table 2 and Figure 9 for timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 1 defines these register commands. NOTE: Any reference to chip enable should be referenced to the falling edge of ALE when accessing the internal memory for programming operations. Insure pin 9 RST is HIGH during all programming operations. Then follow normal bus cycle operation for access to memory.

Read Command

While V_{PP} is high, for erasure and programming, memory contents can be accessed by the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition.

Set-Up Erase / Erase Commands

Set-up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The Set-up Erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Memory	1	Write	X	00H			
Set-up Erase/Erase	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EA	A0H	Read	X	EVD
Set-up Program/Program	2	Write	X	40H	Write	PA	PD
Program Verify	2	Write	X	C0H	Read	X	PVD
Reset	2	Write	X	FFH	Write	X	FFH

Table 1 – Command Definitions

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V_{PP} pin. In the absence of this high voltage, memory contents are protected against erasure. Refer to Figures 8 and 10.

Set-Up Program / Program Commands

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to Figure 5, 6 and 7.

Erase-Verify Command

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified. The Erase Verify operation is initiated by writing A0H into the command register. The address for byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The Erase-Verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g., Program Set-up) to the command register. Figure 8 illustrates how commands and bus operations are combined to perform electrical erasure of the memory.

Program-Verify Command

The memory is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

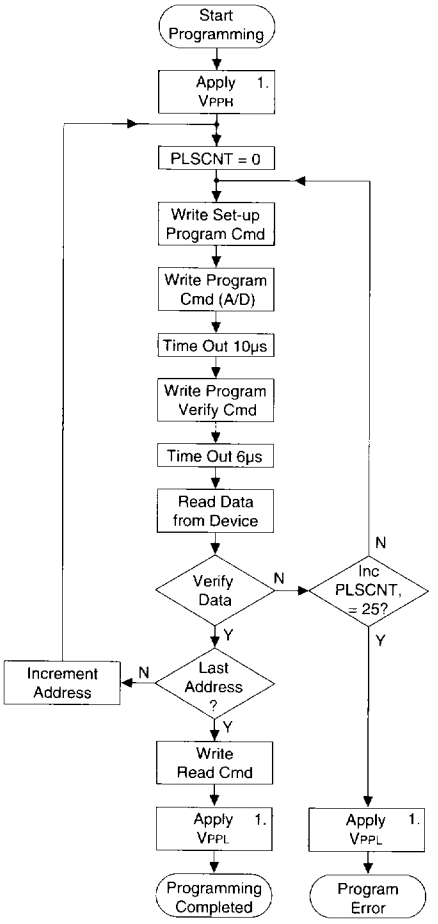
A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 5, the programming algorithm, illustrates how commands are combined with bus operations to perform byte programming.

Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must be written to place the device in the desired state.

PROGRAMMING ALGORITHM

The programming algorithm uses programming operations of 10µS duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figures 5, 6 and 7 illustrate the programming procedure. The algorithm must be followed to ensure proper and reliable operation of the device.



Bus Operation	Command	Comments
Standby		Wait for Vpp ramp to Vpph (= 12.0V)[1]
		Initialize pulse-pulse count
Write	Set-up Program	Data = 40H
Write	Program	Valid address/data
Standby		Duration of Program operation (t_{WHWH1})
Write	Program[2] Verify	Data = C0H; Stops Program Operation
Standby		t_{WHGL}
Read		Read byte to verify programming
Standby		Compare data output to data expected
		Max. Address = FFFFH
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for Vpp ramp to Vppl[1]

Notes:
1. See DC Characteristics for value of Vpph. The Vpp power supply can be hard-wired to the device or switchable. When Vpp is switched, Vppl may be ground, no-connect with a resistor tied to ground, or less than Vcc + 2.0V. (Refer to WF-1024K8 data sheet)
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
3. CAUTION: The algorithm must be followed to ensure proper and reliable operation of the device.

FIGURE 5 – Programming Algorithm

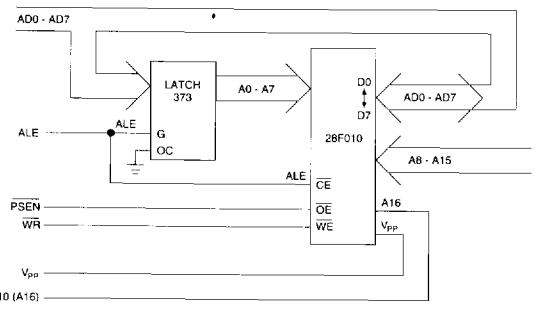


FIGURE 6 – Programming Block Diagram

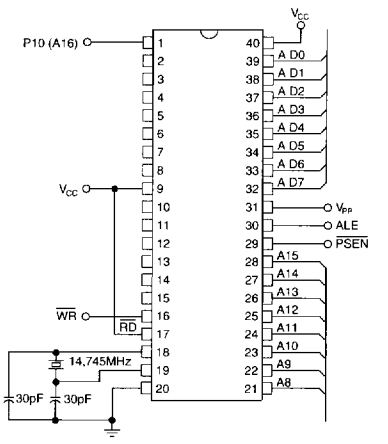


FIGURE 7 – Programming Schematic

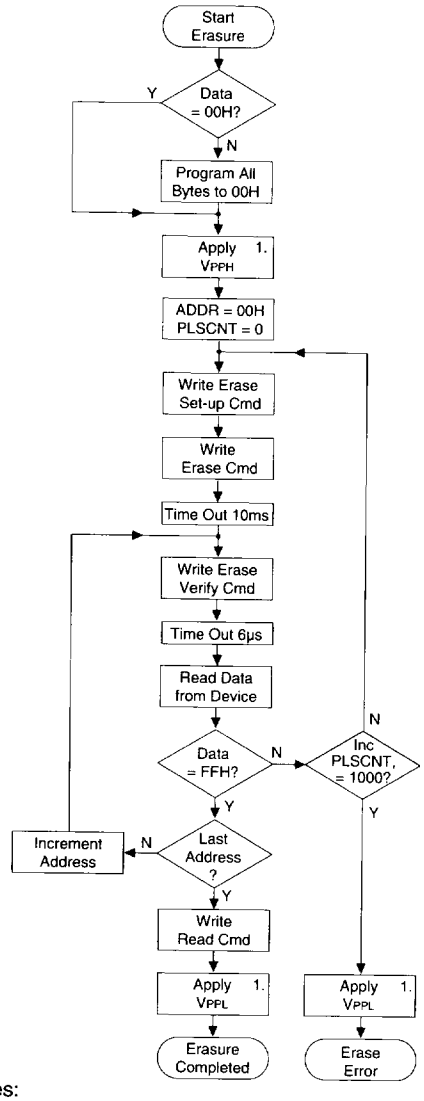
ERASE ALGORITHM

The erase algorithm, Figure 8, yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the programming algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The reading of FFH data from the device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished, using the programming algorithm, in approximately two seconds.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H with pin 1 low and continues through the array to the last address FFFFH, then begins again at address 0000H with pin 1 high and continues through the array to the last address FFFFH, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. The algorithm must be followed to ensure proper and reliable operation of the device.



Bus Operation	Command	Comments
		Entire memory must = 00H before erasure
		NOTE Use Quick-Pulse Programming™ algorithm
Standby		Wait for Vpp ramp to Vpph (=12.0V)[1]
		Initialize Addresses and Pulse Count
Write	Set-up Erase	Data =20H
Write	Erase	Data = 20H
Standby		Duration of Erase operation, t_{WHWH2}, (Table 2)
Write	Erase[2] Verify	Addr = Byte to verify; Data = A0H; Stops Erase Operation
Standby		t_{WHGL}
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
		Last address = IFFFH (4)
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for Vpp ramp to Vppl[1]

Notes:

1. See DC Characteristics for value of Vpph. The Vpp power supply can be hard-wired to the device or switchable. When Vpp is switched, Vppl may be ground, no-connect with a resistor tied to ground, or less than Vcc + 2.0V. (Refer to WF-1024K8 data sheet)
2. Erase verify is performed only after chip erasure. A final read/compare may be performed (optional) after the register is written with the Read command.
3. CAUTION: The algorithm must be followed to ensure proper and reliable operation of the device.
4. P10 is used for the Upper Address (A16) during erasing/programming.

FIGURE 8 – Erase Algorithm

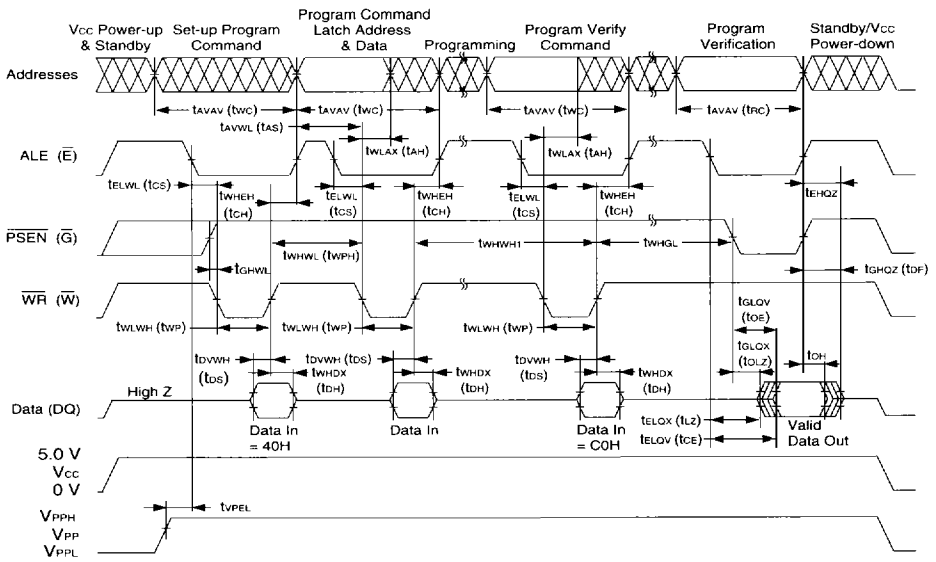


FIGURE 9 – A.C. Waveforms for Programming Operations

Symbol	Characteristic	Min	Max	Unit
t_{AVAV}/t_{WC}	Write Cycle Time	200		nS
t_{AVWL}/t_{AS}	Address Set-up Access Time	30		nS
t_{WLAX}/t_{AH}	Address Hold Time	t_{WP} (1)		nS
t_{DVWH}/t_{DS}	Data Set-up Time	60		nS
t_{WHDX}/t_{DH}	Data Hold Time	15		nS
t_{WHGL}	Write Recovery Time before Read	6		uS

Symbol	Characteristic	Min	Max	Unit
t_{GHWL}	Write Recovery Time before Write	0		uS
t_{WLWH}/t_{WP}	Write Pulse Width	80		nS
t_{WHWL}/t_{WPH}	Write Pulse Width High	20		nS
t_{WHWH1}	Duration of Programming Operation	10	25	uS
t_{WHWH2}	Duration of Erase Operation	9.5	10.5	mS

Table 2 – A.C. Characterisitics - Write/Erase/Program Operations
(1) Minimum $t_{AHZ} \geq t_{WP}$ (Actual)

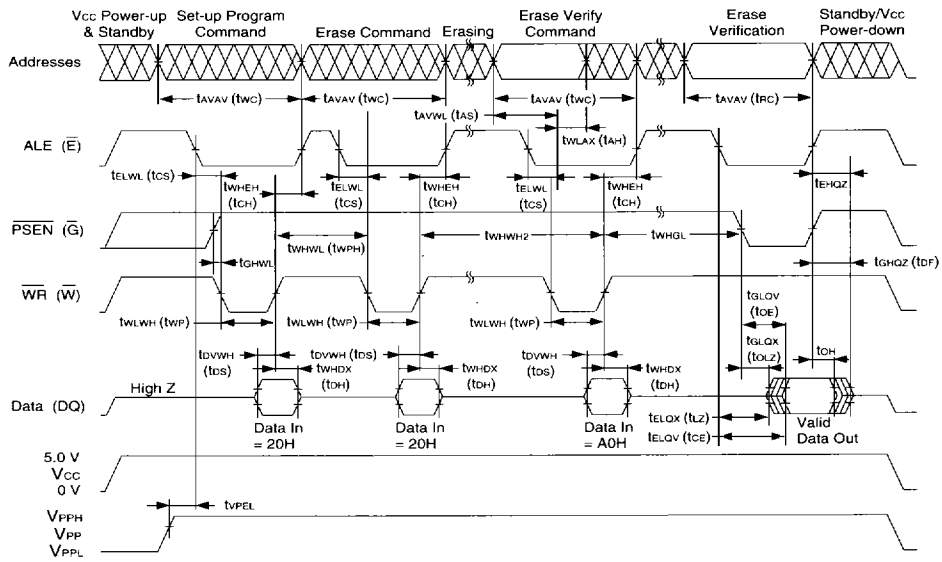


FIGURE 10 – A.C. Waveforms for Erase Operations

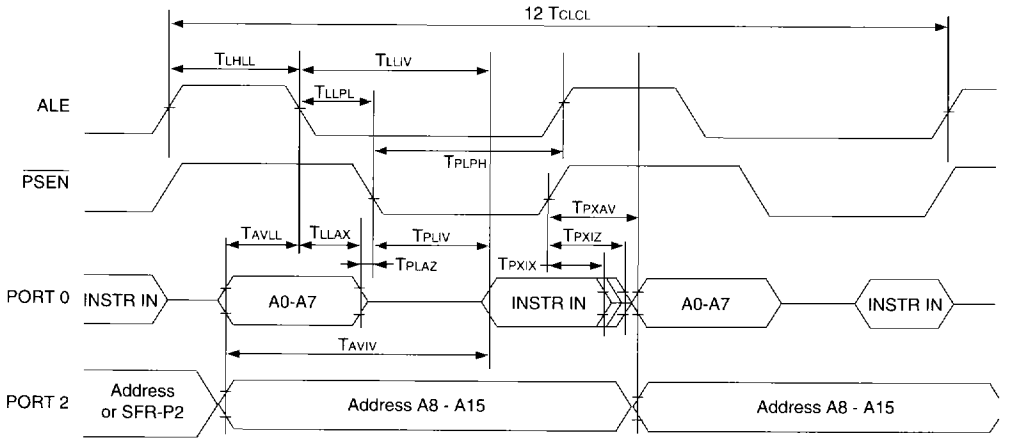


FIGURE 11 – External Program Memory Read Cycle

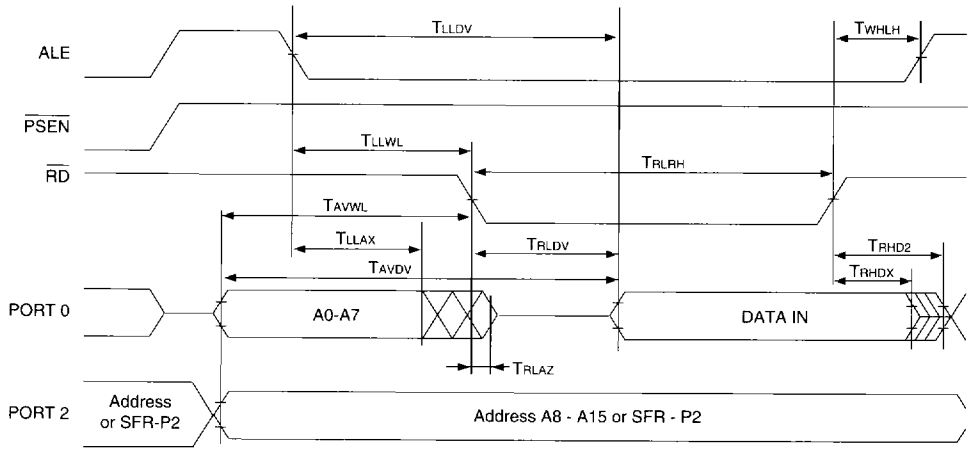


FIGURE 12 – External Data Memory Read Cycle

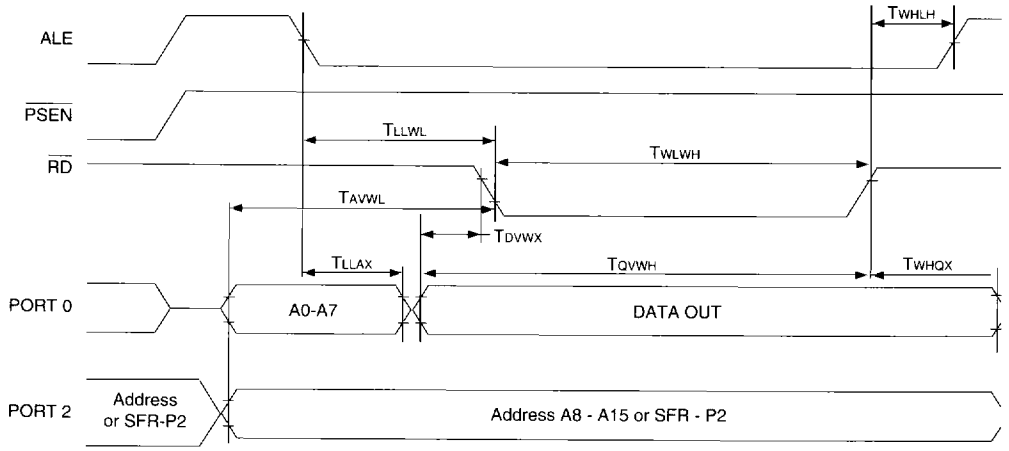


FIGURE 13 – External Data Memory Write Cycle

Symbol	Parameter	Min	Max	Unit
TLHLL	ALE Pulse Width	2TCLCL-55		ns
TAVLL	Address Valid to ALE	TCLCL-70		ns
TLLAX	Address Hold After ALE	TCLCL-50		ns
TLLIV	ALE to Valid instr In		4TCLCL-115	ns
TLLPL	ALE to $\overline{PSEN}$	TCLCL-55		ns
TPLPH	$\overline{PSEN}$ Pulse Width	3TCLCL-60		ns
TPLIV	$\overline{PSEN}$ to Valid instr In		3TCLCL-120	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		ns
TPXIZ	INPUT Instr Float after $\overline{PSEN}$		TCLCL-40	ns
TPXAV	$\overline{PSEN}$ to Address Valid	TCLCL-8		ns
TAVIV	Address to Valid Instr In		5TCLCL-120	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		25	ns

Table 3 – External Program Memory Characteristics

Symbol	Parameter	Min	Max	Unit
TRLRH	$\overline{RD}$ Pulse Width	6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	6TCLCL-100		ns
TLLAX	Data Address Hold After ALE	TCLCL-35		ns
TRLDV	$\overline{RD}$ to Valid Data In		5TCLCL-185	ns
TRHDX	Data Hold After $\overline{RD}$	0		ns
TRHDZ	Data Float After $\overline{RD}$		2TCLCL-85	ns
TLLDV	ALE to Valid Data In		8TCLCL-170	ns
TAVDV	Address to Valid Data In		9TCLCL-185	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	3TCLCL-65	3TCLCL+65	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	4TCLCL-145		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	TCLCL-75		ns
TQVWH	Data Setup to $\overline{WR}$ High	7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	TCLCL-65		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	TCLCL-65	TCLCL+65	ns

Table 4 – External Data Memory Characteristics

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage	-0.5	$0.2V_{CC}$-0.25	V
V_{IH}	Input High Voltage (Except XTAL1, RST)	$0.2V_{CC}$+1.1	V_{CC}+0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	$0.7V_{CC}$+0.2	V_{CC}+0.5	V
V_{OL}	Output Low Voltage		0.45	V
V_{OH}	Output High Voltage	2.4		V
RRST	Reset Pulldown Resistor	40	125	kOhm
IPD	Power Down Current		500	uA
I_{IDL}	Idle Mode Current		8	mA
I_{CC}	Operating Current (@ 14.7456 Mhz)		35	mA
V_{CC}	System Voltage	4.75	5.25	V
V_{PP}	Programming Voltage	11.4	12.6	V

Table 5 – D.C. Characteristics

ORDERING INFORMATION

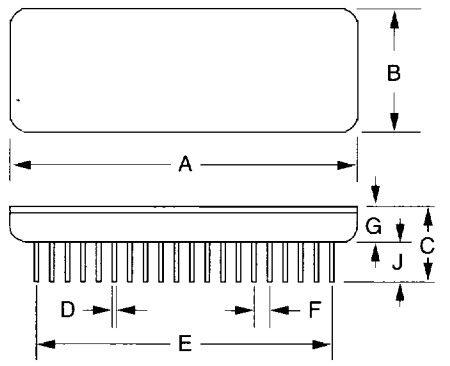
TEMPERATURE RANGE OPTIONS

M	Military	-55°C to +125°C
I	Industrial	-40°C to +85°C

W C8 P31 F-64 X

- **PROCESSING:**
  - M = Military
  - I = Industrial
- **64K Flash**
- **8031 Based**
- **8 Bit Controller**
- **WHITE TECHNOLOGY**

PACKAGE OUTLINE



DIM.	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.068	2.110	52.5	53.6
B	.735	.760	18.7	19.3
C	.336	.420	8.5	10.7
D	.016 Dia.	.020 Dia.	0.4 Dia.	0.5 Dia.
E	1.855	1.905	47.1	48.4
F	.095	.105	2.4	2.7
G	.170	.200	4.3	5.1
H	.595	.605	15.1	15.4
J	.160	.220	4.1	5.6

White Technology, Inc.
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Tel: 602-437-1520 Fax: 602-437-9120

NOTES:

OTHER PRODUCTS FROM WHITE TECHNOLOGY, INC.

Application Specific Multichip Modules for Military, Industrial and Commercial Applications

- Customer specified processors, coprocessors, memory, temperature ranges, packaging and other application specific requirements.
- Engineering support from circuit design through final package assembly.
- Facility certified to MIL-STD-1772.
- Military screening available to meet requirements of MIL-H-38534 and Test Method 5008 of MIL-STD-883.

Standard SRAM Modules

- 25 to 120 nS speeds
- 512K x 8, 256K x 8, 128K x 8
- 32 pin JEDEC DIP pinouts
- Military, Industrial and Commercial temperatures
- Military screening available
- Low power CMOS

Mega Memory Modules

- 64M SRAM configurable to 8M x 8, 4M x 16 or 2M x 32
- 128M Flash PROM configurable to 16M x 8, 8M x 16 or 4M x 32
- Customer defined memory capacities and packaging

Standard EEPROM Modules

- 512K x 8, 256K x 8, 128K x 8
- 150 nS access time
- Low power CMOS
- 32 pin JEDEC DIP pinouts
- Military, Industrial and Commercial temperatures
- Military screening available

Standard Microcontroller Modules

- 80C88 based with 16K x 8 SRAM and 16K x 8 EEPROM
- 68020 based with 32K x 32 SRAM, 32K x 32 EEPROM, optional 68881FPC
- i486™ based with 512K x 32 SRAM, 1M x 32 EEPROM; advanced info
- i960™ based under development

Represented by: