

R2J25953SP

H-Bridge Control High Speed Power Switching with Built-in Driver IC and Power MOS FET

R07DS0044EJ0400

Rev.4.00

May 09, 2013

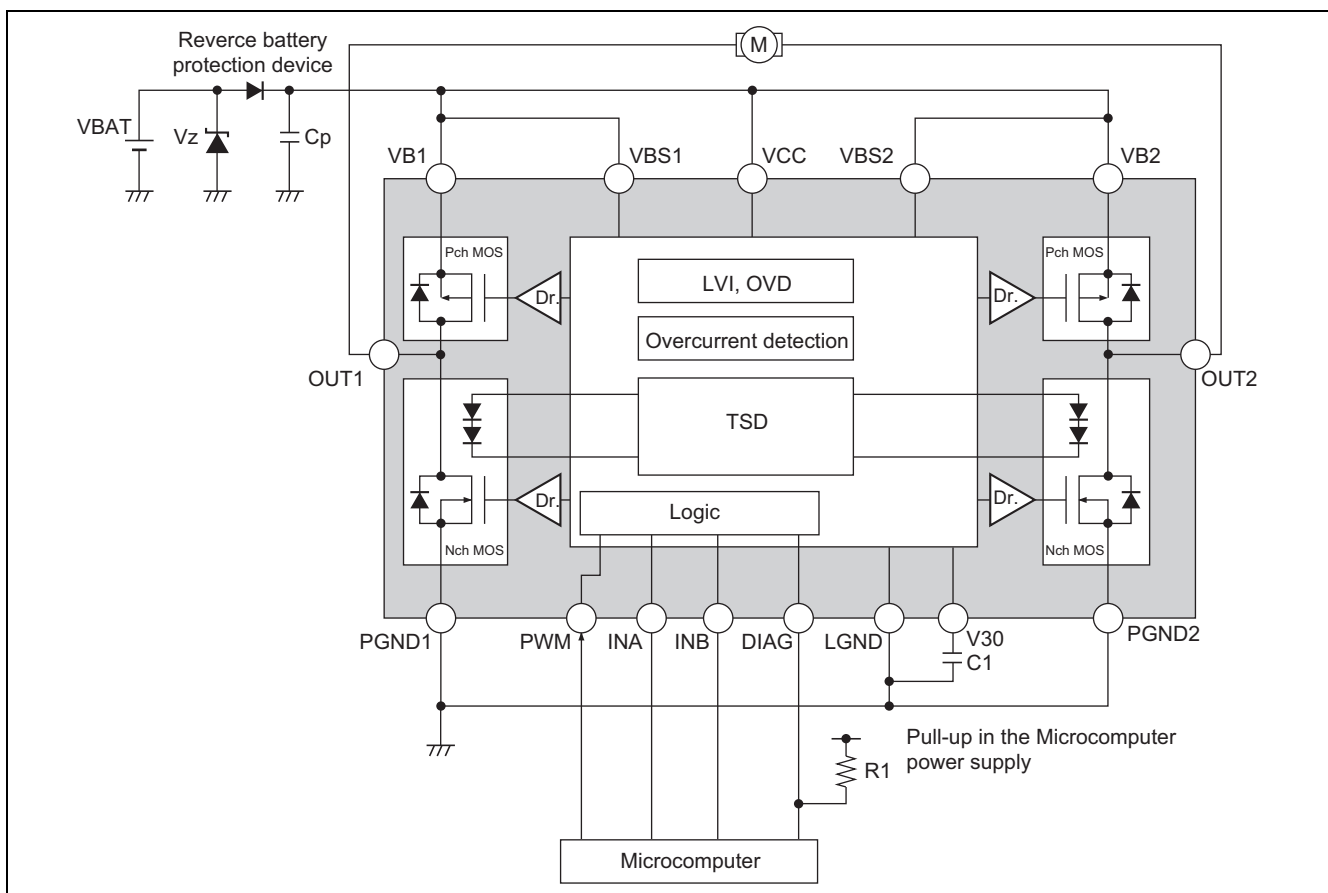
Description

The R2J25953 multi-chip module incorporates high-side Pch MOS FET, low-side Nch MOS FET, and Bi-CMOS driver in a single HSOP-36 package.

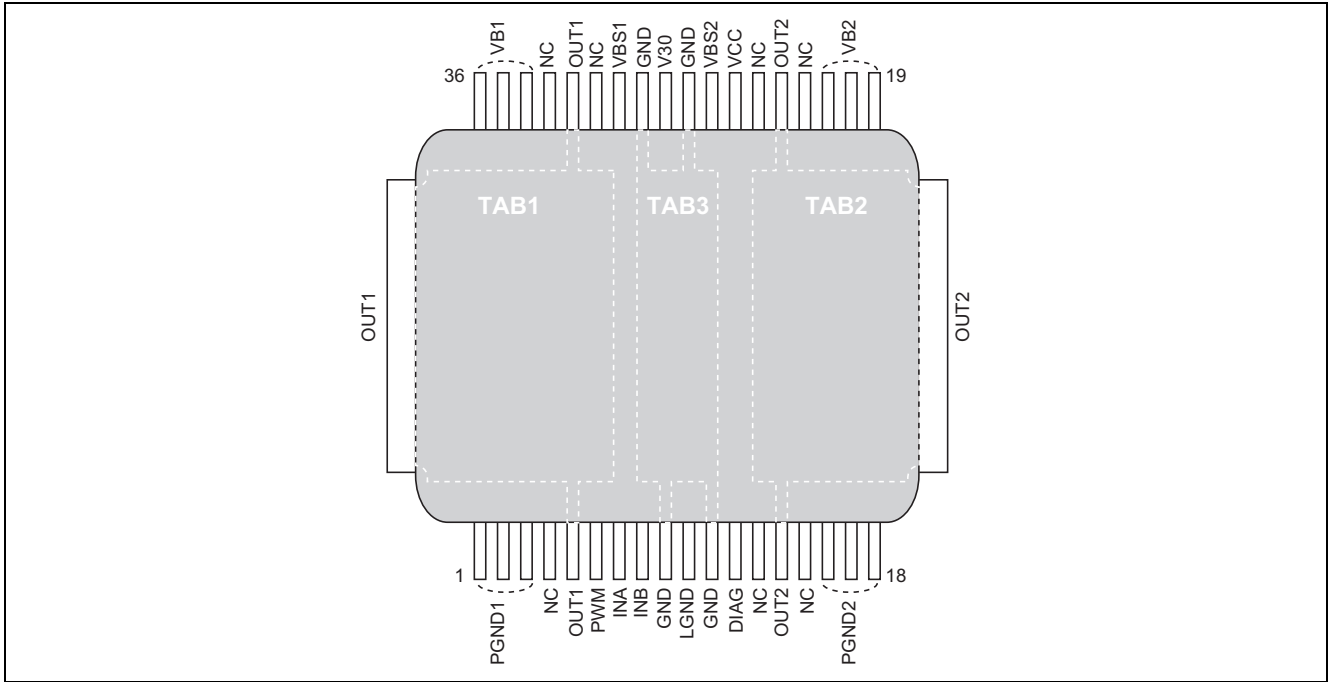
Features

- For Automotive application
- Built-in low on state resistance MOS FET.
(Pch: 16 mΩ Max., Nch: 11 mΩ Max.)
- Pch MOS FET is adopted on the high-side, and the charge pump noise was lost.
- Built-in protection circuit of Thermal shut-down (TSD), Low Voltage Inhibit (LVI), Overvoltage Detection (OVD) and Overcurrent Detection.
- Built-in diagnostic function.
- Built-in cross-conduction protection.
- Small Surface mounting package: HSOP-36

Block Diagram



Outline



Pin Description

| Pin No. | Pin name | Description | Pin No. | Pin name | Description |
|----------|----------|--------------------------------|----------|----------|------------------------------|
| 1 to 3 | PGND1 | Power GND1 | 22 | NC | No connect |
| 4 | NC | No connect | 23 | OUT2 | Internally corrected to TAB2 |
| 5 | OUT1 | Internally corrected to TAB1 | 24 | NC | No connect |
| 6 | PWM | PWM input | 25 | VCC | IC power supply |
| 7 | INA | A input | 26 | VBS2 | VB2 sense |
| 8 | INB | B input | 27 | GND | Internally corrected to TAB3 |
| 9 | GND | Internally corrected to TAB3 | 28 | V30 | IC bias voltage (3.3 V) |
| 10 | LGND | IC GND | 29 | GND | Internally corrected to TAB3 |
| 11 | GND | Internally corrected to TAB3 | 30 | VBS1 | VB1 sense |
| 12 | DIAG | Diagnostic output (open drain) | 31 | NC | No connect |
| 13 | NC | No connect | 32 | OUT1 | Internally corrected to TAB1 |
| 14 | OUT2 | Internally corrected to TAB2 | 33 | NC | No connect |
| 15 | NC | No connect | 34 to 36 | VB1 | MOS FET power supply 1 |
| 16 to 18 | PGND2 | Power GND2 | TAB1 | OUT1 | MOS FET output 1 |
| 19 to 21 | VB2 | MOS FET power supply 2 | TAB2 | OUT2 | MOS FET output 2 |
| | | | TAB3 | GND | IC tab GND |

Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Ratings | Unit | Note |
|----------------------|--------|-------------|------|------|
| Supply voltage | VB | 18 | V | 1 |
| Input voltage | Vin | -0.3 to VB | V | 2 |
| Diag voltage | Vdiag | -0.3 to VB | V | 3 |
| Output current | Iout | 50 | A | |
| Diag current | Idiag | 5 | mA | 3 |
| Junction temperature | Tj | -40 to +150 | °C | |
| Storage temperature | Tstg | -55 to +150 | °C | |
| Power temperature | Pt | 40 | W | 4 |

Notes: 1. 28 V at 25°C, 1 min.

40 V at 25°C, 1 sec.

2. Applies to INA, INB, and PWM. Clamps it with 19 V typ.

3. Applies to DIAG

4. One element operation: Tc = 25°C

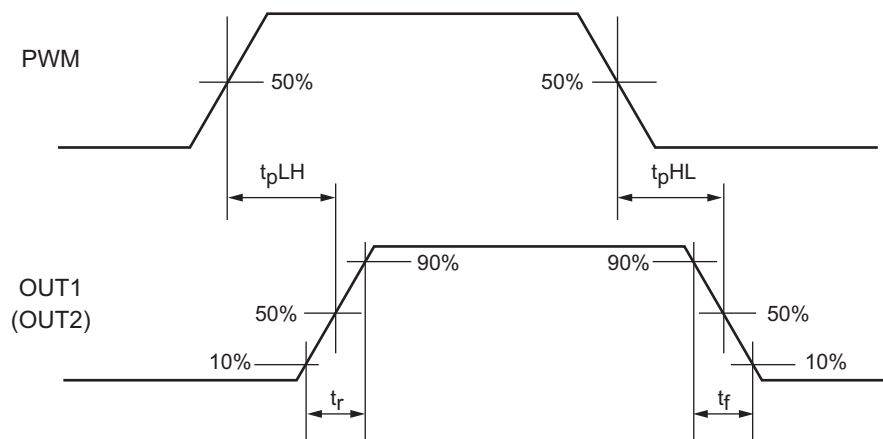
Electrical Characteristics

(Ta = 25°C, VB = VCC = 12 V)

| Item | | Symbol | Min | Typ | Max | Unit | Condition | Application terminal | Note |
|-----------------------|-----------------------------|--------|------|------|------|------|--|----------------------|------|
| Supply current | | Icc0 | — | 30 | 50 | μA | Standby | VCC | 1 |
| | | Icc | — | 3.5 | 10 | mA | ACTIVE | | 1 |
| VB | Input current | IinVB | — | — | ±1 | μA | Standby | VB1/VB2 | 1 |
| MOS | Static High-side resistance | RonH | — | 9 | 16 | mΩ | Iout = 15 A Pulse test | | |
| | Static Low-side resistance | RonL | — | 7 | 11 | mΩ | Iout = 15 A Pulse test | | |
| | Off state current | Ioff | — | 10 | 20 | μA | | | |
| IN | Input current | IinL | — | — | ±10 | μA | Vin = 0 V | INA/INB /PWM | |
| | | IinH | — | — | ±10 | μA | Vin = VB | | |
| | High threshold | Vthin | 3.0 | — | — | V | | | |
| | Low threshold | Vtlin | — | — | 1.5 | V | | | |
| Delay time | | tpLH | — | 1.5 | 4.0 | μs | OUT/IN (PWM) | OUT, PWM | 2 |
| | | tpHL | — | 3.0 | 6.0 | μs | | | |
| Rise time | | tr | — | 1.0 | 3.0 | μs | OUT | OUT1/2 | |
| Fall time | | tf | — | 1.0 | 3.0 | μs | | | |
| DIAG | Output voltage | VDiag | — | 0.4 | 0.6 | V | I = 2 mA, DIAG = Low Vdiag = 0 V | DIAG | |
| | Leak current | IDiag | — | — | ±10 | μA | | | |
| TSD | Shut-down temperature | Tsd | 150 | 175 | — | °C | | | 3 |
| | Hysteresis | Thys | 7 | 25 | — | °C | | | |
| OVD | Shut-down voltage | VtvH | 28.9 | 34 | 39.1 | V | | VCC | |
| | Return voltage | VtvL | 21.3 | 25 | 28.7 | V | | | |
| LVI | Return voltage | VRLVI | 5.0 | 5.35 | 5.6 | V | | VCC | |
| | Hysteresis | VHLVI | 0.3 | 0.5 | 0.7 | V | | | |
| Overcurrent detection | Shut-down current | IcL | 35 | — | — | A | | OUT1/2 | |
| | Detection time | tcL | 60 | 10 | 20 | μs | | | |
| MOS FET Body-diode | Pch forward voltage | VDFp | — | 1.0 | 1.3 | V | IF = 50 A, Pulse test | | |
| | Nch forward voltage | VDFn | — | 1.0 | 1.3 | V | | | |

Notes: 1. Refer to truth table.

2. Refer to the input condition to the truth table.



3. It is a design guaranteed value, and it doesn't apply to the final test.

Truth table

The operation of OUT1, OUT2, and DIAG is shown in the following.

| Input | | | Status | | | | Output | | | State |
|--|------|------|------------------------------------|-----|-----------------------|-----|-----------------|-----------------|----------------|--------------------------|
| PWM | INA | INB | LVI | TSD | Overcurrent detection | OVD | OUT1 | OUT2 | DIAG | |
| High | High | High | off | | | | High | High | High | ACTIVE |
| | | Low | off | | | | High | Low | High | |
| | Low | High | off | | | | Low | High | High | |
| | | Low | off | | | | Low | Low | High | |
| Low | High | High | off | | | | Hi-z | Hi-z | High | |
| | | Low | off | | | | Hi-z | Low | High | |
| | Low | High | off | | | | Low | Hi-z | High | |
| | | Low | Protection circuit doesn't operate | | | | Low | Low | High | |
| Excluding All = Low At least one of PWM, INA, and INB is high. | | | on | x | x | x | Hi-z | Hi-z | High | LVI |
| | | | off | on | x | x | Hi-z | Hi-z | Low | TSD |
| | | | off | x | on | x | Hi-z (Latch) | Hi-z (Latch) | Low (Latch) | Overcurrent detection |
| | | | off | x | x | on | Hi-z | Hi-z | Low | OVD |

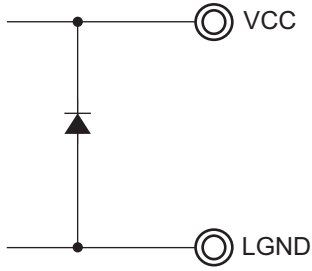
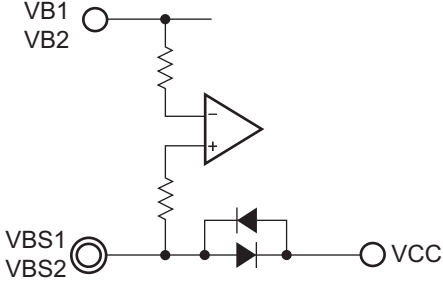
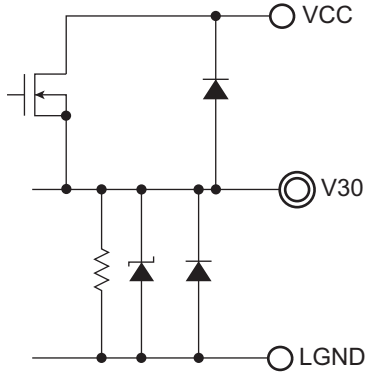
- Notes
1. x: Regardless of High, Low, on and off.
 2. Protect circuit
off = undetection
on = detection
 3. State of pin OUT
Low: Nch MOS FET ON, High: Pch MOS FET ON, Hi-z: Nch and Pch MOS FET OFF
 4. The latch of overcurrent detection is released when LVI = on or INA = INB = Low.

External Parts List

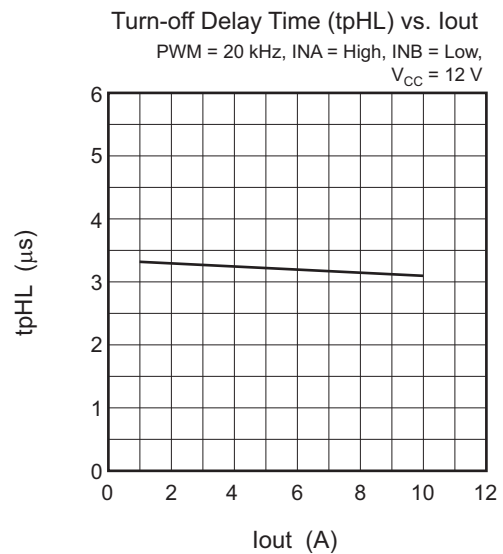
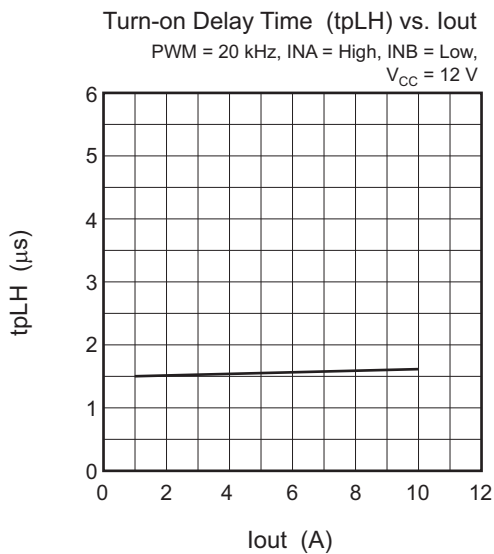
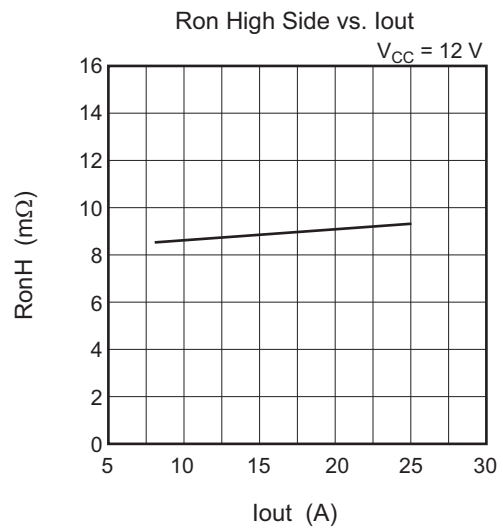
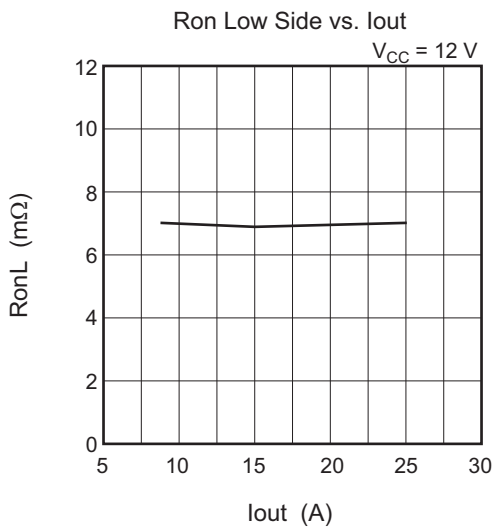
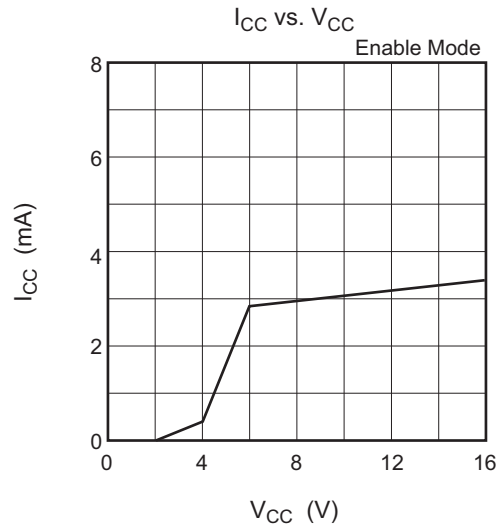
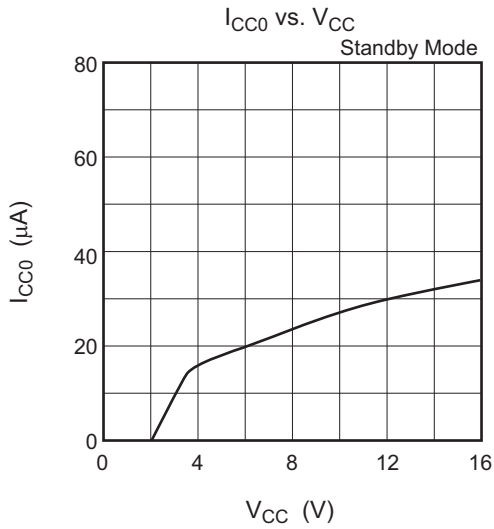
| Parts No. | Recommended value | Purpose |
|-----------|-------------------|-------------------------------|
| Cp | 10 μ F | Power supply bypass capacitor |
| R1 | > 10 k Ω | Pull up Pin DIAG |
| C1 | 0.033 μ F | Pin V30 bypass capacitor |

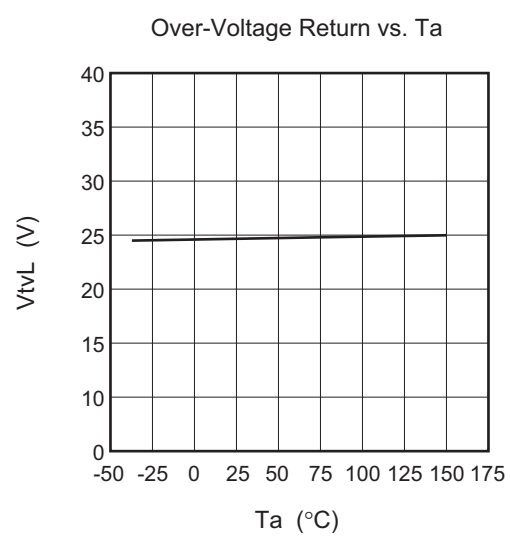
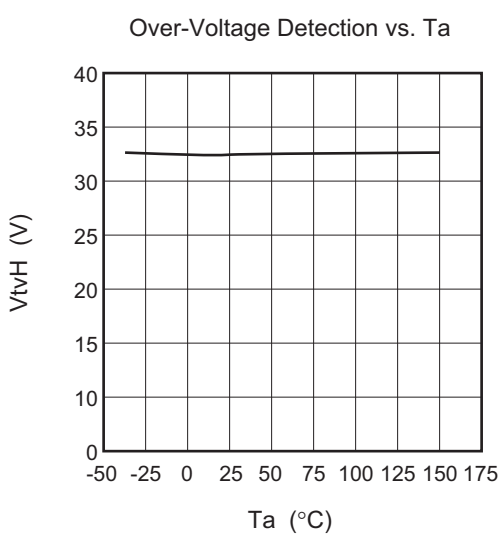
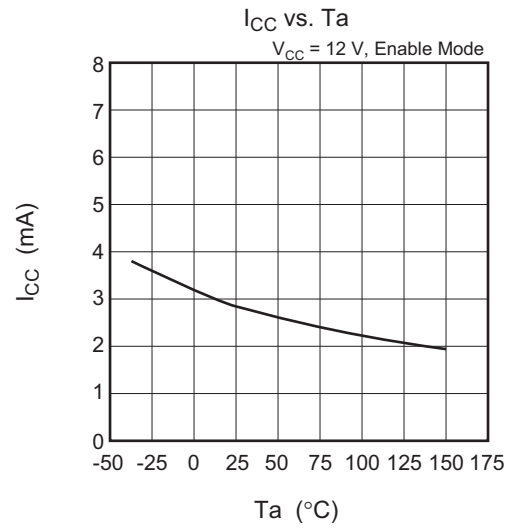
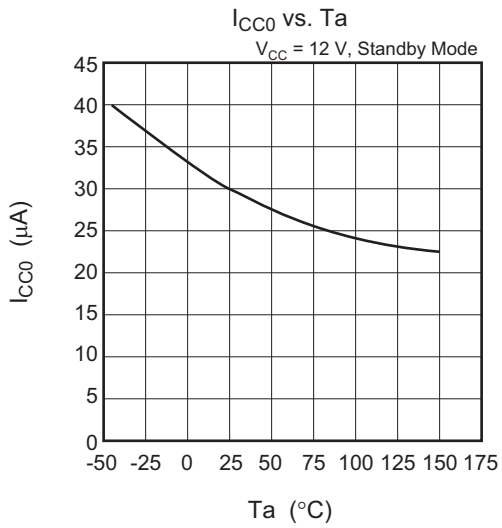
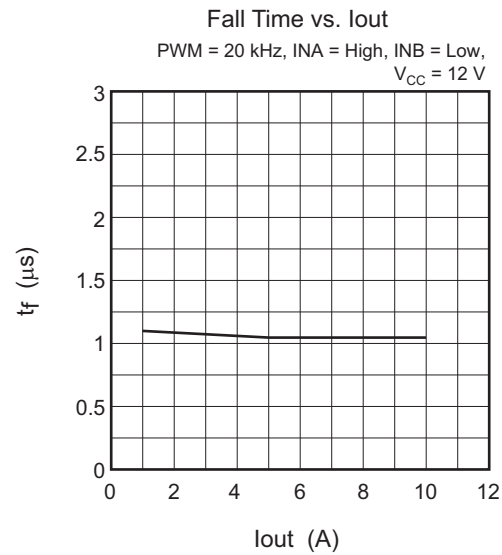
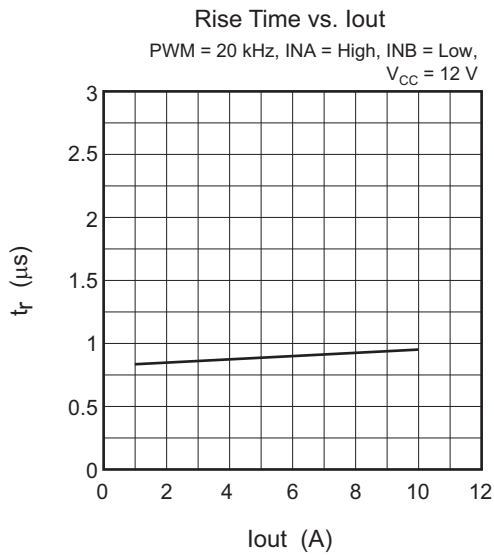
Equivalent Circuit

| Pin name | Pin No. | Equivalent circuit |
|-------------------|-----------------------------|--------------------|
| PGND1 PGND2 | 1, 2, 3, 16, 17, 18 | |
| OUT1 OUT2 | 5, 32, TAB1 14, 23, TAB2 | |
| PWM INA INB | 6 7 8 | |
| DIAG | 12 | |
| VB1 VB2 | 34, 35, 36 19, 20, 21 | |

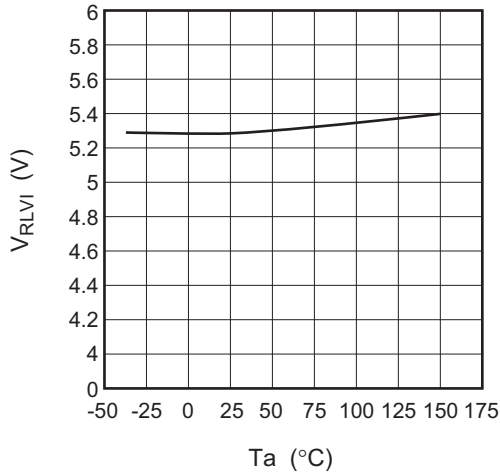
| Pin name | Pin No. | Equivalent circuit |
|--------------|----------|---|
| VCC LGND | 25 10 |  |
| VBS1 VBS2 | 30 26 |  |
| V30 | 28 |  |

Main Characteristics

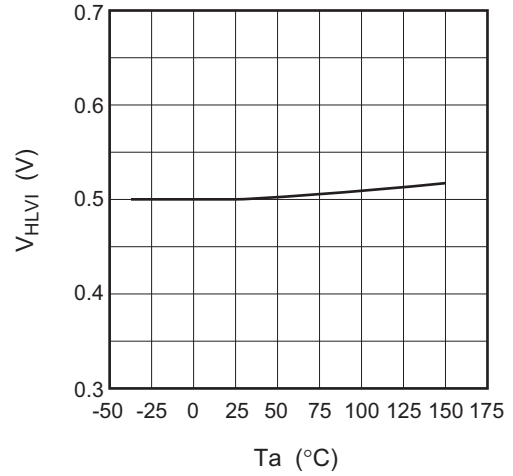




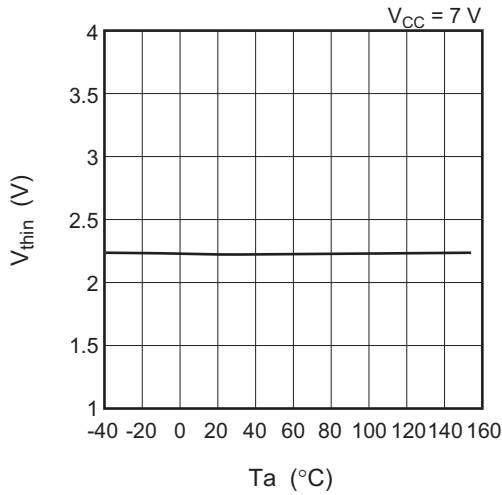
Low-Voltage Inhibit Return vs. Ta



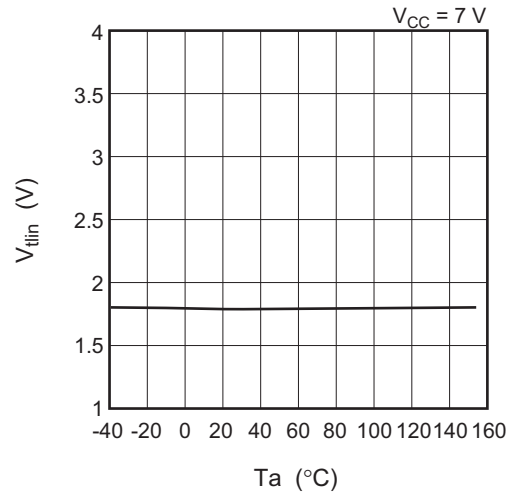
Low-Voltage Inhibit Hysteresis vs. Ta



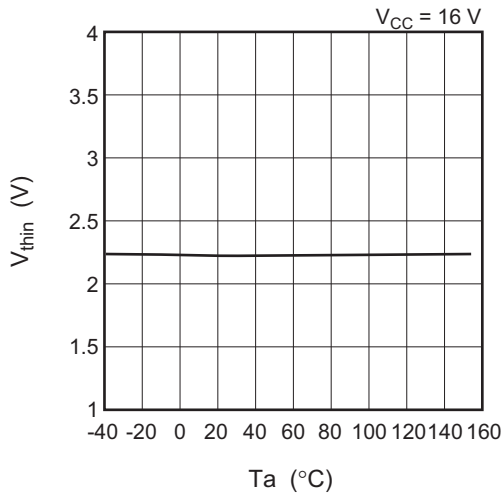
High Level Input Voltage vs. Ta
(PWM/INA/INB)



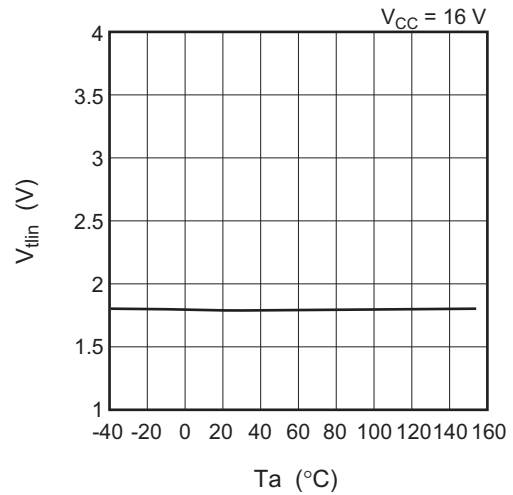
Low Level Input Voltage vs. Ta
(PWM/INA/INB)

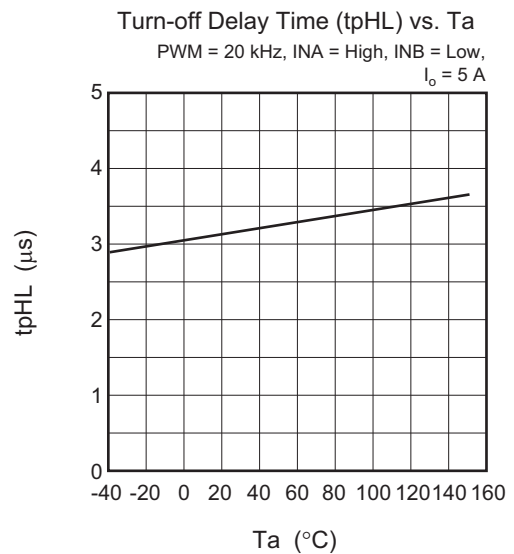
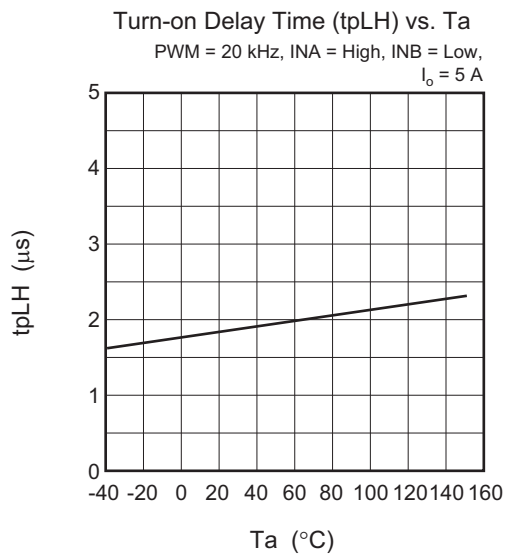
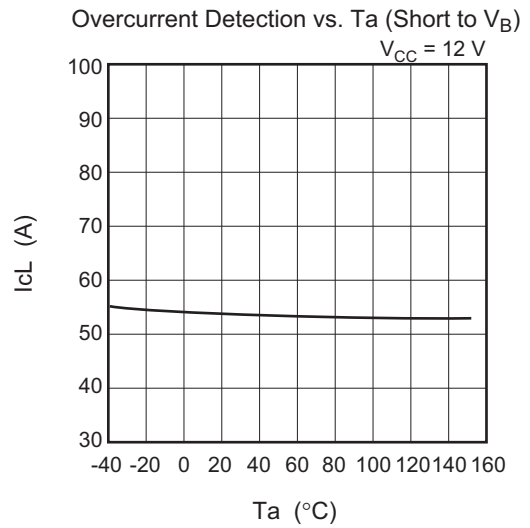
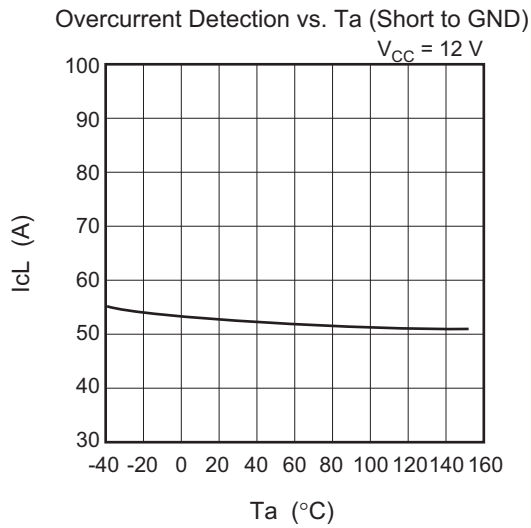
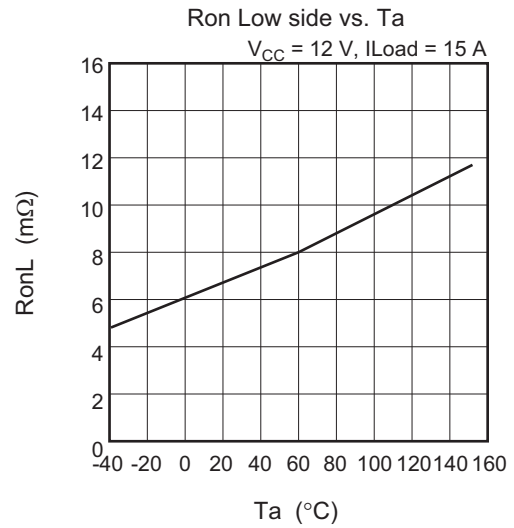
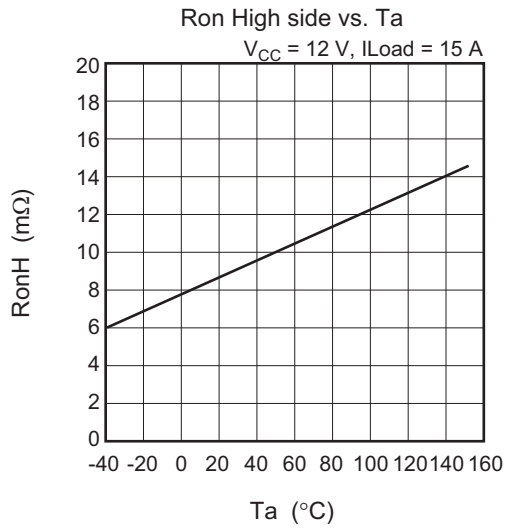


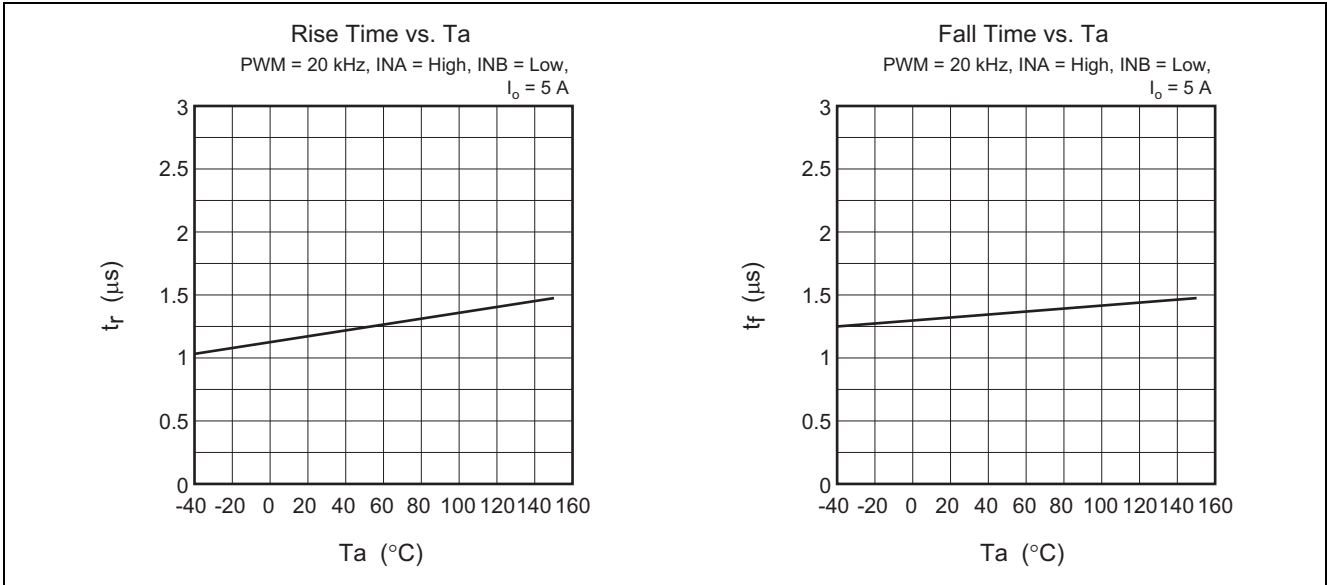
High Level Input Voltage vs. Ta
(PWM/INA/INB)



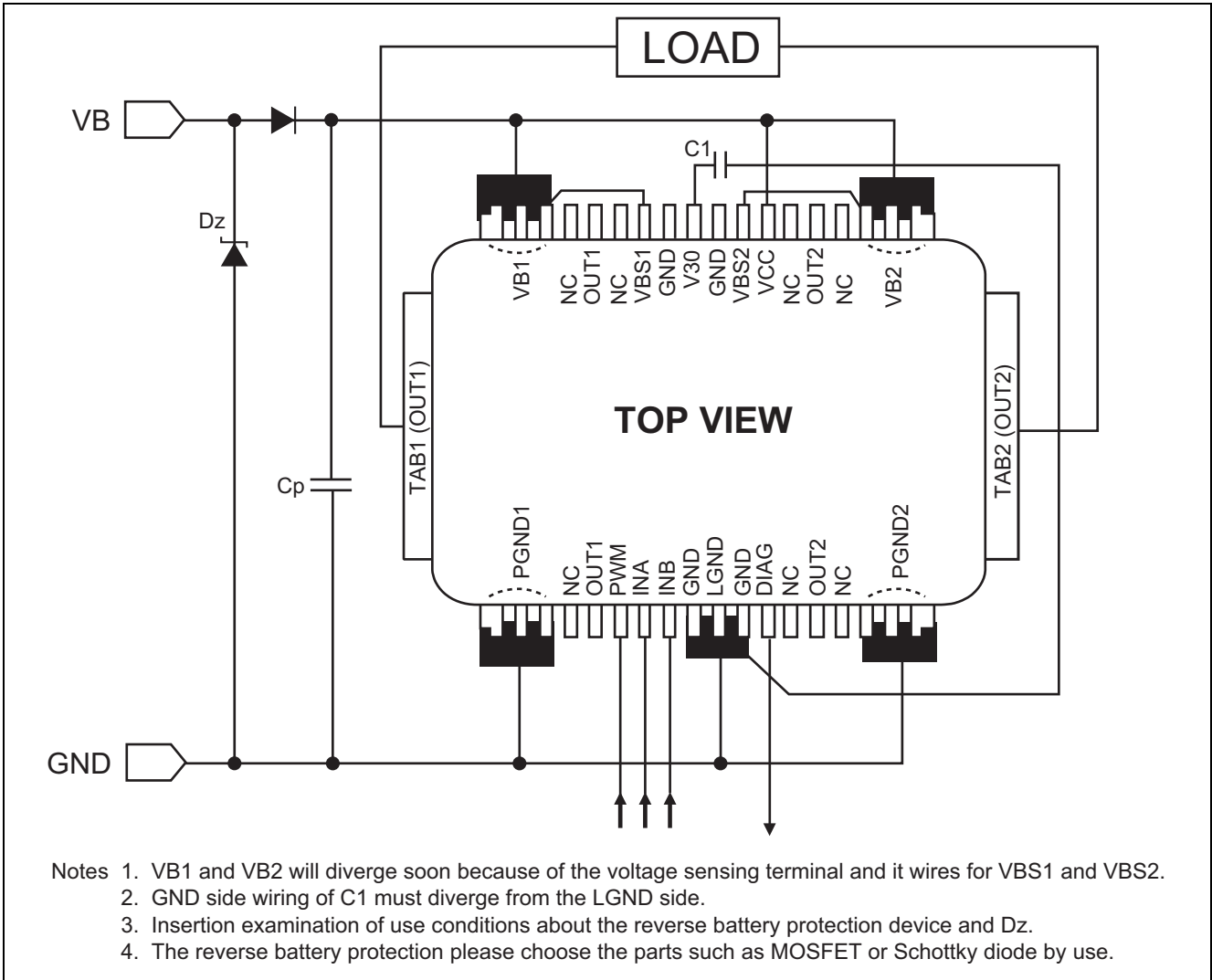
Low Level Input Voltage vs. Ta
(PWM/INA/INB)







Recommended Wiring Pattern

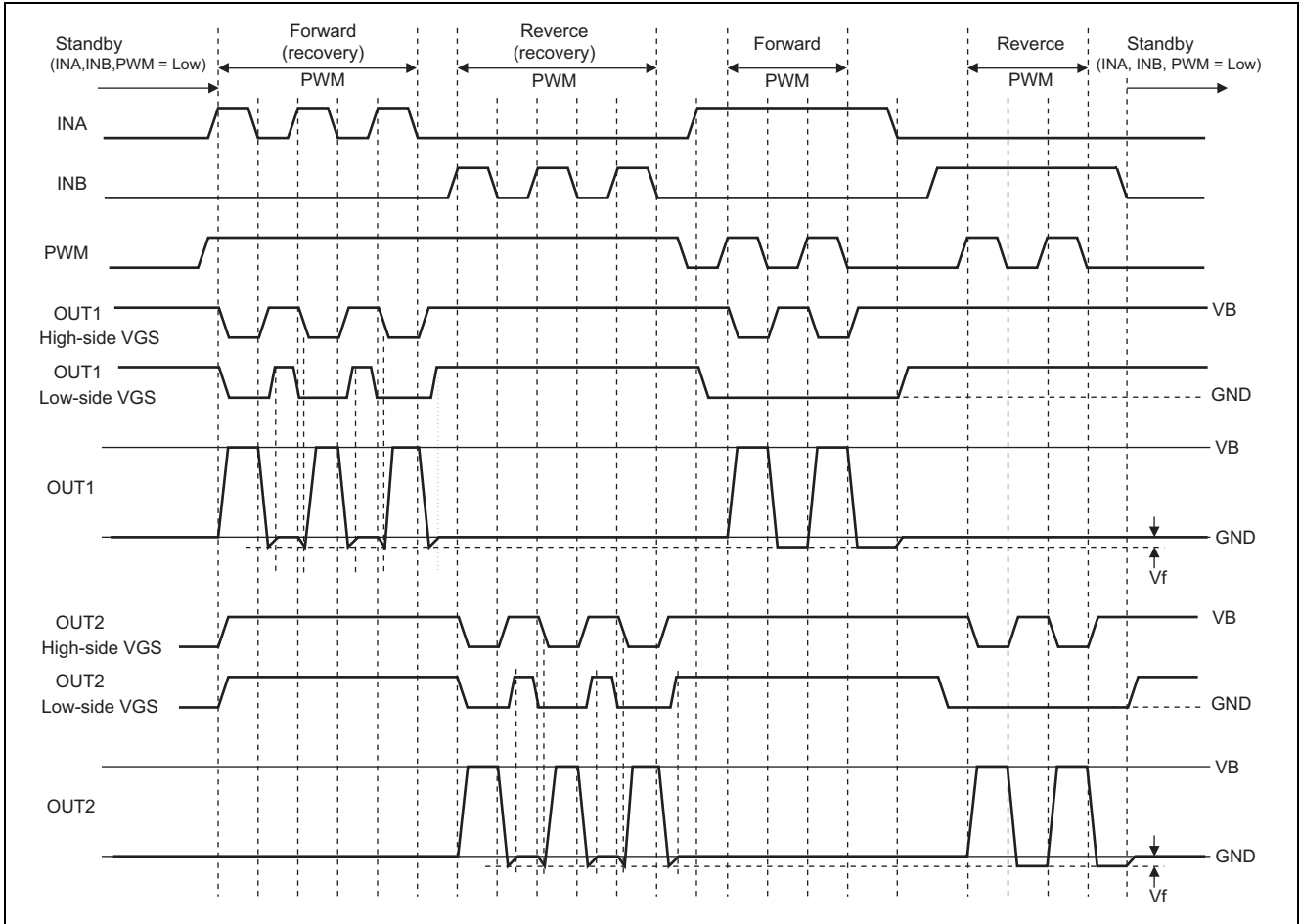


Operational Mode

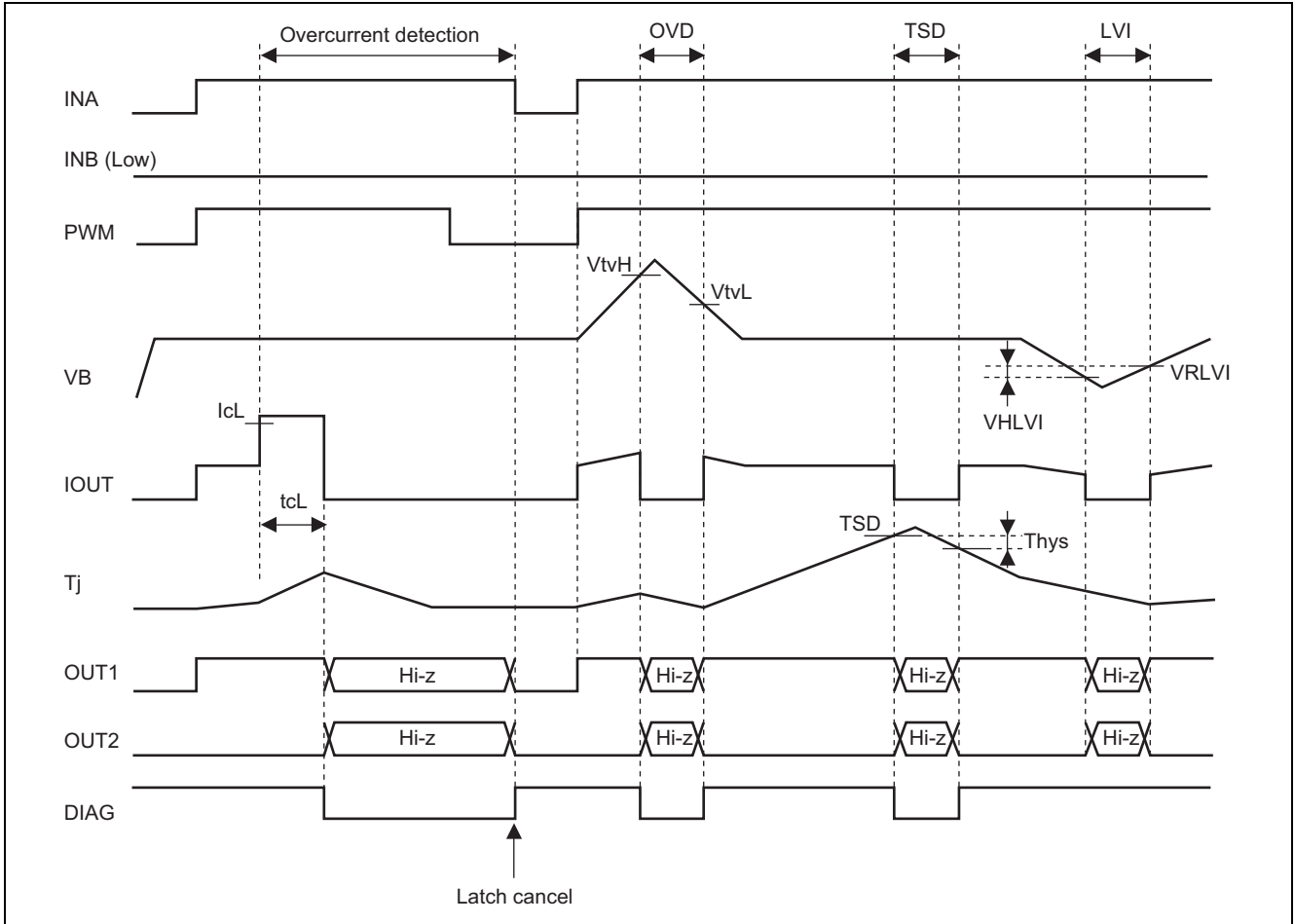
When PWM is controlled, recovery control can be selected because of the low loss. However, please note that reverse-brake hangs at acceleration of the motor.

| Operational mode | Circuit operational |
|---|---------------------|
| <p>Example 1. Forward mode (Recovery control)</p> <p>INA = PWM on/off</p> <p>INB = Low</p> <p>PWM = High</p> | |
| <p>Example 2. Reverse mode (Recovery control)</p> <p>INA = Low</p> <p>INB = PWM on/off</p> <p>PWM = High</p> | |
| <p>Example 3. Forward mode (No recovery control)</p> <p>INA = High</p> <p>INB = Low</p> <p>PWM = PWM on/off</p> | |
| <p>Example 4. Reverse mode (No recovery control)</p> <p>INA = Low</p> <p>INB = High</p> <p>PWM = PWM on/off</p> | |

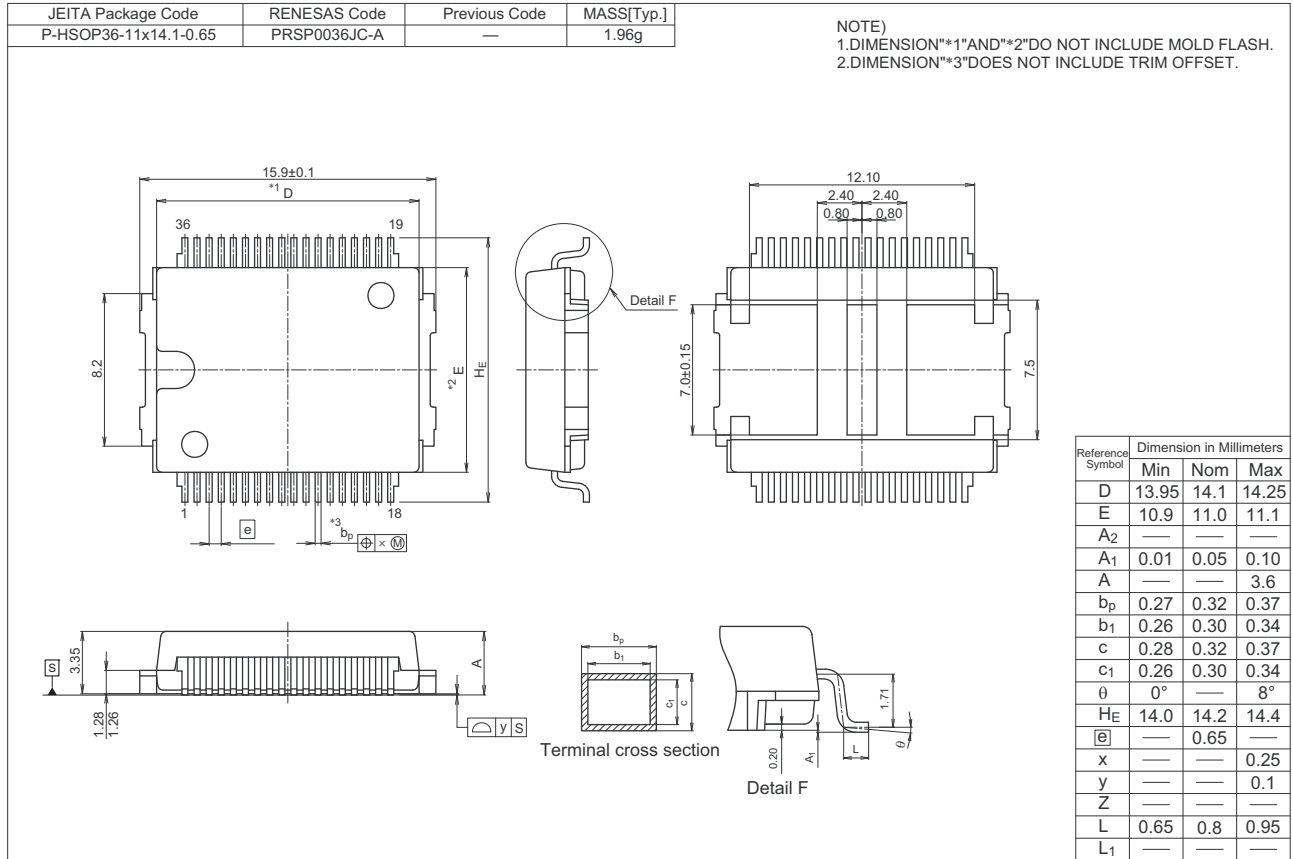
Timing Chart (Normal operation)



Timing Chart (Protection operation)



Package Dimensions



Ordering Information

| Orderable Part Number | Quantity | Shipping Container |
|-----------------------|--------------|--------------------|
| R2J25953SP-00-Q2 | 700 pcs/ box | Taping |

Note: The symbol of 2nd "-" is occasionally presented as "#".

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Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

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