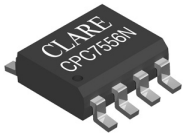
CPC7556
Diode Bridge with Integrated Adjustable OVP Circuit



Bridge Characteristics

Parameter	Rating	Units
Reverse Voltage	100	V
Forward Current	240	mA_{rms}
Thyristor Current	120	mA

Features

- Monolithic Construction
- Surface Mount Package

Applications

- Telecommunications Protection Clamp
- High Voltage Multiplexer/Switch
- High Voltage ESD Clamp

Description

100V Diode Bridge with an integrated Over-Voltage Protection (OVP) thyristor uses Clare's High Voltage SOI technology.

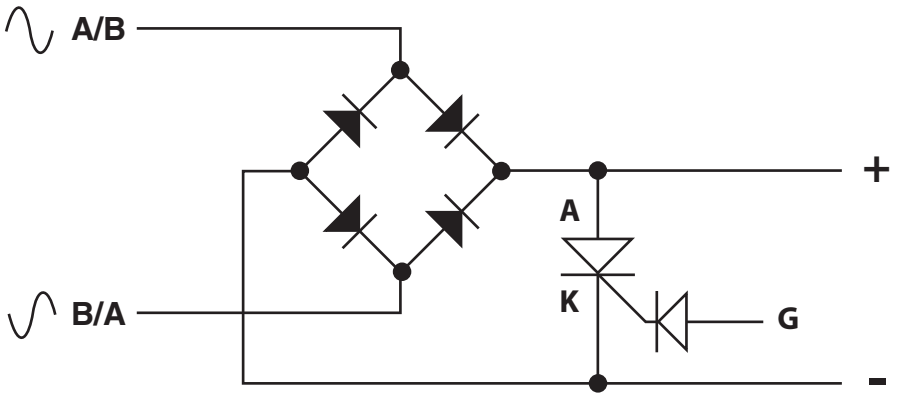
The CPC7556N integrated diode bridge offers protection from high voltage transients by means of an adjustable voltage clamp. The clamp performs two actions, first to limit the voltage across the diode bridge rectified outputs to a value determined by external resistors and the gate voltage and second to fully discharge the V_+ to V_- outputs when the Gate's trigger threshold is exceeded during the voltage limiting function. The rectified outputs are discharged as a result of the voltage fold-back function of the OVP device. Voltage fold back of the OVP circuit will continue until the current through the protector falls below the hold current threshold.

Terminating the gate to V_- will disable the clamp voltage feature up to the thyristor's off state voltage.

Ordering Information

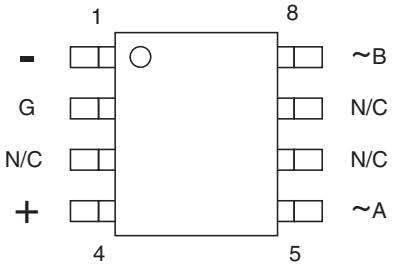
Part	Description
CPC7556N	8-Pin SOIC in Tubes (50/Tube)
CPC7556NTR	8-Pin SOIC Tape & Reel (1000/Reel)

CPC7556N Diagram



1 Specifications

1.1 Package Pinout



1.2 Pin Description

Pin#	Name	Description
1	–	Negative Bridge Output
2	G	Thyristor Gate
3	N/C	No Connection
4	+	Positive Bridge Output
5	~A	Input A
6	N/C	No Connection
7	N/C	No Connection
8	~B	Input B

1.3 Absolute Maximum Ratings

Unless Otherwise Specified all electrical ratings are at 25°C

Parameter	Symbol	Minimum	Maximum	Units
Reverse Voltage	V_{RRM}	-	120	V
Diode Forward Current (Average)	I_F	-	250	mA_{rms}
Diode Forward Surge Current	I_{FSM}	-	2	A
Gate Voltage	V_{GK}	-4	7	V
Gate Current	I_{GK}	-	20	mA
Overvoltage Current	I_{AK}	-	120	mA
Thyristor Surge Current	I_{TSM}	-	1.2	A
Fusing Current	I^2t	-	0.02	A^2s
ESD, Human Body Model	-	-	3	kV
Junction Temperature [1]	T_J	-	+150	°C
Storage Temperature	T_{STG}	-65	+150	°C

[1] Derate package for P_{DISS} 120°C/W.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Diode Forward Current (Average)	I_F	-	240	mA_{rms}
Reverse Voltage	V_R	-	100	V
Operating Temperature Range	T_A	-40	+125	°C
Thermal Impedance	θ_{JA}	120	-	°C/W

1.5 General Conditions

Typical values are characteristic of the device at 25°C and are the result of engineering evaluations. They are provided for information purposes only and are not part of the manufacturing testing requirements.

Unless otherwise noted, all electrical specifications are listed for T_A=25°C.

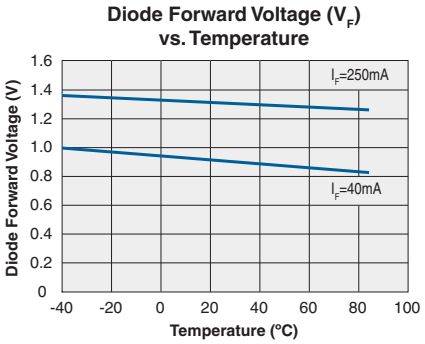
1.6 DC Electrical Characteristics

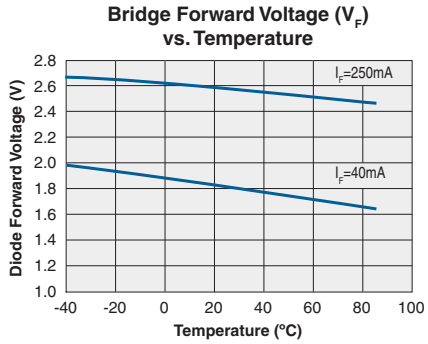
Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Diode Bridge Characteristics:						
Forward Current	-	I_F	-	-	240	mA_{rms}
Diode Forward Voltage Drop	I_F = 40mA	V_F	0.83	0.91	0.97	V
	I_F = 250mA		1	1.3	1.49	
Reverse Voltage Leakage Current	V_R = 100V	I_R	-	-	1	µA
Thyrister Characteristics:						
Gate Trigger Current	$V_{+/-} = V_{AK}$ = 10V, I_{AK} = 110mA	I_{GT}	0.5	1.2	1.8	mA
Gate Trigger Voltage		V_{GK}	2.5	2.8	3.2	V
Trigger Current	-	I_{AKT}	-	25	40	mA
Hold Current	-	I_H	70	100	-	mA
Peak Off State Voltage	V_{GK} = 0V, I_{AK} = 5 uA	V_{DRM}	110	-	-	V

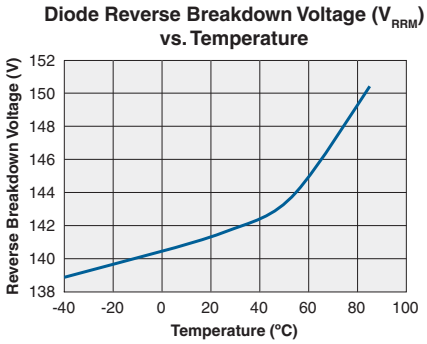
1.7 AC Electrical Characteristics

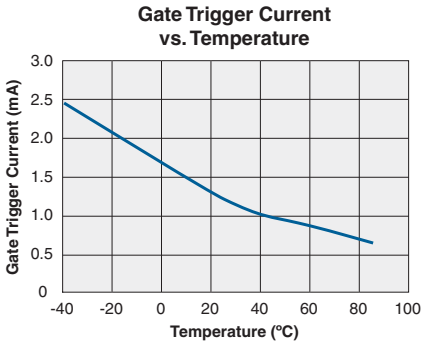
Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Zero Bias Capacitance	$V_+ - V_- = 0V$ Measured from $V_{\sim A}$ to $V_{\sim B}$	$C_{\sim A\sim B}$	-	4.4	12	pF
Output Zero Bias Capacitance	$V_{\sim A} = V_{\sim B}$ Measured from V_+ to V_-	$C_{+/-}$	-	8.3	20	pF
Bridge Zero Bias Capacitance	$V_+ - V_- = 0V$ Measured from $V_{\sim A}$ to $V_{+/-}$ and $V_{\sim B}$ to $V_{+/-}$	$C_{\sim A/+}$, $C_{\sim A/-}$, $C_{\sim B/+}$, $C_{\sim B/-}$	-	8.5	12	pF
Thyristor Peak Pulse Discharge Energy	Single Event Over-Voltage Discharge Energy	E_{PP}	-	-	300	mJ
Thyristor Repeated Discharge Energy	Allowable Repeated Discharge Energy, Rectified 60Hz	E_{AVE}	-	-	14	mJ

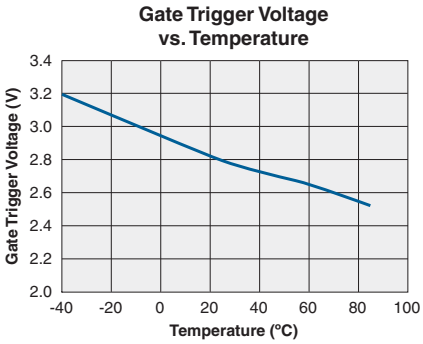
2 Typical Performance Data











3 Manufacturing Information

3.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Clare classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC7556N	MSL 1

3.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

3.3 Reflow Profile

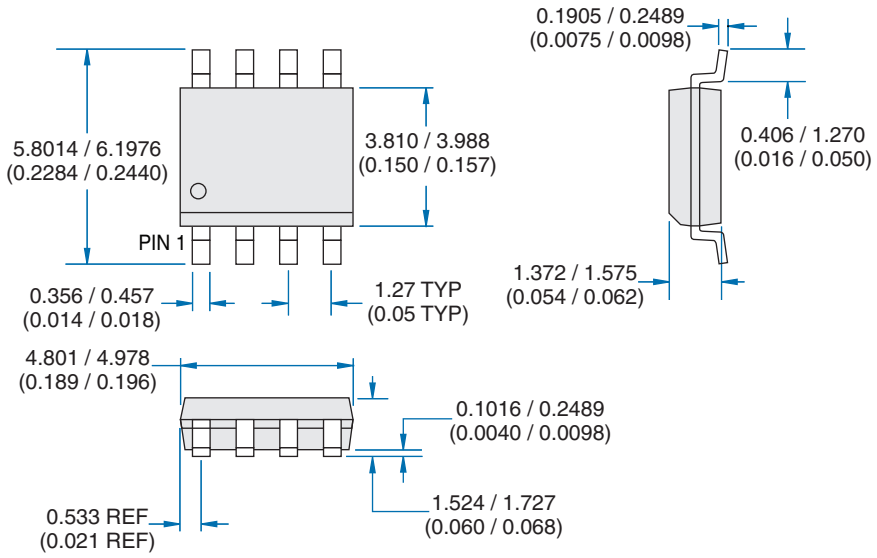
This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
CPC7556N	260°C for 30 seconds

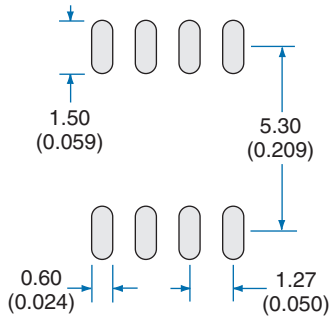
3.4 Board Wash

Clare recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable. The use of a short drying bake may be necessary if a wash is used after solder reflow processes. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

3.5 8-Pin SOIC Package Dimensions

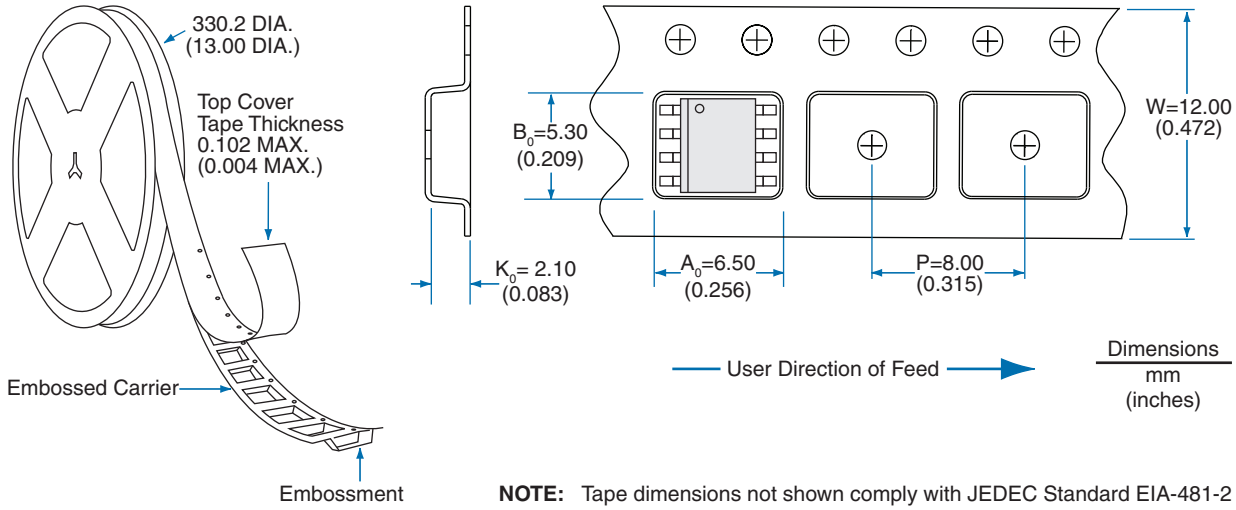


PCB Land Pattern



Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

3.6 Tape & Reel Dimensions



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

For additional information please visit our website at: www.clare.com

Specification: DS-CPC7556 - R02

8/17/2011