VGA PWM Controller with Differential Voltage Feedback

Features

- Adjustable Output Voltage from +0.6V to +3.3V
  - 0.6V Reference Voltage
  - ±0.6% Accuracy Over-Temperature
- Operates from An Input Battery Voltage Range of +1.8V to +28V
- Remote Feedback Sense for Excellent Output Voltage
- REFIN Function for Over-clocking Purpose from 0.5V~2.5V range
- Power-On-Reset Monitoring on VCC pin
- Excellent line and load transient responses
- PFM mode for increased light load efficiency
- Programmable PWM Frequency from 100kHz to 500kHz
- Selectable Forced PWM or automatic PFM/PWM mode
- Built in 30A Output current driving capability
- Integrate MOSFET Drivers
- Integrated Bootstrap Forward P-CH MOSFET
- Adjustable Integrated Soft-Start and Soft-Stop
- Power Good Monitoring
- 70% Under-Voltage Protection
- 125% Over-Voltage Protection
- TQFN3x3-16 Package
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Notebook
- Table PC
- Hand-Held Portable
- AIO PC

General Description

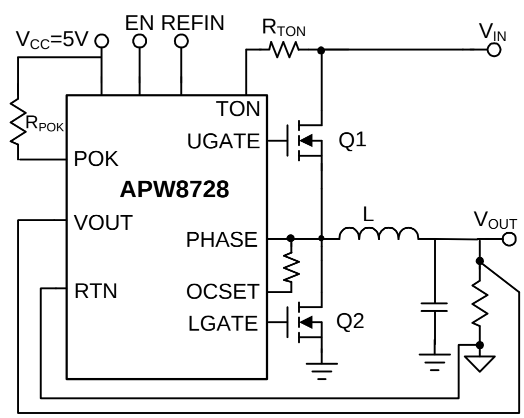
The APW8728 is a single-phase, constant on-time, synchronous PWM controller, which drives N-channel MOSFETs. The APW8728 steps down high voltage to generate low-voltage chipset or RAM supplies in notebook computers.

The APW8728 provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the APW8728 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. In PWM Mode, the converter works nearly at constant frequency for low-noise requirements. APW8728 is built in remote sense function for applications that require remote sense.

The APW8728 is equipped with accurate positive current limit, output under-voltage, and output over-voltage protections, perfect for NB applications. The Power-On-Reset function monitors the voltage on VCC to prevent wrong operation during power-on. The APW8728 has a 1ms digital soft start and built-in an integrated output discharge device for soft stop. An internal integrated soft-start ramps up the output voltage with programmable slew rate to reduce the start-up current. A soft-stop function actively discharges the output capacitors.

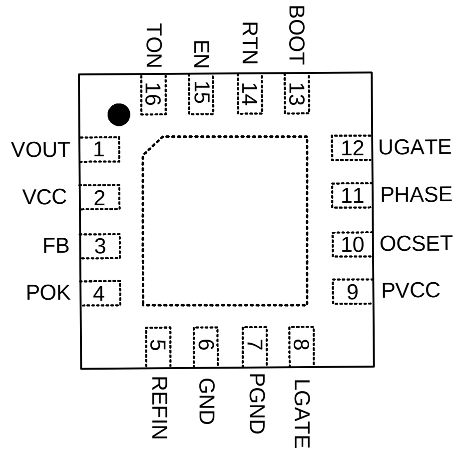
The APW8728 is available in 16pin TQFN3x3-16 package respectively.

Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Pin Configuration



TQFN3x3-16
(TOP VIEW)

Ordering and Marking Information

APW8728 □□-□□□ Assembly Meterial Handling Code Temperature Range Package Code	Package Code QB : TQFN3x3-16 Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Meterial L : Lead Free Device G : Halogen and Lead Free Device
APW8728 QB : APW 8728 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND or PGND)	-0.3 ~ 37	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 7	V
	All Other Pins (VOUT, TON, EN and FB to GND)	-0.3 ~ V_{CC}+0.3	V
	UGATE Voltage (UGATE to PHASE) <20ns Pulse Width >20ns Pulse Width	 -5 ~ V_{BOOT}+1.5 -0.3 ~ V_{BOOT}+0.3	V
	LGATE Voltage (LGATE to GND) <20ns Pulse Width >20ns Pulse Width	 -5 ~ V_{CC}+1.5 -0.3 ~ V_{CC}+0.3	V
V_{PHASE}	PHASE Voltage (PHASE to GND) <20ns Pulse Width >20ns Pulse Width	 -5 ~ 35 -1 ~ 30	V
T_J	Maximum Junction Temperature	150	^oC
T_{STG}	Storage Temperature	-65 ~ 150	^oC
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	^oC

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance-Junction to Ambient (Note2) TQFN3x3-16	40	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Converter Input Voltage	1.8 ~ 28	V
V_{CC}	VCC Supply Voltage	4.5 ~ 5.5	V
V_{OUT}	Converter Output Voltage (external REFIN input)	0.5 ~ 2.5	V
	Converter Output Voltage (internal FB setting)	0.6~ 3.3	V
I_{OUT}	Converter Output Current	0~ 30	A
T_J	Junction Temperature	-40 ~ 125	^oC

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC}=5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8728			Unit
			Min.	Typ.	Max.	
VOUT AND VFB VOLTAGE						
	REFIN Voltage	External REFIN output voltage tolerance, REFIN=1V	-5	-	5	mV
		External REFIN adjustable output range	0.5	-	2.5	V
	Output Voltage	Internal FB adjustable output range	0.6	-	3.3	
V_{REF}	Reference Voltage			0.6		V
	Regulation Accuracy	T_A = 25 °C	-0.4	-	+0.4	%
		T_A = -40 °C ~ 85 °C	-0.6	-	+0.6	%
I_{FB}	FB Input Bias Current	FB=0.5V		0.02	0.1	μA
T_{DIS}	V_{OUT} Discharge Resistance		-	20	32	Ω
SUPPLY CURRENT						
I_{VCC}	VCC Input Bias Current	VCC Current, EN=5V, VFB=0.65V, PHASE=0.5V		600	750	μA
I_{VCC_SHDN}	VCC Shutdown Current	EN=GND, VCC=5V	-	0	7	μA
SWITCHING FREQUENCY AND DUTY AND INTERNAL SOFT START						
T_{ON}	on time	V_{IN}=15V, V_{OUT}=1.25V, R_{TON}=1MΩ	267	334	401	ns
$T_{ON(MIN)}$	Minimum on time		80	110	140	ns
$T_{OFF(MIN)}$	Minimum off time	V_{FB}=0.55V, V_{PHASE}=-0.1V	350	450	550	ns
T_{SS}	Internal Soft Start Time	EN High to V_{OUT} Regulation(95%)	-	1.0	-	ms
GATE DRIVER						
	UG Pull-Up Resistance	BOOT-UG=0.5V	-	1.5	3	Ω
	UG Sink Resistance	UG-PHASE=0.5V	-	0.7	1.8	Ω
	LG Pull-Up Resistance	PVCC-LG=0.5V	-	1.0	2.2	Ω
	LG Sink Resistance	LG-PGND=0.5V	-	0.5	1.2	Ω
	UG to LG Dead time (Note4)	UG falling to LG rising	-	20	-	ns
	LG to UG Dead time (Note4)	LG falling to UG rising	-	20	-	ns
BOOTSTRAP SWITCH						
V_F	Ron	V_{VCC} – $V_{BOOT-GND}$, I_F = 10mA	-	0.3	0.4	V
I_R	Reverse Leakage	$V_{BOOT-GND}$ = 30V, V_{PHASE} = 25V, V_{VCC} = 5V	-	-	0.5	μA
VCC POR THRESHOLD						
V_{VCC_THR}	Rising VCC POR Threshold Voltage		4.25	4.35	4.45	V
	VCC POR Hysteresis		-	100	-	mV
V_{PVCC_THR}	Rising PVCC POR Threshold Voltage		4.25	4.35	4.45	V
	PVCC POR Hysteresis		-	100	-	mV

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Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC}=5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8728			Unit
			Min.	Typ.	Max.	
CONTROL INPUTS						
	REFIN Voltage threshold	Shutdown	-	-	0.4	V
		External Reference, V_{OUT}=V_{REFIN}	0.5	-	2.5	
		Internal Reference, V_{OUT}=FB setting	2.8	3	3.2	
	REFIN Leakage	REFIN=0V	-	0.1	1.0	µA
	REFIN slew rate	Internal rise/fall limit	-	8	-	mV/us
	EN Voltage threshold	Shutdown	-	-	0.4	V
		Hysteresis	-	30	-	mV
		Enable	0.5	-	-	V
POWER-OK INDICATOR						
V_{POK}	POK Threshold	POK in from Lower (POK Goes High)	87	90	93	%
		POK out from normal (POK Goes Low) with 30us noise filter	120	125	130	%
I_{POK}	POK Leakage Current	V_{POK}=5V	-	0.1	1.0	µA
	POK Sink Current	V_{POK}=0.5V	2.5	7.5	-	mA
	POK Enable Delay Time	EN High to POK High	-	1.6	-	ms
CURRENT SENSE						
I_{OCSET}	I_{OCSET} OCP Threshold	I_{OCSET} Sourcing	18	20	22	µA
$T_{CIOCSET}$	I_{OCSET} Temperature Coefficient	On The Basis of 25°C	-	4500	-	ppm/°C
V_{OCSET}	Current Limit Threshold Setting Range	$V_{OCSET-GND}$ Voltage, Over All Temperature	30		300	mV
	Maximum Current Limit Threshold	R_{OCSET} open	-	0.6		V
	Zero Crossing Comparator Offset	$V_{GND-PHASE}$ Voltage	-3	0	3	mV
	Over current protection Comparator Offset	($V_{OCSET-PHASE}$-$V_{GND-PHASE}$) Voltage, $V_{OCSET-GND}$=60mV	-10	0	10	mV
PROTECTION						
V_{UV}	UVP Threshold		60	70	80	%
	UVP Debounce Interval		-	16	-	µs
	UVP Enable Delay	EN High to POK High	-	1.6	-	ms

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC}=5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

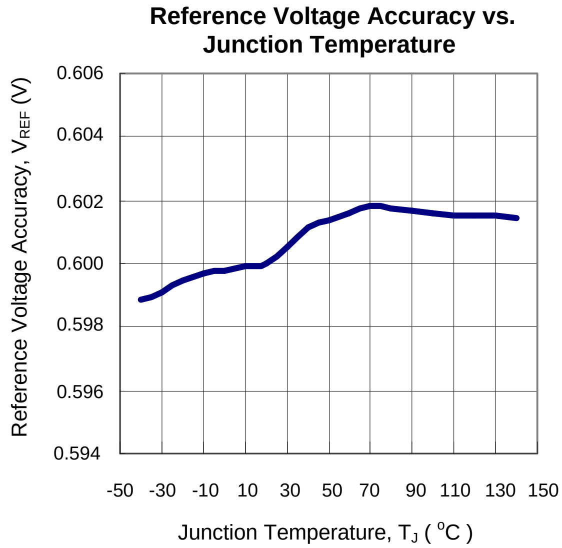
Symbol	Parameter	Test Conditions	APW8728			Unit
			Min.	Typ.	Max.	
PROTECTION						
V_{OVR}	OVP Rising Threshold		120	125	130	%
	OVP Hysteresis		-	5	-	%
	OVP Propagation Delay	V_{FB} Rising	-	2	-	μs
T_{OTR}	OTP Rising Threshold (Note 4)		-	140	-	°C
	OTP Hysteresis (Note 4)		-	25	-	°C
Remote Sense Amplifier						
Bw	Open loop bandwidth (Note4)		-	6	-	MHz
	Open loop gain (Note4)		-	86	-	dB

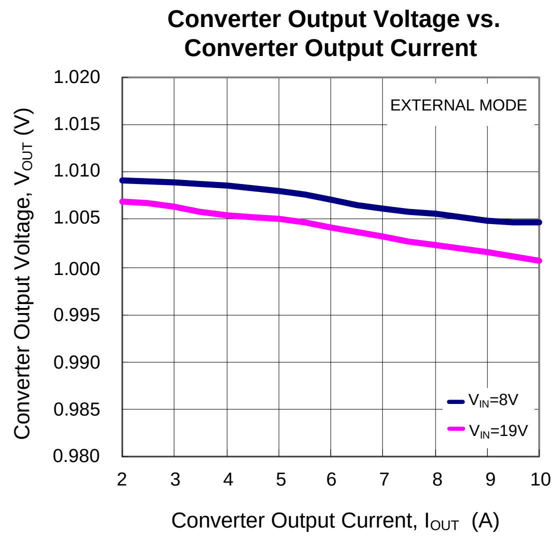
Note4: Guaranteed by design.

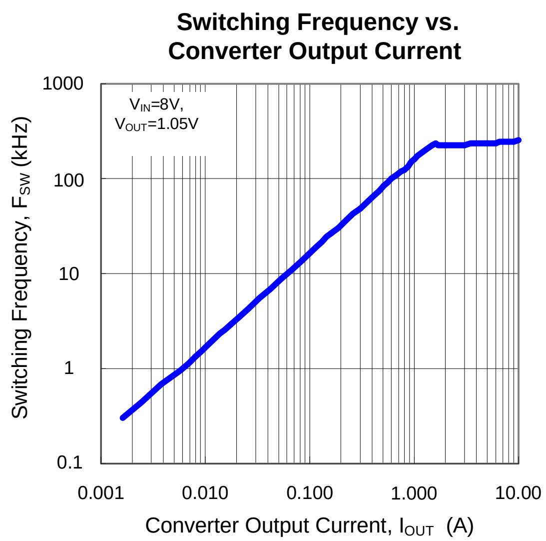
Pin Description

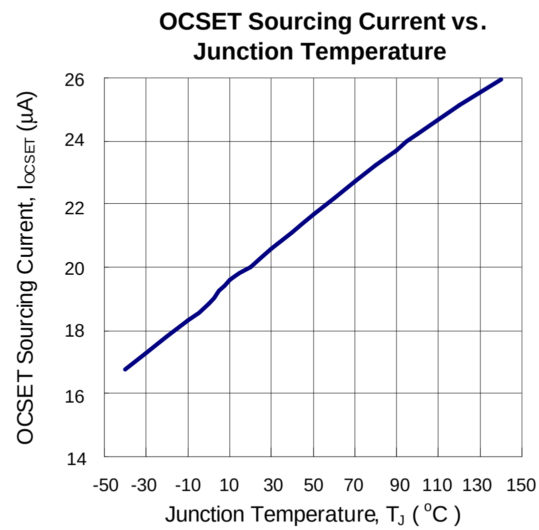
PIN		FUNCTION
NO. TQFN3x3-16	NAME	
1	VOUT	This pin is the positive node of the differential remote voltage sensing. The VOUT pin should be connected to the remote load voltage sense point directly.
2	VCC	Supply Voltage Input Pin for Control Circuitry. Connect +5V from the VCC pin to the GND. Decoupling at least 1μF of a MLCC capacitor from the VCC pin to the GND.
3	FB	Output Voltage Feedback Pin. In internal mode, this pin is connected to the resistive divider that set the desired output voltage. The POK, UVP, and OVP circuits detect this signal to report output voltage status.
4	POK	Power Good Output. POK is an open drain output used to indicate the status of the output voltage. Connect the POK in to +5V through a pull-high resistor.
5	REFIN	Enable/Shutdown Pin or External Reference Selection of The PWM Controller.
6	GND	Signal Ground for The IC
7	PGND	Power Ground of The LG Low-side MOSFET Driver. Connect the pin to the Source of the low-side MOSFET
8	LGATE	Output of The Low-side MOSFET Driver. Connect this pin to Gate of the low-side MOSFET. Swings from PGND to VCC.
9	PVCC	Supply Voltage Input Pin for The LG Low-side MOSFET Gate Driver. Connect +5V from the PVCC pin to the PGND pin. Decoupling at least 1μF of a MLCC capacitor from the PVCC pin to the PGND pin.
10	OCSET	Current-Limit Threshold Setting Pin. There is an internal source current 10μA through a resistor from OCSET pin to PHASE. This pin is used to monitor the voltage drop across the Drain and Source of the low-side MOSFET for current-limit.
11	PHASE	Junction Point of The High-side MOSFET Source, Output Filter Inductor and The Low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. PHASE serves as the lower supply rail for the UG high-side gate driver.
12	UGATE	Output of The High-side MOSFET Driver. Connect this pin to Gate of the high-side MOSFET.
13	BOOT	Supply Input for The UGATE Driver and An Internal Level-shift Circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
14	RTN	This pin is the negative node of the differential remote voltage sensing. The RTN pin should be connected to the remote GND sense point directly.
15	EN	Enable Pin of The PWM Controller. When the EN is above high logic level, the Device is in automatic PFM/PWM Mode. When the EN is below low logic level, the device is in shutdown and only low leakage current is taken from V_{CC} and V_{IN}.
16	TON	This Pin is Allowed to Adjust The Switching Frequency. Connect a resistor R_{TON}=400kΩ ~ 1500kΩ from TON pin to V_{IN}.

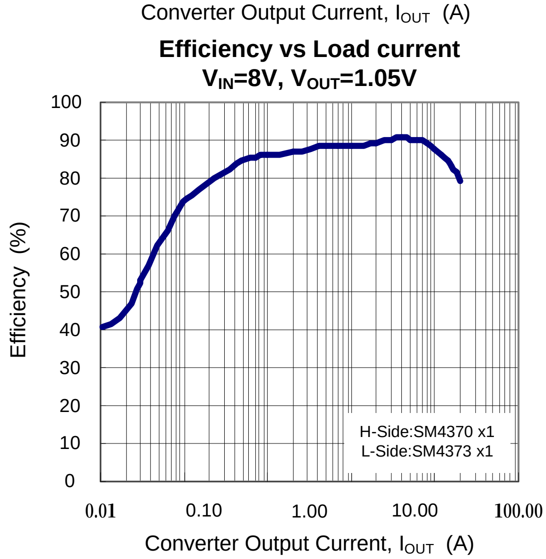
Typical Operating Characteristics

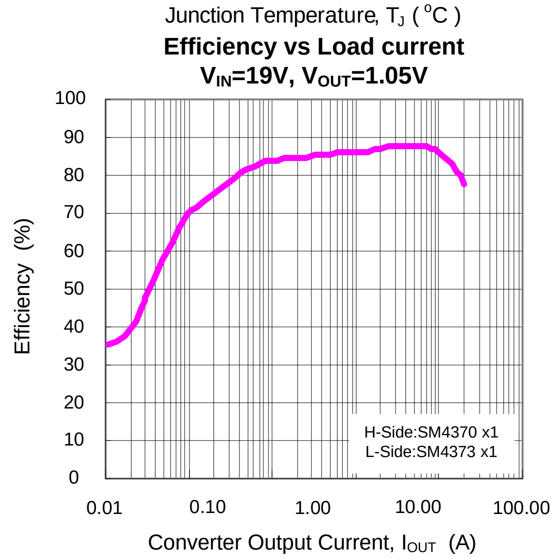












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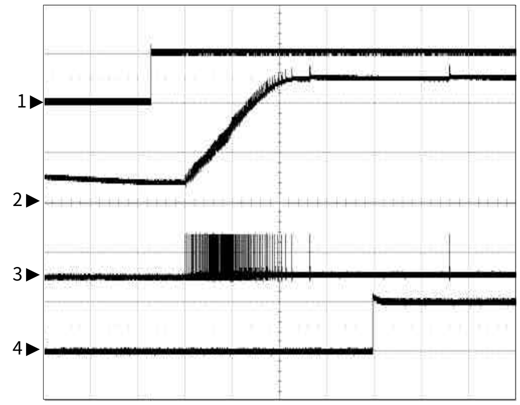
Operating Waveforms

Refer to the typical application circuit. The test condition is V_{IN}=19V, T_A= 25°C unless otherwise specified.

Enable at Zero Initial Voltage of V_{OUT}

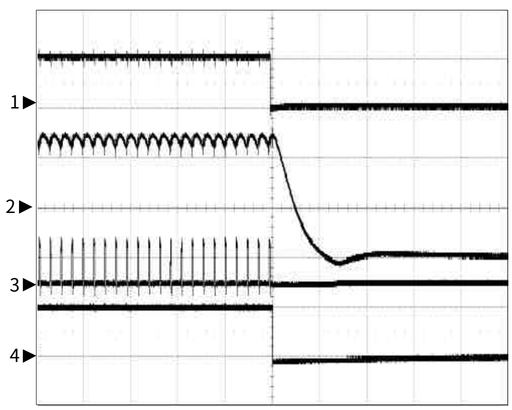
CH1: V_{REFIN}, 5V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{PHASE}, 20V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 500μs/Div

Enable Before End of Soft-Stop



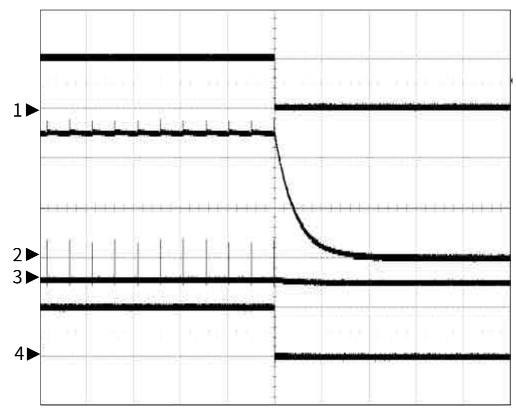
CH1: V_{REFIN}, 5V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{PHASE}, 20V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 500μs/Div

Shutdown at I_{OUT}=20A



CH1: V_{REFIN}, 5V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{PHASE}, 20V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 20μs/Div

Shutdown with Soft-Stop at No Load

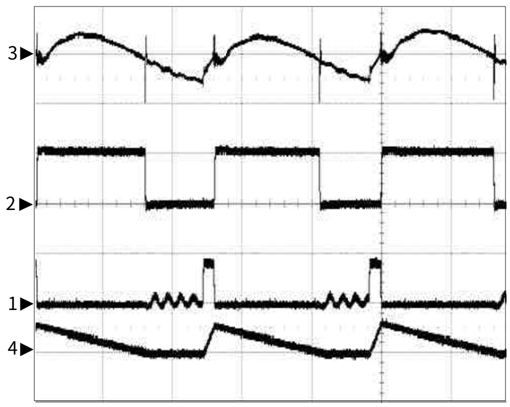


CH1: V_{REFIN}, 5V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{PHASE}, 20V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 10ms/Div

Operating Waveforms

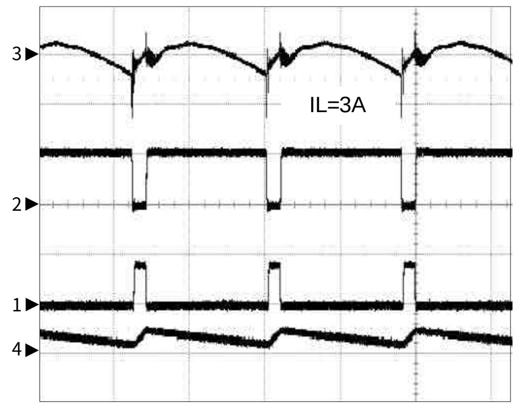
Refer to the typical application circuit. The test condition is V_{IN}=19V, T_A= 25°C unless otherwise specified.

Operating at PFM Mode



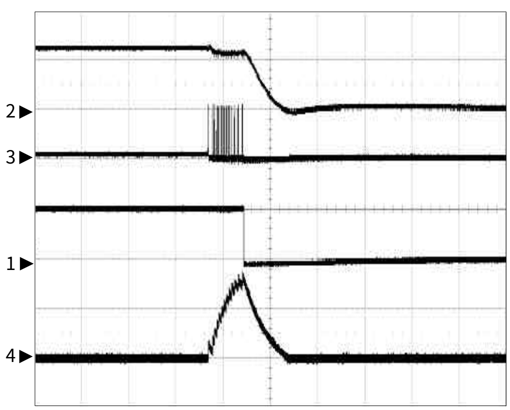
CH1: V_{PHASE}, 20V/Div, DC
CH2: V_{LGATE}, 5V/Div, DC
CH3: V_{OUT}, 100mV/Div, AC
CH4: IL, 10A/Div, DC
TIME: 2 μs/Div

Operating at PWM Mode



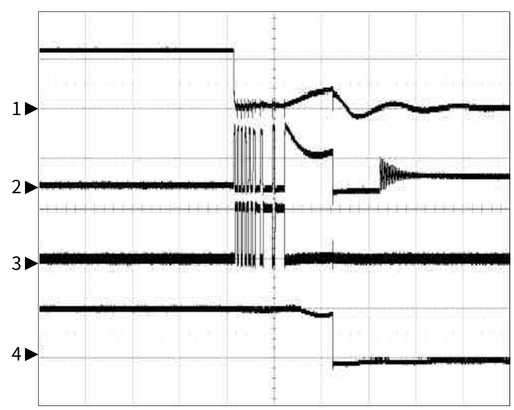
CH1: V_{PHASE}, 20V/Div, DC
CH2: V_{LGATE}, 5V/Div, DC
CH3: V_{OUT}, 100mV/Div, AC
CH4: IL, 10A/Div, DC
TIME: 2 μs/Div

Over-Current Protection



CH1: V_{POK}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{PHASE}, 20V/Div, DC
CH4: I_L, 20A/Div, DC
TIME: 20 μs/Div

Under-Voltage Protection

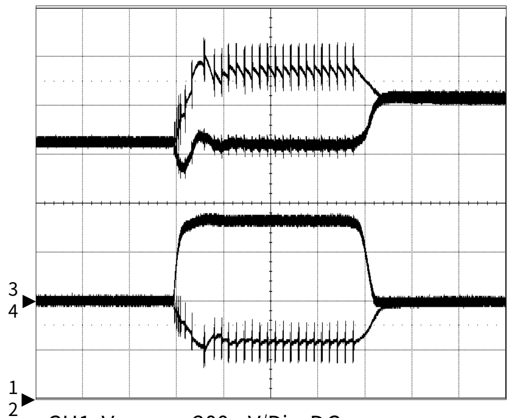


CH1: V_{FB}, 500mV/Div, DC
CH2: V_{UGATE}, 20V/Div, DC
CH3: V_{LGATE}, 10V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 10 μs/Div

Operating Waveforms

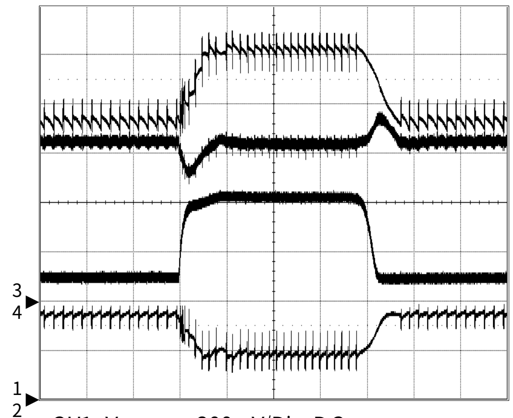
Refer to the typical application circuit. The test condition is V_{IN}=19V, T_A= 25°C unless otherwise specified.

Load Transient
0A->17.5A->0A
When Total Impedance of Line = 20mOhm



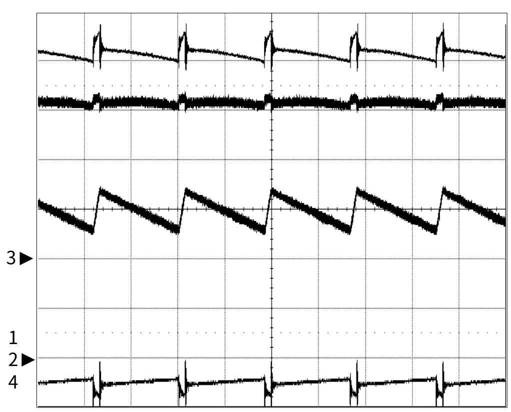
CH1: V_{OUT_near}, 200mV/Div, DC
CH2: V_{OUT_remote}, 200mV/Div, DC
CH3: I_{OUT}, 10A/Div, DC
CH4: $V_{GND\_near-remote}$, 200mV/Div, DC
TIME: 20μs/Div

Load Transient
5A->20A->5A
When Total Impedance of Line = 20mOhm



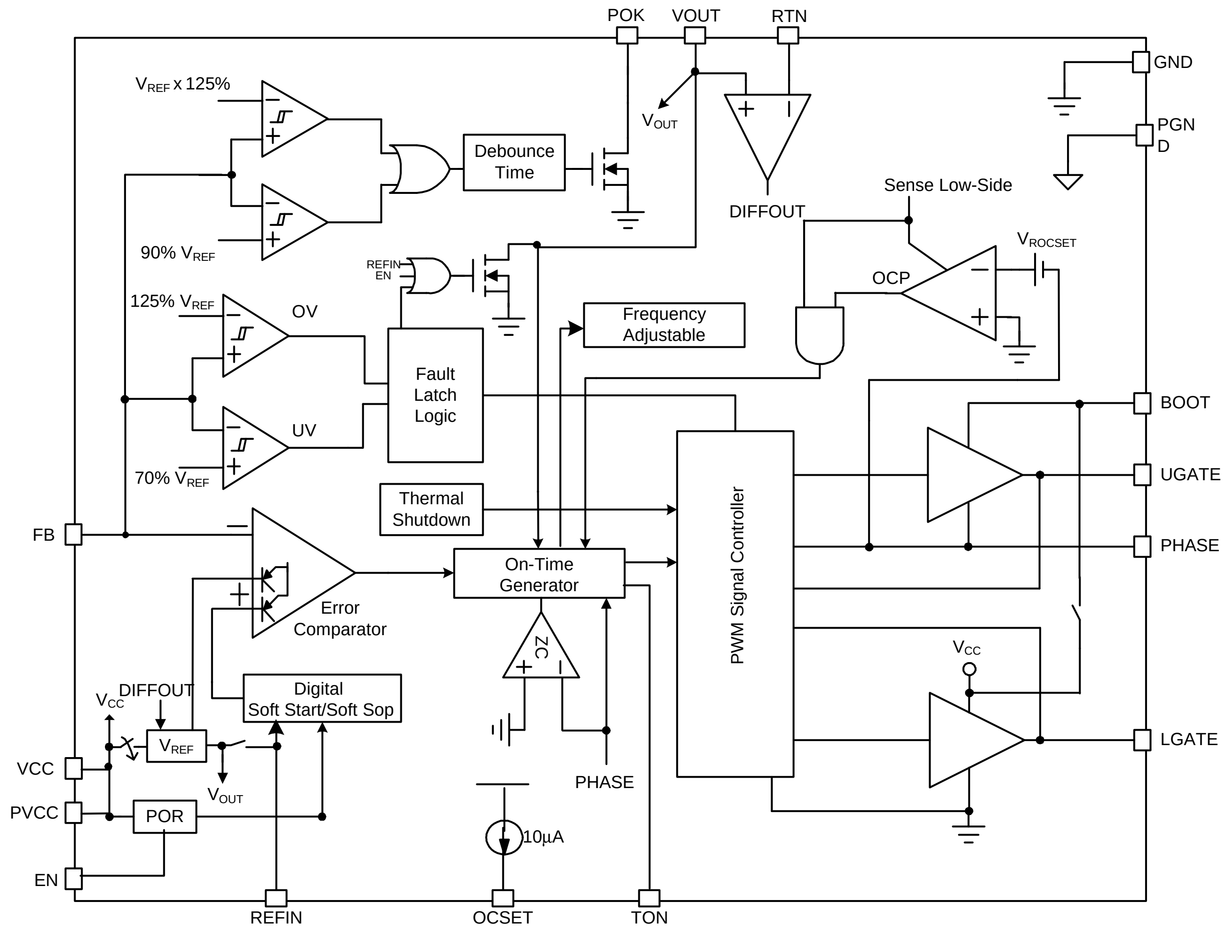
CH1: V_{OUT_near}, 200mV/Div, DC
CH2: V_{OUT_remote}, 200mV/Div, DC
CH3: I_{OUT}, 10A/Div, DC
CH4: $V_{GND\_near-remote}$, 200mV/Div, DC
TIME: 20 μs/Div

Remote Sense
When Total Impedance of Line = 20mOhm



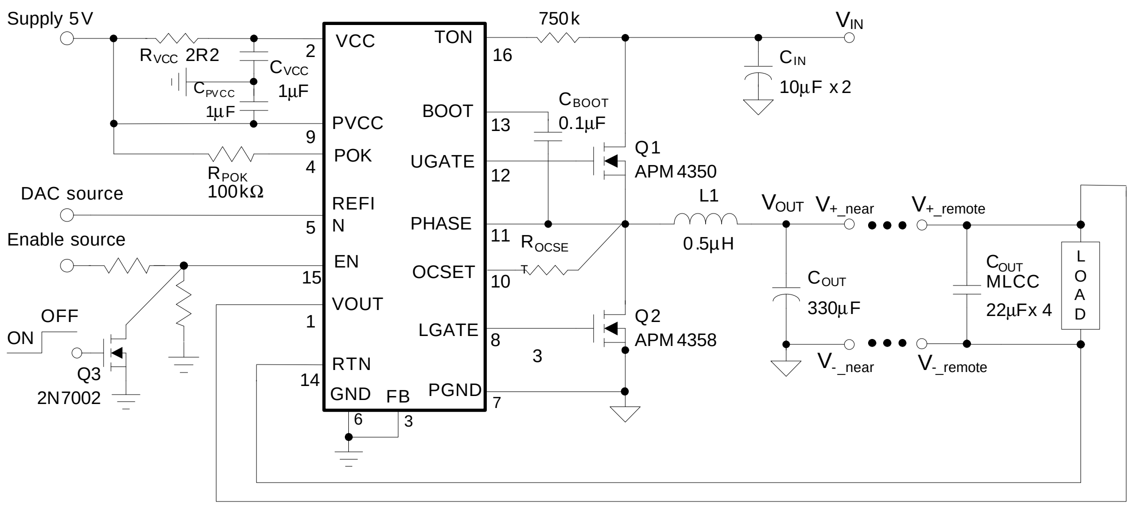
CH1: V_{OUT_near}, 200mV/Div, DC
CH2: V_{OUT_remote}, 200mV/Div, DC
CH3: I_L, 10A/Div, DC
CH4: $V_{GND\_near-remote}$, 200mV/Div, DC
TIME: 2 μs/Div

Block Diagram



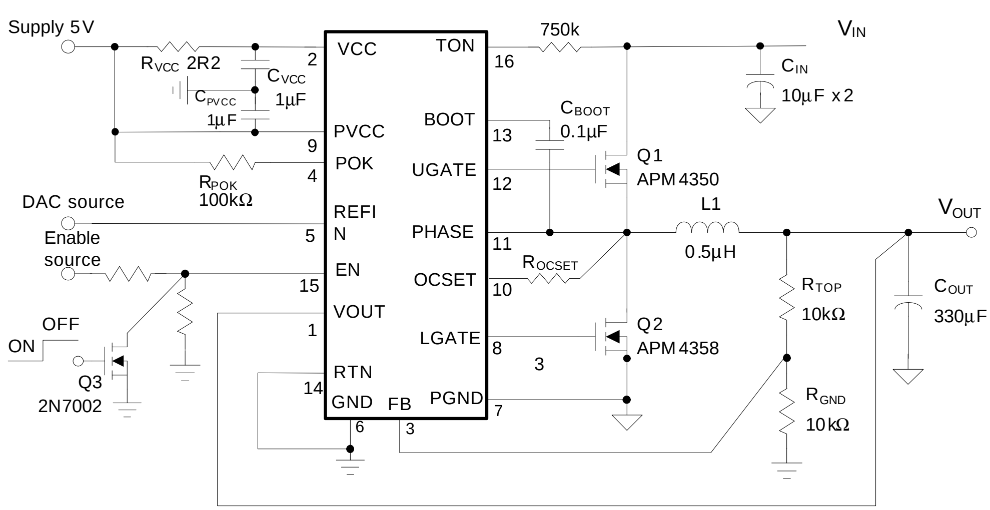
Typical Application Circuit

FOR External Mode Application



APW8728 (TQFN3x3-16)

FOR Internal Mode Application



APW8728 (TQFN3X3-16)

Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time is controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to the input voltage and directly proportional to the output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block.

The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant-on-time controller, which has large switching frequency variation over input voltage, output current, and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on TON pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 450ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Pulse-Frequency Modulation (PFM)

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{ON-PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the nominal switching frequency of the converter in PWM mode.

The load current at handoff from PFM to PWM mode is given by:

$$I_{LOAD(PFMtoPWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON-PFM} = \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Power-On-Reset (POR)

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.35V, typical), the POR signal goes high and the chip initiates soft-start operations. When this voltage drops lower than 4.25V (typical), the POR disables the chip.

REFIN Pin Control

The voltage (V_{REFIN}) applied to REFIN pin selects either enable-shutdown or adjustable external reference. When V_{REFIN} is above the EN high threshold (2.8V, typical), the PWM is enabled. When V_{REFIN} is from 0.5V to 2.5V, the output voltage can be programmed as same as V_{REFIN} voltage. When V_{REFIN} is below the EN low threshold, the chip is in the shutdown and only low leakage current is taken from VCC. Once APW8728 has been operating at internal mode, it is unable to transform into external mode. On the other hand, it is able to transform into internal mode. The slew rate of V_{REFIN} must be faster than 0.5V/µs to avoid wrong output voltage.

Function Description (Cont.)

EN Pin Control

When V_{EN} is above the EN high threshold (0.5V, minimum), the converter is enabled in automatic PFM/PWM operation mode. When V_{EN} is below the EN low threshold (0.4V, maximum), the chip is in the shutdown and only low leakage current is taken from VCC.

Digital Soft-Start

The APW8728 integrates digital soft-start circuits to ramp up the output voltage of the converter to the programmed regulation setpoint at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process. The figure 1 shows soft-start sequence. When the EN pin is pulled above the rising EN threshold voltage, the device initiates a soft-start process to ramp up the output voltage. The soft-start interval is 1ms (typical) and independent of the UGATE switching frequency.

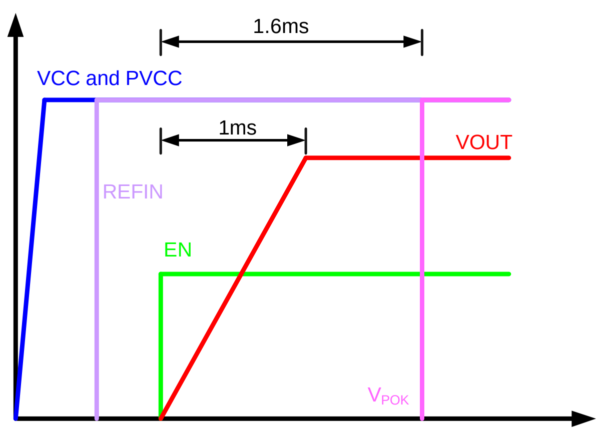


Figure 1. Soft-Start Sequence

During soft-start stage before the POK pin is ready, the under-voltage protection is prohibited. The over-voltage and current-limit protection functions are enabled. If the output capacitor has residue voltage before start-up, both low-side and high-side MOSFETs are in off-state until the internal digital soft-start voltage equals to the V_{FB} voltage. This will ensure that the output voltage starts from its existing voltage level.

In the event of under-voltage, over-voltage, over-temperature, or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the output voltages to the PGND through an internal 20Ω switch.

Power OK Indicator

The APW8728 features an open-drain POK pin to indicate output regulation status. In normal operation, when the output voltage rises 90% of its target value, the POK goes high after 63µs internal delay. When the output voltage outruns 70% or 125% of the target voltage, POK signal will be pulled low immediately.

Since the FB pin is used for both feedback and monitoring purposes, the output voltage deviation can be coupled directly to the FB pin by the capacitor in parallel with the voltage divider as shown in the typical applications. In order to prevent false POK from dropping, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current-limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage protection circuit continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the under-voltage threshold is 70% of the nominal output voltage, the internal UVP delay counter starts to count. After 16µs debounce time, the device turns off both high-side and low-side MOSEFET with latched and starts a soft-stop process to shut down the output gradually. Toggling enable pin to low or recycling PVCC or VCC, will clear the latch and bring the chip back to operation.

Over-Voltage Protection (OVP)

The over-voltage protection monitors the FB voltage to prevent the output from over-voltage condition. When the output voltage rises above 125% of the nominal output voltage, the APW8728 turns off the high-side MOSFET and turns on the low-side MOSFET until the output voltage falls below the falling OVP threshold.

Function Description (Cont.)

Current-Limit

The current-limit circuit employs a "valley" current-sensing algorithm (See Figure 2). The APW8728 uses the low-side MOSFET's $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at PHASE pin is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equals to the inductor ripple 4 current. Therefore, the exact current-limit characteristic and maximum load capability are the functions of the sense resistance, inductor value, and input voltage.

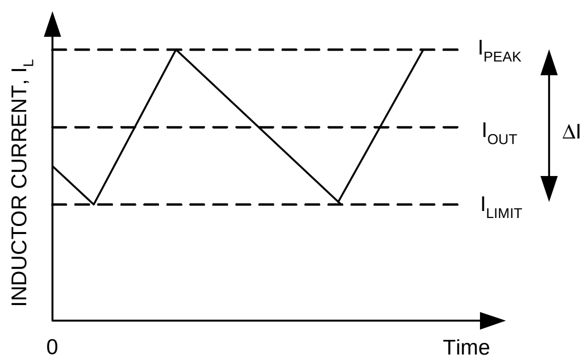


Figure 2. Current-Limit Algorithm

The PWM controller uses the low-side MOSFETs on-resistance $R_{DS(ON)}$ to monitor the current for protection against shortened outputs. The MOSFET's $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacture's datasheet.

When LG is turned on, the OCSET pin can source 20µA through an external resistor for adjusting current-limit threshold. The voltage at OCSET pin is equal to V_{PHASE}+20µA x R_{OCSET}. The relationship between the sampled voltage V_{OCSET} and the current-limit threshold I_{LIMIT} is given by:

$$20\mu A \times R_{OCSET} = I_{LIMIT} \times R_{DS(ON)}$$

Where R_{OCSET} is the resistor of current-limit setting threshold. $R_{DS(ON)}$ is the low side MOSFETs conducive resistance. I_{LIMIT} is the setting current-limit threshold. I_{LIMIT} can be expressed as I_{OUT} minus half of peak-to-peak inductor current.

The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at PHASE. Place the hottest power MOSEFTs as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.

Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature T_{OTR}, the IC will enter the over-temperature protection state that suspends the PWM, which forces the UGATE and LGATE gate drivers output low. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 25°C. The OTP is designed with a 25°C hysteresis to lower the average T_J during continuous thermal overload conditions, which increases lifetime of the APW8728.

Programming the On-Time Control and PWM Switching Frequency

The APW828 does not use a clock signal to produce PWM. The device uses the constant-on-time control architecture to produce pseudo-fixed frequency with input voltage feed-forward. The on-time pulse width is proportional to output voltage V_{OUT} and inverses proportional to input voltage V_{IN}. In PWM, the on-time calculation is written as below :

$$T_{ON} = 4 \times 10^{-12} \times R_{TON} \left[\frac{V_{OUT}}{V_{IN}} \right]$$

Where:

R_{TON} is the resistor connected from TON pin to PHASE pin. Furthermore, the approximate PWM switching frequency is written as :

Function Description (Cont.)

Programming the On-Time Control and PWM Switching Frequency (Cont.)

$$T_{ON} = \frac{D}{F_{SW}} \Rightarrow F_{SW} = \frac{V_{OUT}/V_{IN}}{T_{ON}}$$

Where:

F_{SW} is the PWM switching frequency.

APW8728 doesn't have VIN pin to calculate on-time pulse width. Therefore, monitoring V_{TON} voltage as input voltage to calculate on-time. And then, use the relationship between ontime and duty cycle to obtain the switching frequency. The curve below is the relationship between R_{TON} and the switching frequency F_{SW}.

Romote Sense

APW8728 has a RTN pin for external mode applications that require remote sense. In some applications where high current, low voltage and accurate output voltage regulation are needed, RTN can sense the negative terminal of remote load capacitor directly, and improve output voltage drop which is due to the board interconnection loss.

Application Information

Output Voltage Setting

The output voltage is adjustable from 0.6V to 3.3V with a resistor-divider connected with FB, GND, and converter's output. The voltage (V_{REFIN}) applied to REFIN pin selects adjustable external reference from 0.5V to 2.5V. Using 1% or better resistors for the resistor-divider is recommended. The output voltage is determined by:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{GND}}\right)$$

Where 0.6 is the reference voltage, R_{TOP} is the resistor connected from converter's output to FB, and R_{GND} is the resistor connected from FB to GND. Suggested R_{GND} is in the range from 1k to 20kΩ. To prevent stray pickup, locate resistors R_{TOP} and R_{GND} close to APW8728. Similarly, when V_{REFIN} is from 0.5V to 2.5V, the output voltage can be programmed as same as V_{REFIN} voltage.

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current, I_{RIPPLE}, and affects the load transient reponse. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor which is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage. Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors which have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak inductor's current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor (1μF) in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered. To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times

Application Information (Cont.)

Input Capacitor Selection (Cont.)

higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power-up, the input capacitors have to handle great amount of surge current. For low-duty notebook appliactions, ceramic capacitor is recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

MOSFET Selection

The application for a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the $R_{DS(ON)}$ of the MOSFET:

For the low-side MOSFET, before it is turned on, the body diode has been conducting. The low-side MOSFET driver will not charge the miller capacitor of this MOSFET.

In the turning off process of the low-side MOSFET, the load current will shift to the body diode first. The high dv/dt of the phase node voltage will charge the miller capacitor through the low-side MOSFET driver sinking current path. This results in much less switching loss of the low-side MOSFETs. The duty cycle is often very small in high battery voltage applications, and the low-side MOSFET will conduct most of the switching cycle; therefore, when using smaller $R_{DS(ON)}$ of the low-side MOSFET, the converter can reduce power loss. The gate charge for this MOSFET is usually the secondary consideration. The high-side MOSFET does not have this zero voltage switching condition; in addition, it conducts for less time compared to the low-side MOSFET, so the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gate driver loss and switching loss will be minimized.

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reversing transfer capacitance (C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{high\text{-}side} = I_{OUT}{}^2(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$
$$P_{low\text{-}side} = I_{OUT}{}^2(1+TC)(R_{DS(ON)})(1-D)$$

Where

I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_{SW} is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching interval, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is a factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET.

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Besides, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

· Keep the switching nodes (UGATE, LGATE, BOOT, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals.
Therefore, keep traces to these nodes as short as

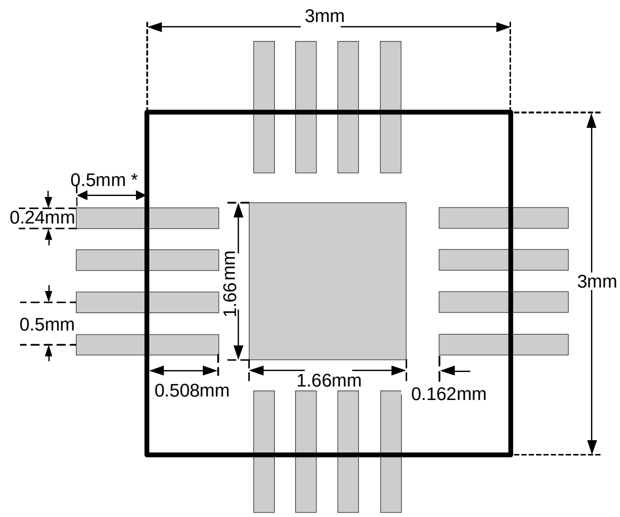
Application Information (Cont.)

Layout Consideration (Cont.)

possible and there should be no other weak signal traces in parallel with theses traces on any layer.

- The signals going through theses traces have both high dv/dt and high di/dt with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATE and LGATE) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (V_{IN} and PHASE nodes) can get better heat sinking.
- The PGND is the current sensing circuit reference ground and also the power ground of the LGATE low-side MOSFET. On the other hand, the PGND trace should be a separate trace and independently go to the source of the low-side MOSFET. Besides, the current sense resistor should be close to OCSET pin to avoid parasitic capacitor effect and noise coupling.
- Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible.)
- The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.
- Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces (UGATE, LGATE, BOOT, and PHASE).

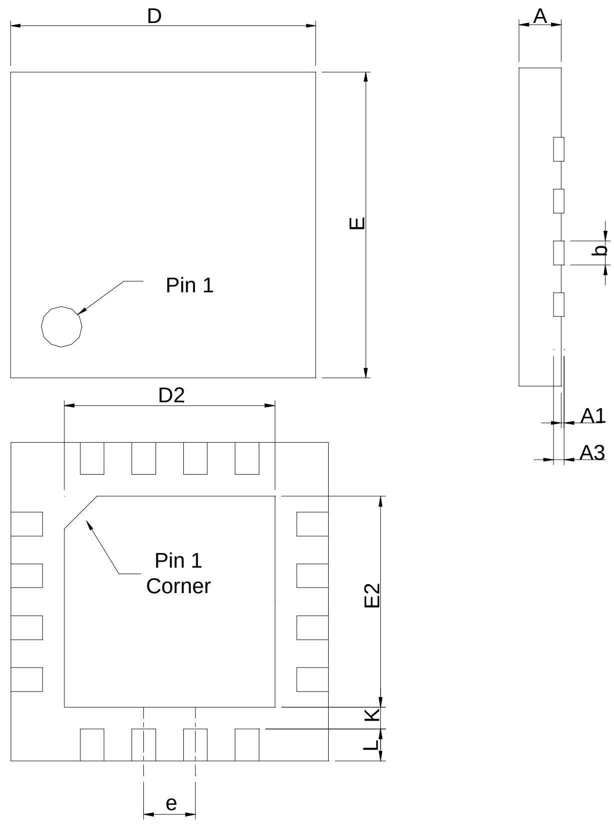
Recommended Minimum Footprint



* Just Recommend

Package Information

TQFN3x3-16



SYMBOL	TQFN3x3-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : Follow JEDEC MO-220 WEED-4.

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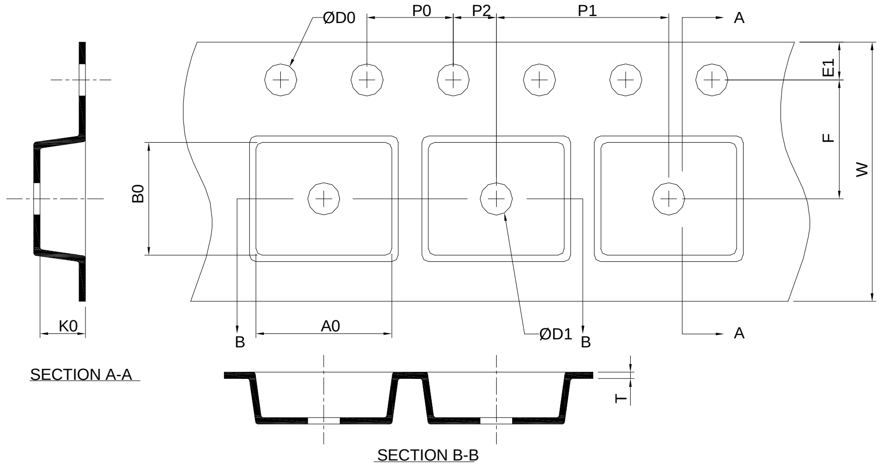
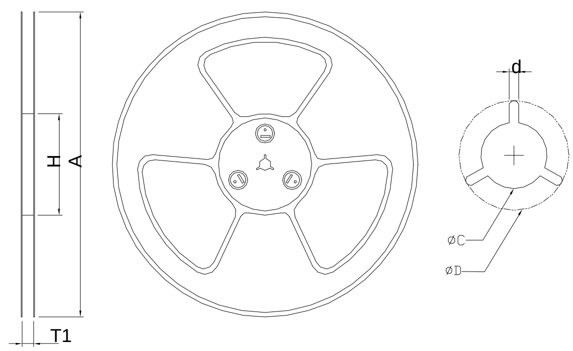
Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
TQFN3x3-16	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

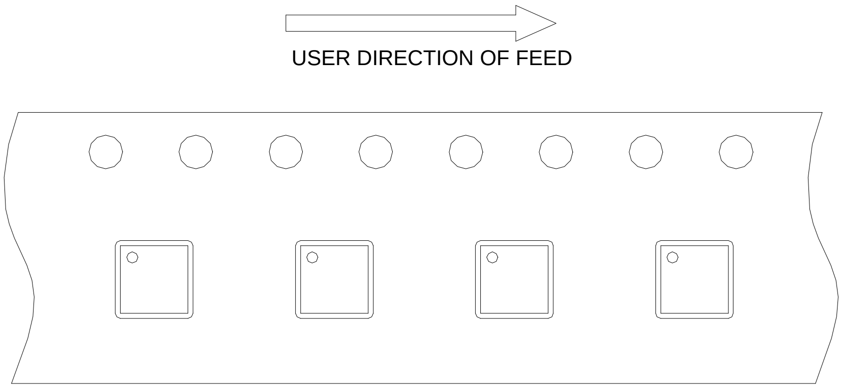
(mm)

Devices Per Unit

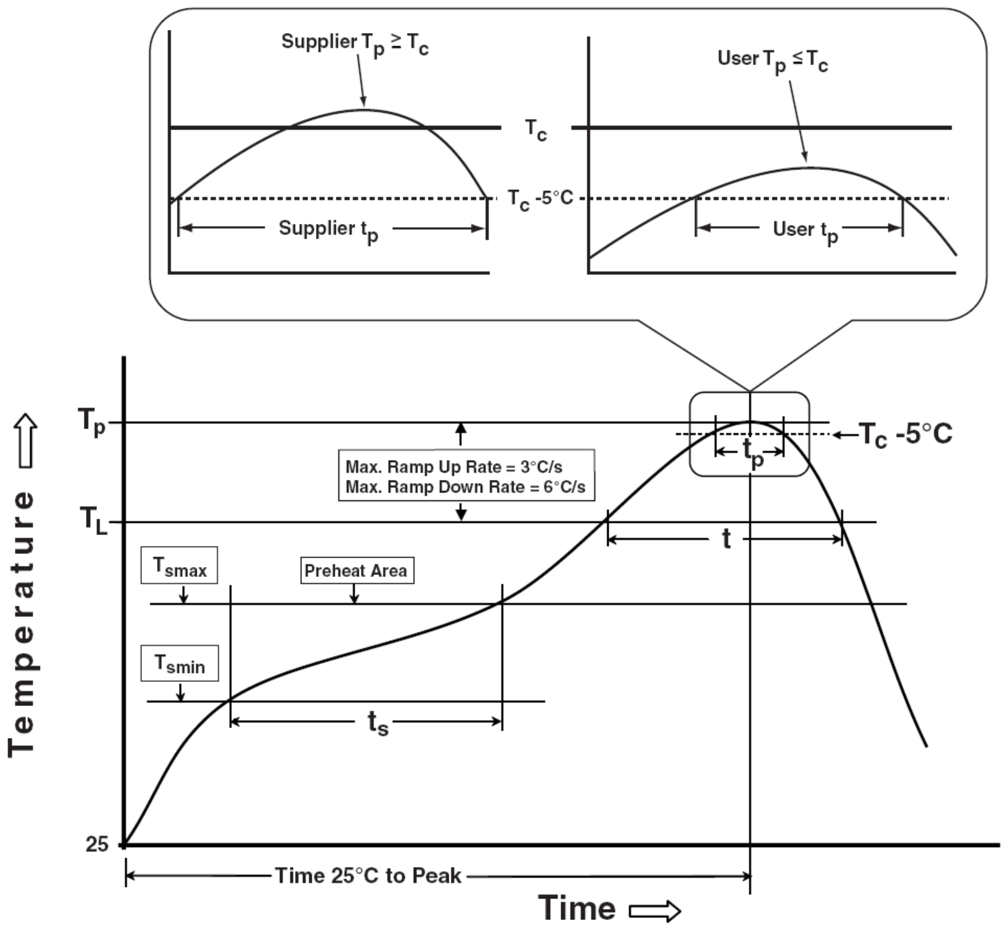
Package Type	Unit	Quantity
TQFN3x3-16	Tape & Reel	3000

Taping Direction Information

TQFN3x3-16



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ^{3}350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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