PRELIMINARY DATA SHEET 5-8-85

SFT1001 AND SFT1003
100 AMP
HIGH SPEED PNP TRANSISTOR
250 VOLTS

SSDI
14830 Valley View Avenue
La Mirada, California 90638
(213) 921-9660
TWX 910-583-4807
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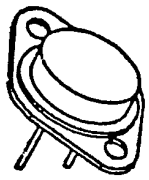
CASE STYLE R
TO—3 WITH .060 PINS



FEATURES

- RADIATION TOLERANT
- FAST SWITCHING
- HIGH FREQUENCY, 80 MHZ TYPICAL
- BVCEO 150 VOLTS MIN.
- HIGH LINEAR GAIN
- LOW LEAKAGE AND SATURATION VOLTAGE
- 200°C OPERATING, GOLD EUTECTIC DIE ATTACH
- DESIGNED FOR COMPLEMENTARY USE WITH SFT1002 AND SFT1004

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector - Emitter Voltage	V_{CEO}	150	Volts
Collector - Base Voltage	V_{CBO}	200	Volts
Emitter - Base Voltage	V_{EBO}	10	Volts
Collector Current	I_C	100	Amps
Base Current	I_B	20	Amps
Total Device Dissipation @ TC = 25 °C Derate above 25 °C	P_D	200 1.14	Watts W/°C
Operating and Storage Temperature	Tj, Tstg	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance, Junction to Case	RθJC	0.875	°C.W

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min.	Max.	Unit
Collector - Emitter Breakdown Voltage* (I_C = 10 m Adc)	BV_{CEO}*	150		Vdc
Collector - Base Breakdown Voltage (I_C = 200 u Adc)	BV_{CBO}	200		Vdc
Emitter - Base Breakdown Voltage (I_E = 200 u Adc)	BV_{EBO}	10		Vdc

NOTE: All specifications subject to change without notice.

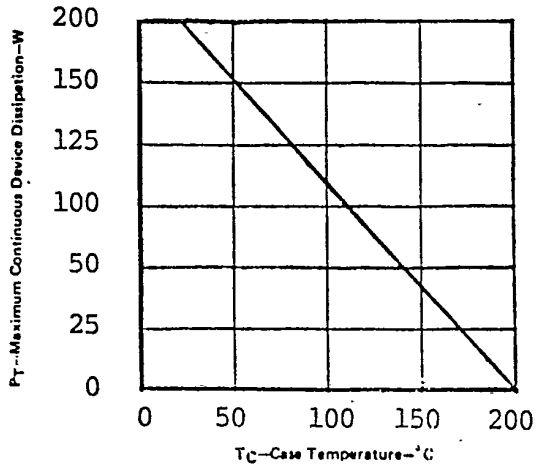
ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min.	Max.	Unit
Collector Cutoff Current (V_{CE} = 120 V)	I_{CEO}		10	uAdc
Collector Cutoff Current (V_{CB} = 150 V)	I_{CBO}		10	uAdc
Emitter Cutoff Current (V_{EB} = 10 V)	I_{EBO}		500	nAdc
DC Current Gain* (I_C = 50 Adc, V_{CE} = 5 Vdc) SFT1001 / SFT1003	h_{FE}*	10 / 25		
(I_C = 100 Adc, V_{CE} = 5 Vdc) SFT1001 / SFT1003		5 / 15		
Collector - Emitter Saturation Voltage* (I_C = 50 Adc, I_B = 5 Adc)	$V_{CE(SAT)}$*		0.7	Vdc
(I_C = 100 Adc, I_B = 10 Adc)			1.5	
Base - Emitter Saturation Voltage* (I_C = 50 Adc, I_B = 5 Adc)	$V_{BE(SAT)}$*		1.5	Vdc
(I_C = 100 Adc, I_B = 10 Adc)			2.5	
Current - Gain - Bandwith Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 10 MHz)	f_T	50		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{ob}		900	pf
Input Capacitance (V_{BE} = 10 Vdc, I_C = 0, f = 1 MHz)	C_{ib}		2500	pf
Delay Time	t_d		100	ns
Rise Time (V_{CC} = 100 Vdc, I_C = 20 Adc, $I_{B1} = I_{B2}$ = 2 Adc)	t_r		300	ns
Storage Time	t_s*		1.5	us
Fall Time	t_f		300	ns

*Pulse Test: Pulse width = 300 us, DutyCycle = 2%

TYPICAL OPERATING CURVES

DISSIPATION DERATING CURVE



SOLID STATE DEVICES, INC.

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SOLID STATE DEVICES, I

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T-91-01

RECTIFIER AND TRANSISTOR CHIPS

The "Chip Family"
Reprinted May 1, 1988

SSDI is a "vertically integrated" company. This means we manufacture our power semiconductor devices from silicon wafers, through wafer processing, package assembly, 100% hi-rel screening, and Groups A, B, and C testing. Many of our chips (die) are consumed internally, however, the demand for power devices in chip form has increased substantially. More and more of our Customers are building or buying power hybrids in lieu of discrete components. Therefore, SSDI offers our most popular products in chip form to be used in power hybrids.

SSDI standard criteria in supplying chips is per MIL-STD-883, method 5008, level "B". Also available at extra cost is level "S" (Space), and method 5007 Wafer Lot Acceptance Test. SSDI has supplied the principle rectifier chip used in the navigation system of Peacekeeper to level "S" for over 10 years.

SSDI performs the following minimum flow requirements for <u>every</u> customer chip order:

1. 100% electrical probe critical 25°C parameters (up to 10 Amps or 2000 Volts, except VF, VCE, and VBE: these are tested on the packaged samples up to 200 Amps).

2. 100% Visual inspection using a metallurgical (light through the lens) microscope at typically 100X, per MIL-STD-750, method 2072, 2073, and/or 2074.

3. Element evaluation (also known as Lot Acceptance Testing, L.A.T.) on packaged samples, LTPD = 10. Read and record critical parameters, decap and perform destructive bond pull on 10 bonds, record readings. The read and record/ bond pull data is sent to the customer, the samples are filed at SSDI.

4. Chips are packaged in conductive antistatic "waffle pack" carriers (from 10-400 per carrier), labeled with the part number, L.A.T. date code, diffusion run#, purchase order number, etc., then sealed in nitrogen filled antistatic bags. The bags are then labeled again and receive an ESD sticker per DOD-STD-1686. Chips can be "oriented" for automatic "pick and place" if specified on the customer purchase order.

All chips have heavy aluminum top metallization for gold or aluminum wire bonding. Depending on the geometry, die are gold or bare silicon backed. SSDI can supply chips with gold/eutectic die attach on the following: molybdenum (moly) pad, kovar pad, beryllium oxide (BeO) pad, leadless chip carrier (LCC or LLCC), flat pack, or cerdip, for applications requiring low temperature solder or epoxy attach.

The procedure to obtain information on a particular chip is as follows:

1. Contact our Marketing department and request the part number required (do not request the geometry number). This could be a "1N" (rectifier) or "2N" (transistor) number, a data sheet number, a competitor's number, or a source/specification control drawing (new specifications should be submitted for review by our technical staff).

2. The marketing coordinator will advise the mask/geometry number which corresponds to the requested part number. A drawing of the topography can be mailed per your request.

3. Samples are normally available for your evaluation, and our Marketing department will be pleased to submit a quotation if required.

The following list of geometries represents our most popular devices only. In most cases the chips are in stock, ready for the element evaluation described above, which requires approximately 4-16 weeks (depending on the geometry and whether it is a new or existing part number). Should you require a chip which is not listed, consult our Marketing department. SSDI is continuously developing new geometries and is interested in designing new chips for your custom requirements.

T-01-05
T-03-05

Geometry	Popular Part Numbers	trr (typ.)	IO (Amps)	VR* (Volts)	Size** (Inches)	RAD*** tested
RECTIFIERS, STANDARD RECOVERY						
G000A	1N4245-49	2usec	1.0	200-1000	.050x.050	n/a
G000C	1N5415-20	2usec	3.0	200-1000	.100x.100	n/a
G000E	1N1199-1206	2usec	10-40	200-1000	.160x.160	n/a
RECTIFIERS, FAST RECOVERY						
G000B	1N4942-46	150nsec	1.0	200-500	.050x.050	n/a
G000D	1N5415-20	150nsec	3-10	200-600	.100x.100	n/a
G000M	1N3889-93					
	1N3909-13	150nsec	20-40	200-600	.160x.160	n/a
RECTIFIERS, ULTRA-FAST RECOVERY						
G0003	SDR1A-G	30nsec	1.0	50-500	.050x.050	yes
G0009	SDR3A-G	30nsec	3.0	50-500	.070x.070	n/a
G000J	1N6079-81	25nsec	6.0	50-200	.080x.080	n/a
G0006	1N5812-16	30nsec	10-20	50-200	.120x.120	yes
G0007	SDR623-625					
	SDR933-935	25nsec	20-30	100-500	.130x.130	n/a
G000M	SDR943-946	70nsec	40	100-600	.160x.160	n/a
G000S	SDR952-955	30nsec	50	100-500	.155x.155	n/a

Geometry	Popular Part Numbers	CJ (pf.)	IO (Amps)	VR* (Volts)	Size** (Inches)	RAD*** tested
RECTIFIERS, SCHOTTKEY						
G000K	SPD5817-19	50	1.0	20-40	.050x.050	yes
G000W	SPD5822A-C	100	3.0	40-80	.060x.060	n/a
G000V	SPD5823-25	800	5-20	20-40	.120x.120	n/a
RECTIFIERS, EPION II ™						
R0010	5R0-15R0/52	15	1.0	50-150	.050x.050	yes
R0011	5R1-15R1/52	35	3.0	50-150	.070x.070	yes
R0014	5R4-15R4/59	150	20	50-150	.120x.120	yes
R0016	5R6-15R6/3D	250	50	50-150	.170x.170	yes
R0018	5R8-15R8/3D	400	100	50-150	.240x.240	yes
R0019	5R9-15R9/3D	500	150	50-150	.320x.320	yes

* Higher voltages available, consult SSDI for assistance
** All chips are .010" thick unless specified. Tolerances +/- .003"
*** yes = Radiation test data on file or available from SSDI to customers with security clearance.
n/a = Not available as of this printing.

SHM15 THROUGH SHM100

100 - 250mA, HIGH VOLTAGE STANDARD RECOVERY RECTIFER
1,500 - 10,000 VOLTS

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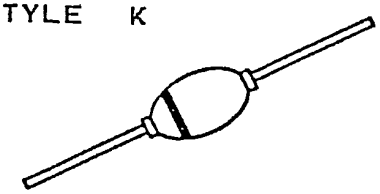
CASE STYLE K



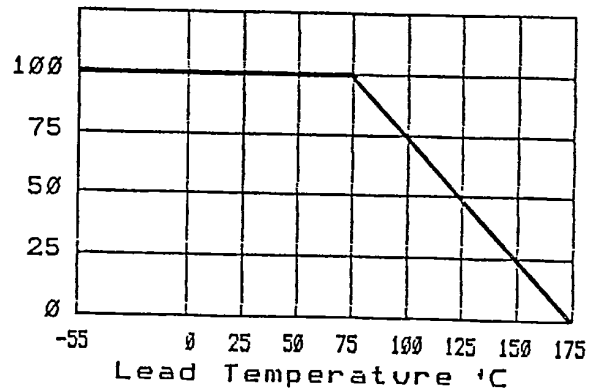
FEATURES
- HEMETICALLY SEALED GLASS PACKAGE
- LOW CAPACITANCE
- 175 °C OPERATING MAXIMUM TEMPERATURE
- HIGHER VOLTAGES AVAILABLE
- METALLURGICALLY BONDED JUNCTIONS
- SUBMINIATURE PACKAGE

PART NUMBER	PEAK INVERSE VOLTAGE PIV	AVERAGE RECTIFIED CURRENT IO		MAXIMUM REVERSE CURRENT @ PIV IR		MAXIMUM FORWARD VOLTAGE @55°C IO VF	MAXIMUM SURGE CURRENT 1 CYCLE IFS	MAXIMUM REVERSE RECOVERY TIME TRR	MAXIMUM JUNCTION CAPACITANCE CJ	TYPICAL THERMAL IMPEDANCE θJ-L
		55°C	100°C	55°C	100°C	25°C	25°C	25°C	@ 100V	L = .25
	VOLTS	mA	mA	µA	µA	VOLTS	AMPS	µsec	pf	°C/W
SHM15	1500	250	185	1.0	25	6	15	5	8	65
SHM20	2000	250	185	1.0	25	6	15	5	8	65
SHM25	2500	250	185	1.0	25	6	15	5	8	65
SHM30	3000	150	110	1.0	25	8	10	5	4	80
SHM40	4000	150	110	1.0	25	8	10	5	4	80
SHM50	5000	150	110	1.0	25	8	10	5	4	80
SHM60	6000	100	75	1.0	25	16	5	5	2	80
SHM80	8000	100	75	1.0	25	16	5	5	2	80
SHM100	10000	100	75	1.0	25	16	5	5	2	80

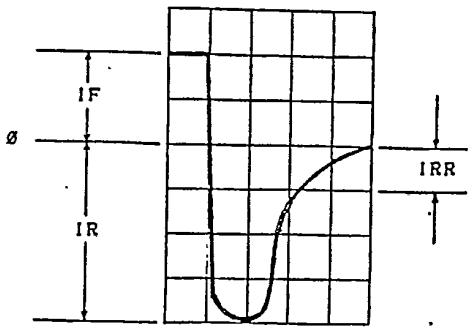
* Reverse recovery test conditions: IF = 50mA, IR = 100mA, IRR = 25mA.

1. Operating and testing over 10,000 V/inch may require encapsulation or immerson in a suitable dielectric material.
2. Maximum forward voltage measured with instantaneous forward pulse of 8.3 mS.
3. Maximum lead temperature for soldering is 250°C, 3/8 inch from case for 5 seconds maximum.
4. Operating and storage tempaerature -65°C to +175°C.

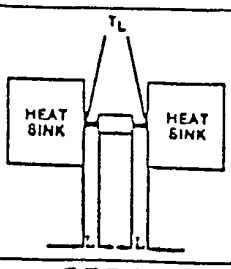
Maximum forward current vs. Lead Temperature



Reverse Recovery Wave Form

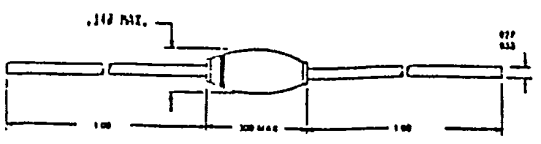


THERMAL IMPEDANCE θJ-L INFORMATION



HEAT SINKS ARE INFINITE
TL = LEAD TEMP. ADJACENT TO HEAT SINK
TJ = TEMP. OF CENTER JUNCTION
EXPOSED PORTION OF LEADS SHALL BE FREE OF PAINT, GREASE OR COATINGS OF ANY KIND.

BODY MATERIAL = GLASS
LEAD MATERIAL = TINNED COPPER



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