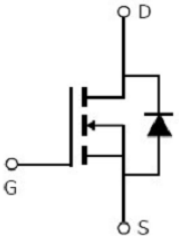
Main Product Characteristics

V_{DSS}	600V
R_{DS}(on)	3.8Ω (typ.)
I_D	2A

TO-252

Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150℃ operating temperature

Description

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V①	2	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V①	1.3	
I_{DM}	Pulsed Drain Current②	8	
P_D @TC = 25°C	Power Dissipation③	42	W
	Linear Derating Factor	0.34	W/°C
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy @ L=53mH	116	mJ
I_{AS}	Avalanche Current @ L=53mH	2.1	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

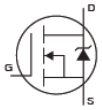
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case③	—	2.95	℃/W
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	—	110	℃/W

Electrical Characteristics @T_A=25℃ unless otherwise specified

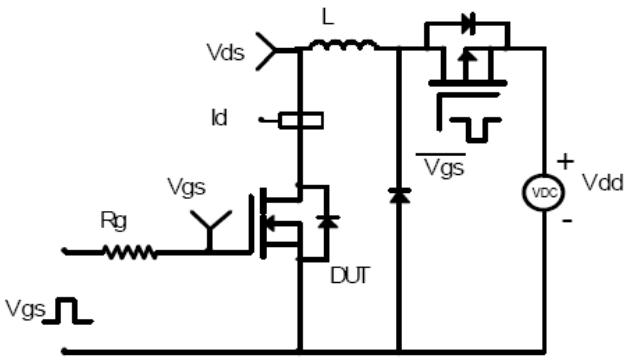
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	600	—	—	V	V_{GS} = 0V, ID = 250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	3.8	4.5	Ω	V_{GS}=10V,I_D = 1.0A
		—	8.2	—		T_J = 125℃
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
		—	2.4	—		T_J = 125℃
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	V_{DS} = 600V,V_{GS} = 0V
		—	—	50		T_J = 125℃
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS} =30V
		—	—	-100		V_{GS} = -30V
Q_g	Total gate charge	—	5.7	—	nC	I_D = 2.0A,
Q_{gs}	Gate-to-Source charge	—	1.7	—		V_{DS}=480V,
Q_{gd}	Gate-to-Drain("Miller") charge	—	2.0	—		V_{GS} = 10V
$t_{d(on)}$	Turn-on delay time	—	9.1	—	ns	V_{GS}=10V, VDS=300V, R_{GEN}=25Ω, ID=2.0A
t_r	Rise time	—	6.3	—		
$t_{d(off)}$	Turn-Off delay time	—	23	—		
t_f	Fall time	—	13	—		
C_{iss}	Input capacitance	—	329	—	pF	V_{GS} = 0V
C_{oss}	Output capacitance	—	32	—		V_{DS} = 25V
C_{rss}	Reverse transfer capacitance	—	4	—		f = 1MHz

Source-Drain Ratings and Characteristics

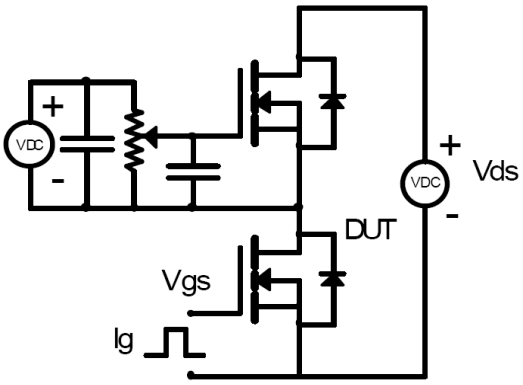
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	8	A	
V_{sd}	Diode Forward Voltage	—	0.84	1.4	V	I_S=1.9A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	—	357	—	ns	T_J = 25°C, I_F =2A, di/dt = 100A/μs
Q_{rr}	Reverse Recovery Charge	—	1030	—	nC	

Test circuits and Waveforms

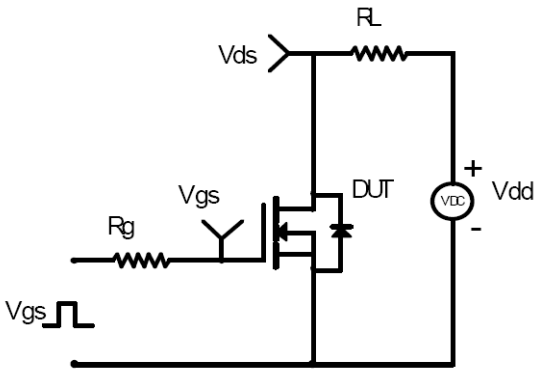
EAS Test Circuit



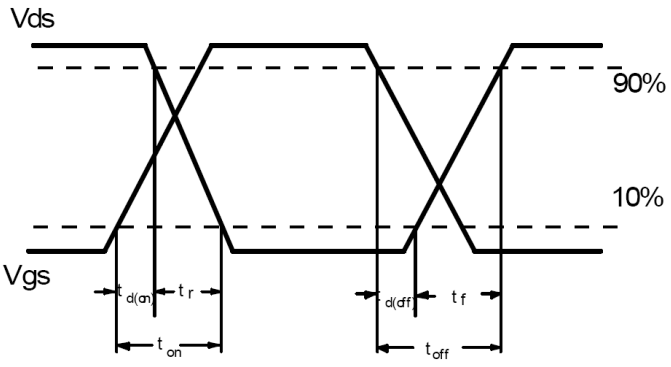
Gate charge test circuit



Switching Time Test Circuit



Switching Waveforms



Notes:

①Calculated continuous current based on maximum allowable junction temperature.

②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

④The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C

Typical electrical and thermal characteristics

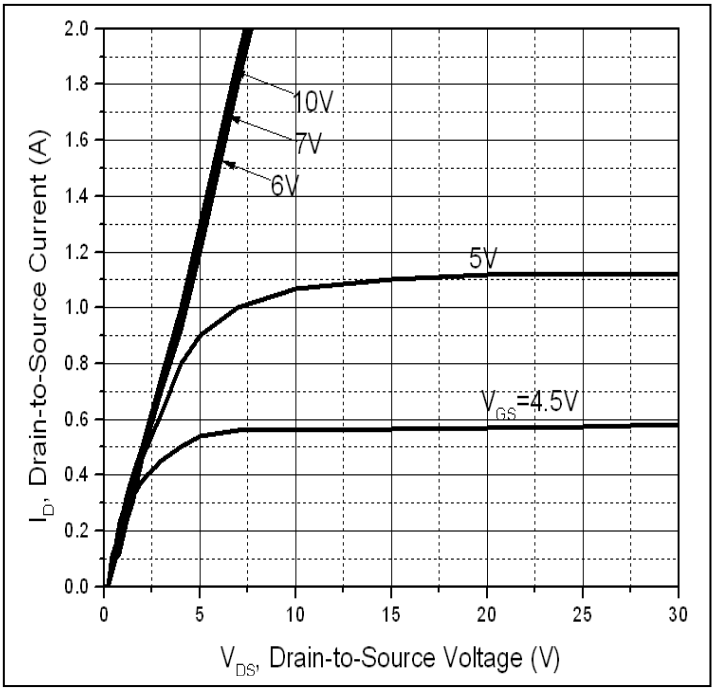


Figure 1: Typical Output Characteristics

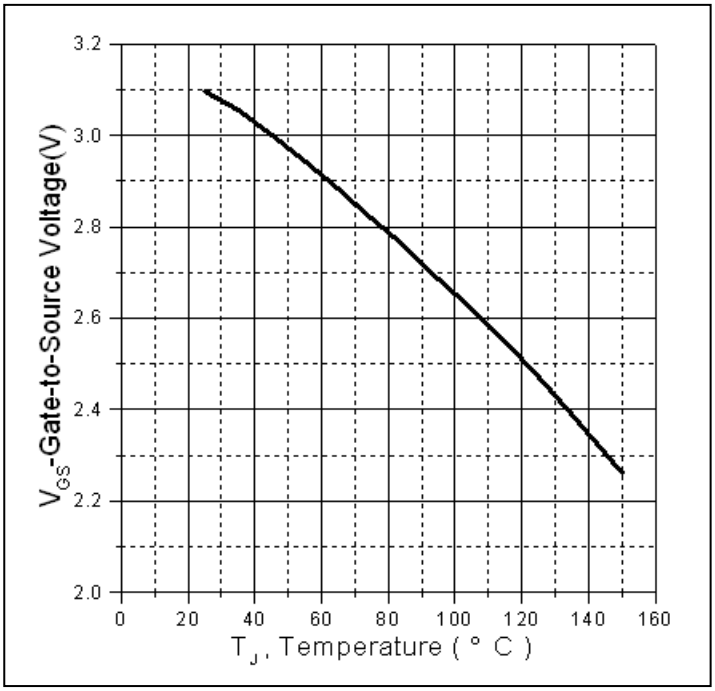


Figure 2. Gate to source cut-off voltage

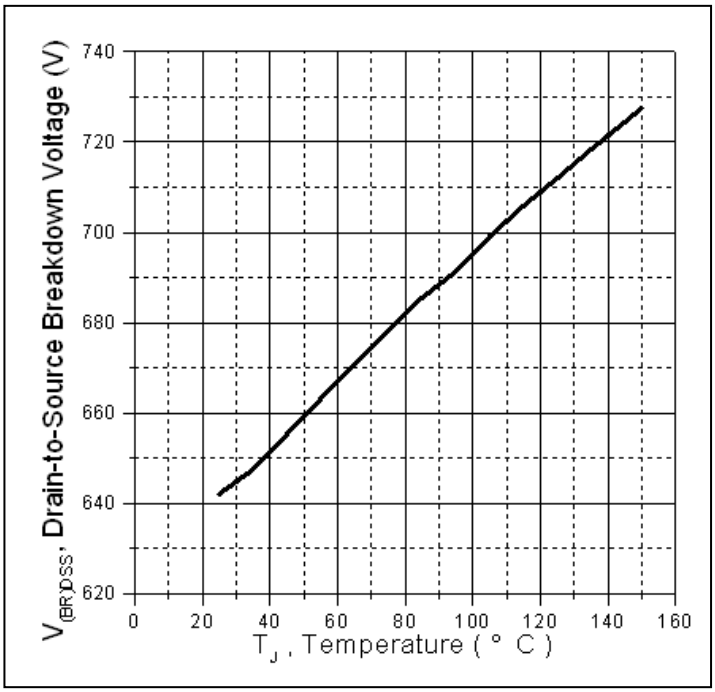


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

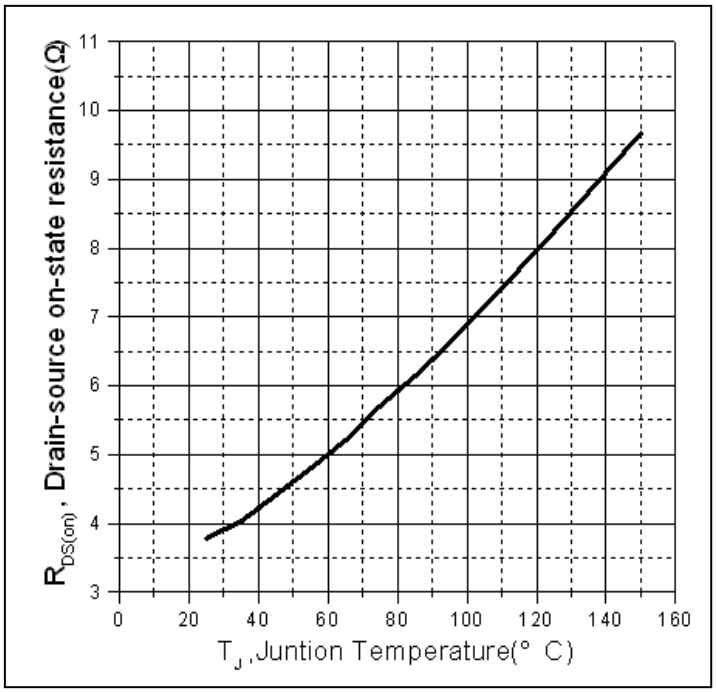


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

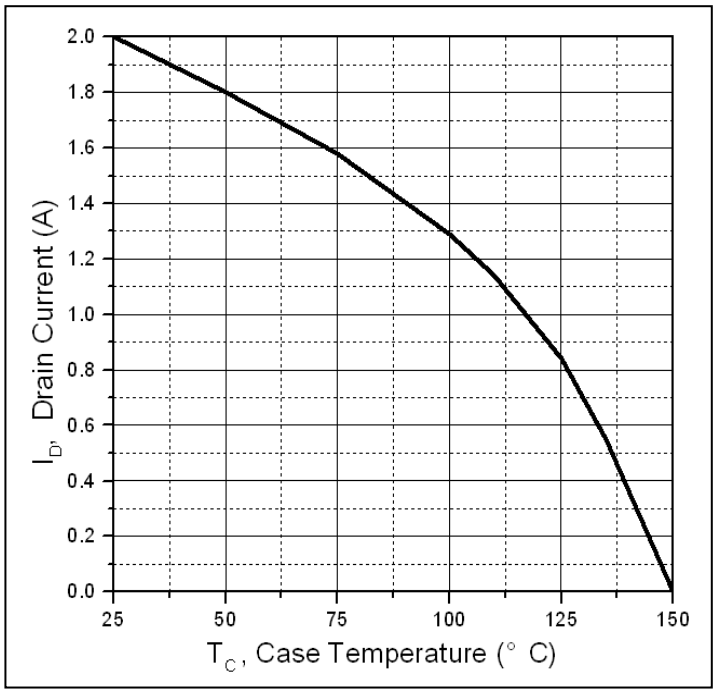


Figure 5. Maximum Drain Current Vs. Case Temperature

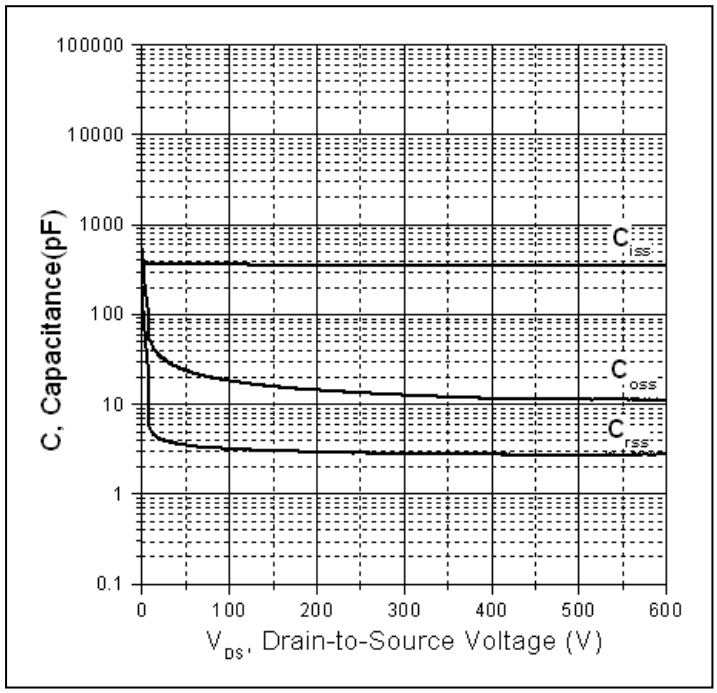


Figure 6.Typical Capacitance Vs. Drain-to-Source Voltage

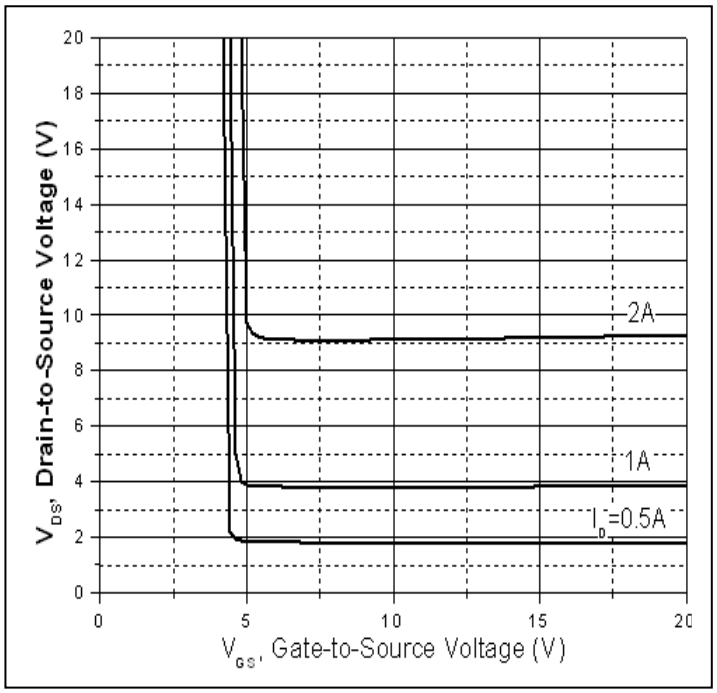


Figure7. Drain-to-Source Voltage Vs. Gate-to-Source Voltage

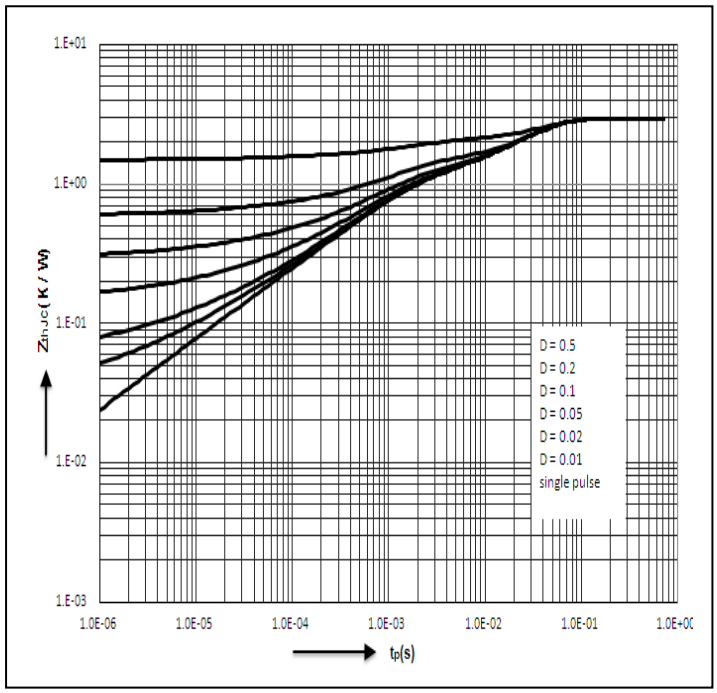
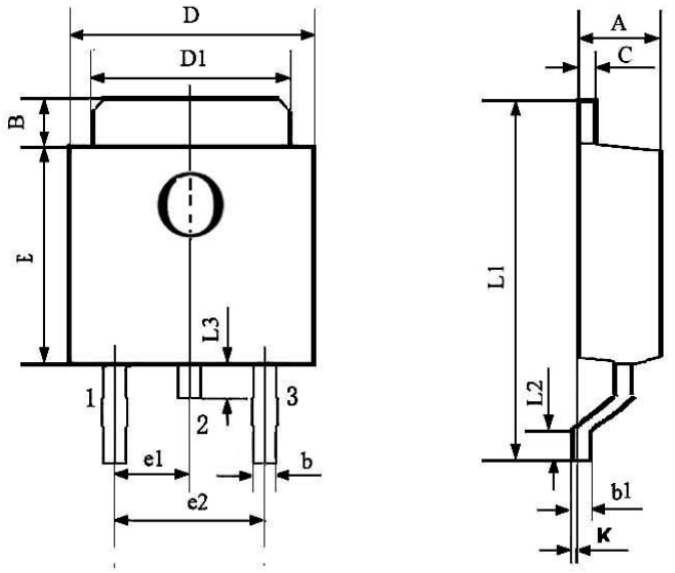


Figure8. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data：

TO-252 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	-	2.400	0.087	-	0.094
B	0.950	-	1.250	0.037	-	0.049
b	0.500	-	0.700	0.020	-	0.028
b1	0.450	-	0.550	0.018	-	0.022
C	0.450	-	0.550	0.018	-	0.022
D	6.450	-	6.750	0.254	-	0.266
D1	5.200	-	5.400	0.205	-	0.213
E	5.950	-	6.250	0.234	-	0.246
e1	2.240	-	2.340	0.088	-	0.092
e2	4.430	-	4.730	0.174	-	0.186
L1	9.450	-	9.950	0.372	-	0.392
L2	1.250	-	1.750	0.049	-	0.069
L3	0.600	-	0.900	0.024	-	0.035
K	0.000	-	0.100	0.000	-	0.004

Ordering and Marking Information

Device Marking: SSF2N60D

Package (Available)

TO-252(D-PAK)

Operating Temperature Range

C : -55 to 150 °C

Devices per Unit（options）

Package Type	Units/Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-252	2500	2	5000	7	35000
TO-252	2500	1	2500	10	25000
TO-252	800	5	4000	8	32000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ to 150℃ @ 80% of Max V_{DSS}/V_{CES}/VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=150℃ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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