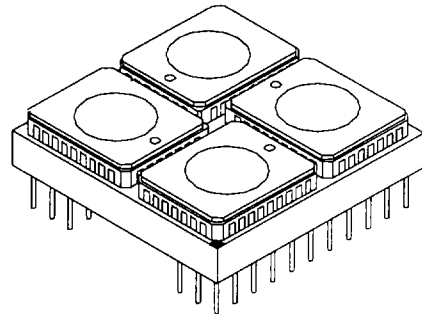


### DESCRIPTION:

The DPV256X32V is a 66-pin Pin Grid Array (PGA) consisting of four 256K X 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matched thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

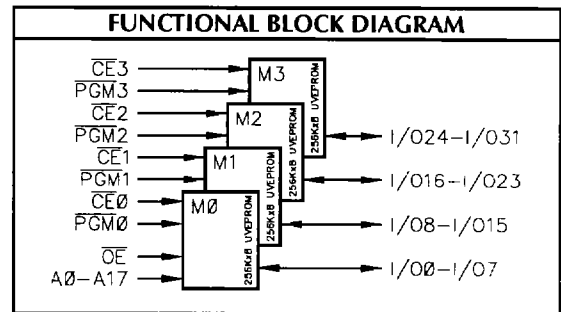
The pins have been arranged around a central 0.6" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing four 0.1µf decoupling capacitors.



### FEATURES:

- Organizations Available:  
1024K X 8, 512K X 16 or 256K X 32
- Access Times:  
100\*, 120\*, 150, 200, 250ns
- Fully Static Operation  
- No clock or refresh required
- Programming Voltage 12.75 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm  
(100µs Pulses Typ.)
- Common Data Inputs and Outputs
- Power Consumption:  
22mW (Standby)  
1.1W (Active)
- TTL-compatible Inputs and Outputs
- 66-Pin PGA (Pin Grid Array) Package
- Same Package as other Versapac Versions  
(EEPROM, SRAM and MIXED)
- Module Weight is 15 grams

\* Commercial and industrial only.



PIN NAMES	
A0 - A17	Address Inputs
I/O0 - I/O31	Data In/Out
CE0 - CE3	Chip Enables
PGM0 - PGM3	Program Enables
OE	Output Enable
VDD	Power (+5V)
VSS	Ground
VPP	Programming Voltage
N.C.	No Connect

### PIN-OUT DIAGRAM

1 I/08	12 PGM1	23 I/015	Ⓜ Ⓜ Ⓜ	Ⓜ Ⓜ Ⓜ	34 I/024	45 VDD	56 I/031
2 I/09	13 CE1	24 I/014	○○○	○○○	35 I/025	46 CE3	57 I/030
3 I/010	14 VSS	25 I/013	○○○	○○○	36 I/026	47 PGM3	58 I/029
4 A13	15 I/011	26 I/012	○○○	○○○	37 A6	48 I/027	59 I/028
5 A14	16 A10	27 OE	○○○	○○○	38 A7	49 A3	60 A0
6 A15	17 A11	28 N.C.	○○○ (TOP VIEW)	○○○	39 VPP	50 A4	61 A1
7 A16	18 A12	29 PGM0	○○○	○○○	40 A8	51 A5	62 A2
8 A17	19 VDD	30 I/07	○○○	○○○	41 A9	52 PGM2	63 I/023
9 I/00	20 CE0	31 I/06	○○○	○○○	42 I/016	53 CE2	64 I/022
10 I/01	21 N.C.	32 I/05	○○○	○○○	43 I/017	54 VSS	65 I/021
11 I/02	22 I/03	33 I/04	Ⓜ Ⓜ Ⓜ	Ⓜ Ⓜ Ⓜ	44 I/018	55 I/019	66 I/020

ABSOLUTE MAXIMUM RATINGS <sup>1</sup>			
Symbol	Parameter	Value	Unit
T <sub>STG</sub>	Storage Temperature	-65 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
V <sub>DD</sub>	Supply Voltage <sup>2</sup>	-0.5 to +7.0	V
V <sub>I/O</sub>	Input/Output Voltage <sup>2</sup>	-0.5 to V <sub>DD</sub> +0.6	V
V <sub>PP</sub>	Programming Voltage <sup>2</sup>	-0.5 to +13.5	V

AC TEST CONDITIONS: Including Programming	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Time	≤ 20ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

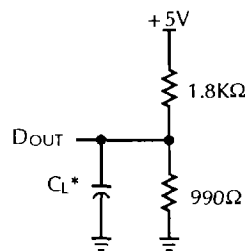
RECOMMENDED OPERATING RANGE <sup>2</sup>					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage <sup>4</sup>	4.5	5.0	5.5	V
V <sub>IH</sub>	Input HIGH Voltage	2.0		V <sub>DD</sub> +0.5	V
V <sub>IL</sub>	Input LOW Voltage	-0.2		0.8	V
V <sub>PP</sub>	V <sub>PP</sub> Supply Voltage <sup>5</sup>	12.5	12.75	13.0	V

Output Load		
Float	C <sub>L</sub>	Parameters Measured
1	100 pF	except t <sub>DF</sub> and t <sub>DFP</sub>
2	5 pF	t <sub>DF</sub> and t <sub>DFP</sub>

CAPACITANCE <sup>3</sup> : T <sub>A</sub> = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C <sub>CE</sub>	Chip Enable	15	pF	V <sub>IN</sub> = 0V
C <sub>ADR</sub>	Address Input	50		
C <sub>OE</sub>	Output Enable	50		
C <sub>I/O</sub>	Data Input/Output	25		

Figure 1. Output Load

\* Including Scope and Jig Capacitance.



DC OPERATING CHARACTERISTICS <sup>6</sup> : Over operating ranges (unless otherwise stated)									
Symbol	Characteristics	Test Conditions	X8		X16		X32		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = V <sub>DD</sub>	-4	4	-4	4	-4	4	μA
I <sub>OUT</sub>	Output Leakage Current	$\overline{CE} = V_{IH}, V_{IN} = V_{DD} \text{ or } V_{SS}$	-20	20	-10	10	-5	5	μA
I <sub>CC</sub>	V <sub>DD</sub> Operation Current, Read	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> = 0mA Cycle = min. Duty = 100%		65		125		240	mA
I <sub>SB1</sub>	V <sub>DD</sub> Standby Current (TTL)	$\overline{CE} = V_{IH}, V_{IN} = V_{IH} \text{ or } V_{IL}$		4		4		4	mA
I <sub>SB2</sub>	V <sub>DD</sub> Standby Current (CMOS)	$\overline{CE} = V_{DD} \pm 0.3V$ V <sub>IN</sub> ≥ V <sub>DD</sub> - 3.0V or V <sub>IN</sub> ≤ 0.3V		400		400		400	μA
I <sub>PP1</sub>	V <sub>PP</sub> Supply Current Programming	$\overline{CE}, \overline{OE} = V_{IH}, T_A = 25^\circ C \pm 5^\circ C$		30		60		120	mA
I <sub>PP3</sub>	V <sub>PP</sub> Supply Current Read <sup>4</sup>	$\overline{CE}, \overline{OE} = V_{IL}, I_{OUT} > 0mA$		400		400		400	μA
V <sub>OL</sub>	Output LOW Voltage	I <sub>OUT</sub> = 2.1mA		0.45		0.45		0.45	V
V <sub>OH1</sub>	Output HIGH Voltage	I <sub>OUT</sub> = -400μA	2.4		2.4		2.4		V
V <sub>IL</sub>	Input LOW Level		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
V <sub>IH</sub>	Input HIGH Level		2.0	V <sub>DD</sub> +0.5	2.0	V <sub>DD</sub> +0.5	2.0	V <sub>DD</sub> +0.5	V

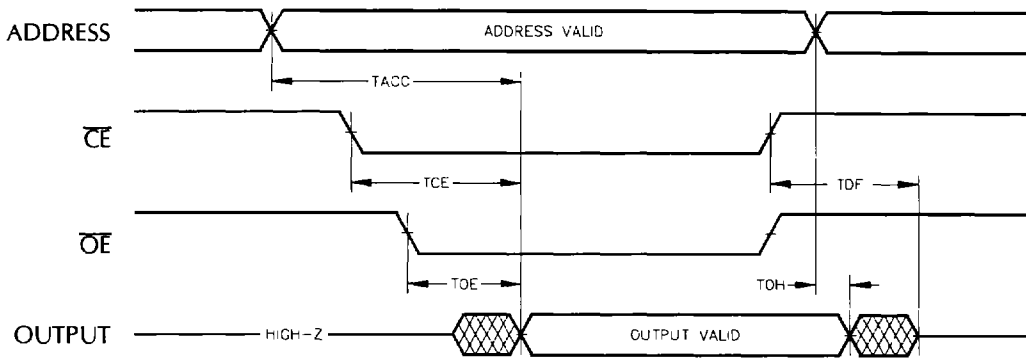
FUNCTIONS AND PIN CONNECTIONS							
Mode	Function	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	$V_{PP}$	$V_{DD}$	I/O0-I/O31
Read Operations	Read	L	L	X	5V	5V	Data Out
	Output Deselect	X	H	X			High Impedance
	Standby	H	X	X			High Impedance
Program Operations ( $T_A = +25 \pm 5^\circ\text{C}$ )	Program	L	H	L	12.75V	6.25V	Data In
	Program Inhibit	H	X	X			High Impedance
	Program Verify	L	L	H			Data Out

L = LOW, H = HIGH and X = Don't Care

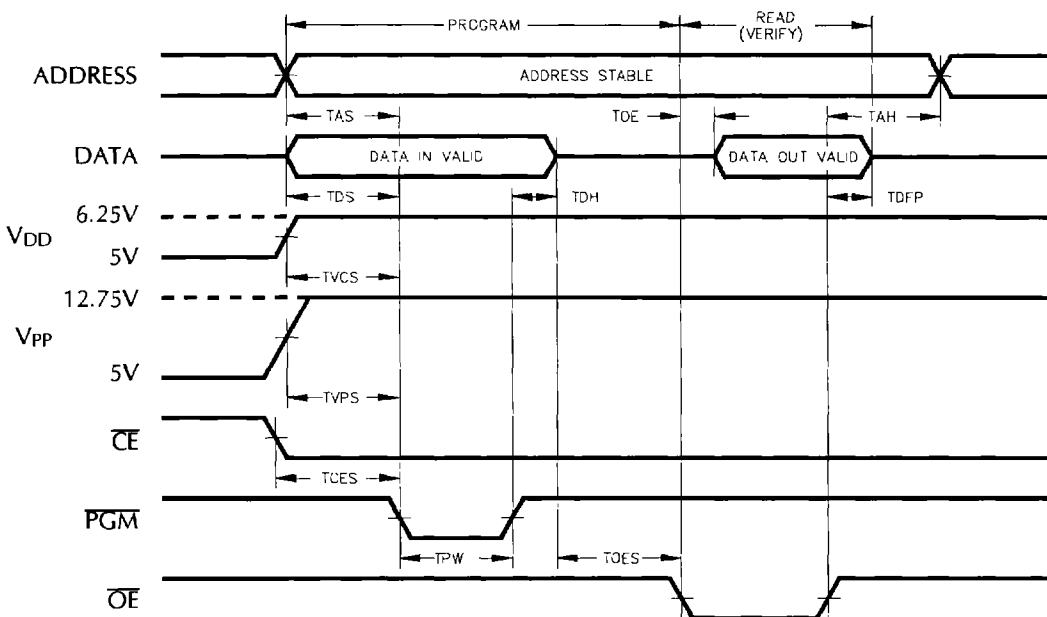
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ: Over operating ranges													
No.	Symbol	Parameter	-100		-120		-150		-200		-250		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	$t_{ACC}$	Address Access Time <sup>8</sup>		100		120		150		200		250	ns
2	$t_{CE}$	Chip Enable to Output Valid <sup>7</sup>		100		120		150		200		250	ns
3	$t_{OE}$	Output Enable to Output Valid <sup>7, 8</sup>		50		50		65		75		100	ns
4	$t_{DF}$	$\overline{OE}$ or $\overline{CE}$ HIGH to Output Float <sup>3, 9</sup>	0	40	0	40	0	50	0	60	0	60	ns
5	$t_{OH}$	Output Hold from Address Change	0		0		0		0		0		ns

AC PROGRAMMING CONDITIONS AND CHARACTERISTICS: Over operating ranges					
No.	Symbol	Parameter	Min.	Max.	Unit
6	$t_{AS}$	Address Set-up Time	2		$\mu\text{s}$
7	$t_{CES}$	Chip Enable Set-up Time	2		$\mu\text{s}$
8	$t_{OES}$	Output Enable Set-up Time	2		$\mu\text{s}$
9	$t_{DS}$	Data Set-up Time	2		$\mu\text{s}$
10	$t_{VCS}$	$V_{DD}$ Set-up Time <sup>5</sup>	2		$\mu\text{s}$
11	$t_{VPS}$	$V_{PP}$ Set-up Time <sup>5</sup>	2		$\mu\text{s}$
12	$t_{AH}$	Address Hold Time	0		$\mu\text{s}$
13	$t_{DH}$	Data Hold Time	2		$\mu\text{s}$
14	$t_{DFP}$	Output Enable HIGH Output Float Delay <sup>5</sup>	0	130	ns
15	$t_{PW}$	Programming Pulse Width <sup>10</sup>	95	105	$\mu\text{s}$
16	$t_{OE}$	Data Valid from Output Enable		150	ns

READ TIMING



PROGRAMMING TIMING <sup>4</sup>



## PROGRAMMING AND ERASING INFORMATION

**Programming**

Upon delivery from Dense-Pac, or after erasure (See *Erasure section*), the DPV256X32V contains "1's" in every location, and read data is in the high state. "0's" are written into the DPV256X32V through the procedure of programming. A 0.1 $\mu$ F capacitor between  $V_{PP}$  and  $V_{SS}$  is required to prevent excessive voltage transients during programming which could damage the device. Programming modes require +6.25V and +12.75V to be applied to  $V_{DD}$  and  $V_{PP}$  respectively.

Individual bytes or address locations can be selected and programmed by using the programming algorithm shown in Figure 2. In the programming mode,  $\overline{CE}$  is set at  $V_{IL}$ ,  $\overline{OE}$  is set at  $V_{IH}$ ,  $V_{DD}$  is set at +6.25V, and  $V_{PP}$  is set at +12.75V. After the applied address and input data signals are stable, programming is accomplished by a 100 $\mu$ s  $V_{IL}$  pulse on the  $\overline{PGM}$  pin (refer to the *Programming Timing Diagram*).

First program each address with a 100 $\mu$ s pulse on the  $\overline{PGM}$  without verification. Then return to first address and start a verification loop verifying each address. If an address location fails verification, apply up to 25 consecutive 100 $\mu$ s  $\overline{PGM}$  pulses with a verification after each pulse.

If the device fails to program after 25 attempts, the programming is considered failed. After the byte is verified, continue the algorithm through all the required addresses. Then lower  $V_{DD}$  and  $V_{PP}$  to +5.0Vdc and compare the data programmed with the original data to determine if the device passes. A programming adapter for programming on standard EPROM programmers is available, contact Dense-Pac sales for more information.

**Erasure**

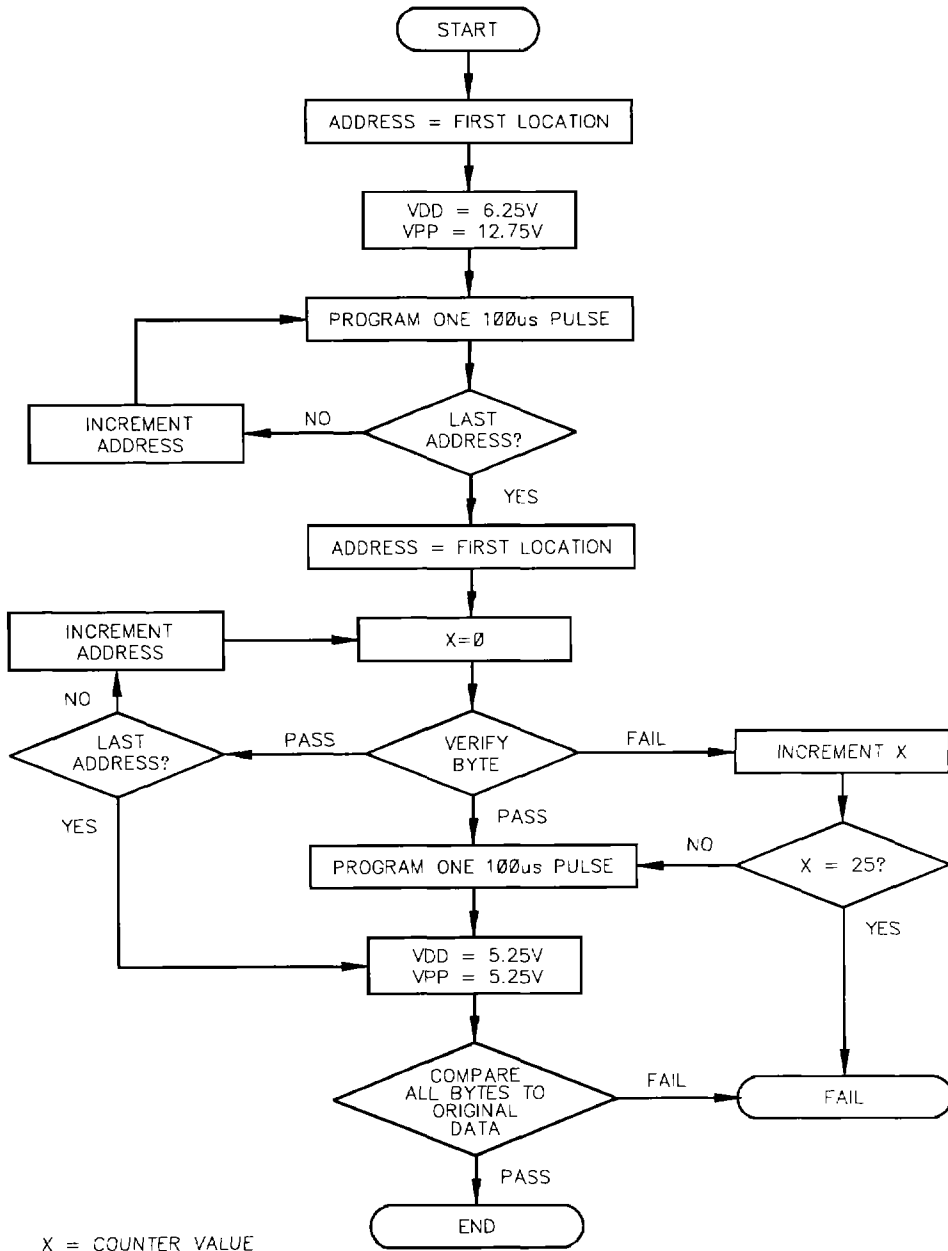
To clear all locations of their programmed contents it is necessary to expose the DPV256X32V to an ultraviolet light source. A dosage of 15W-seconds/cm<sup>2</sup> is required to completely erase a DPV256X32V. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (A) with an intensity of 12,000 $\mu$ W/cm<sup>2</sup>] for 20 minutes.

The DPV256X32V and similar devices can be erased by light sources having wavelengths shorter than 4000A. Although erasure time will be much longer than with UV sources at 2537A, nevertheless the exposure to fluorescent light or sunlight will eventually erase the DPV256X32V. After programming, the package windows should be covered by an opaque label or substance, to prevent inadvertent erasure.

**NOTES:**

1. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are with respect to  $V_{SS}$ .
3. This parameter is guaranteed and not 100% tested.
4.  $V_{DD}$  must be applied either coincident with or before  $V_{PP}$  and removed either coincident with or after  $V_{PP}$ .
5.  $V_{PP}$  must not be greater than 13.5 V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with  $V_{PP} = 12.75V$ . Also, during  $\overline{CE} = V_{IL}$ ,  $V_{PP}$  must not be switched from 5.0V to 12.750V or vice-versa.
6.  $t_A = -55^\circ C$  to  $+125^\circ C$ ,  $V_{DD} = 5.0V \pm 0.5V$ , and  $V_{PP} = V_{DD}$  reading.  $t_A = +25^\circ C \pm 5^\circ C$ ,  $V_{DD} = 6.25V \pm 0.25V$ ,  $V_{PP} = 12.75V \pm 0.25V$  programming.
7.  $\overline{OE}$  may be delayed up to  $t_{CE-tOE}$  after the following edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
8.  $\overline{OE}$  may be delayed up to  $t_{ACC-tOE}$  after the following Address is valid without impact on  $t_{ACC}$ .
9.  $T_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.
10. Program Pulse Width Tolerance is 100 $\mu$ s  $\pm$  5%.

Figure 2. Programming Flow Chart



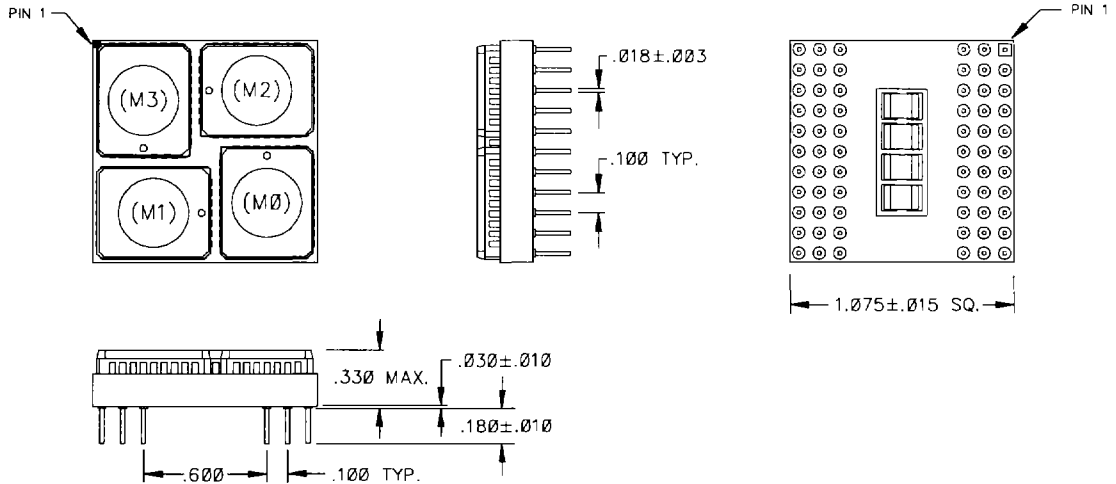
ORDERING INFORMATION

DP V256X32 V - XX X  
 PREFIX DEVICE TYPE PACKAGE SPEED GRADE

C	COMMERCIAL	0° to +70°C
I	INDUSTRIAL	-40° to +85°C
M	MILITARY	-55° to +125°C
B *	MIL-PROCESSED	-55° to +125°C
10	100ns	"C" & "I" GRADE ONLY
12	120ns	"C" & "I" GRADE ONLY
15	150ns	
20	200ns	
25	250ns	
V	66-PIN PGA VERSAPAC	
UVEPROM 1024KX8, 512KX16 OR 256KX32		

\* B grade modules are constructed with 883 devices.

MECHANICAL DIAGRAMS



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 (714) 898-0007 ♦ (800) 642-4477 (Outside CA) ♦ FAX: (714) 897-1772