SPN3402

DESCRIPTION

The SPN3402 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

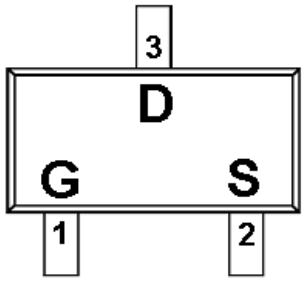
APPLICATIONS

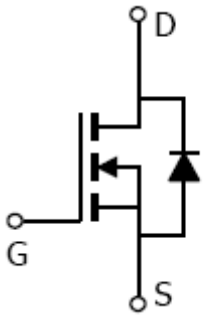
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

FEATURES

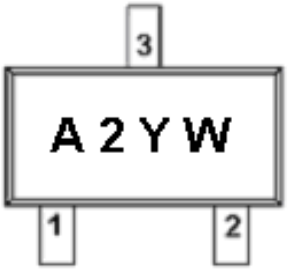
- 30V/2.8A,$R_{DS(ON)}$= 58mΩ@V_{GS}=10V
- 30V/2.3A,$R_{DS(ON)}$= 65mΩ@V_{GS}=4.5V
- 30V/1.5A,$R_{DS(ON)}$= 105mΩ@V_{GS}=2.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

PIN CONFIGURATION (SOT-23-3L)





PART MARKING



Y : Year Code
W : Week Code

SPN3402

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN3402S23RG	SOT-23-3L	A2YW
SPN3402S23RGB	SOT-23-3L	A2YW

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPN3402S23RG : Tape Reel ; Pb – Free
※ SPN3402S23RGB : Tape Reel ; Pb – Free; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate –Source Voltage		V_{GSS}	±12	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	4.0	A
	T_A=70℃		2.8	
Pulsed Drain Current		I_{DM}	10	A
Continuous Source Current(Diode Conduction)		I_S	1.25	A
Power Dissipation	T_A=25℃	P_D	1.25	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	100	℃/W

SPN3402

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	0.8		1.6	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V,V_{GS}=0.0V			1	uA
		V_{DS}=24V,V_{GS}=0.0V T_J=55℃			10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≧4.5V,V_{GS}=10V	6			A
		V_{DS}≧4.5V,V_{GS}=4.5V	4			
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V,I_D=2.8A		0.048	0.058	Ω
		V_{GS} =4.5V,I_D=2.3A		0.053	0.065	
		V_{GS} =2.5V,I_D=1.5A		0.080	0.105	
Forward Transconductance	gfs	V_{DS}=4.5V,I_D=2.8A		4.6		S
Diode Forward Voltage	V_{SD}	I_S=1.25A,V_{GS}=0V		0.82	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=15,V_{GS}=4.5V I_D≡2.0A		4.2	6	nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			1.5		
Input Capacitance	C_{iss}	V_{DS}=15,V_{GS}=0V f =1MHz		350		pF
Output Capacitance	C_{oss}			55		
Reverse Transfer Capacitance	C_{rss}			41		
Turn-On Time	$t_{d(on)}$	V_{DD}=15,R_L=10Ω V_{GEN}=10V,R_G=3Ω		2.5		ns
	t_r			2.5		
Turn-Off Time	$t_{d(off)}$			20		
	t_f			4		