

MN3718MFE, MN3718MAE

6mm (1/3 inch) 768H High-Resolution CCD Area Image Sensors

■ Overview

The MN3718MFE and MN3718MAE are 6mm (1/3 inch) Interline Transfer CCD (IT-CCD) solid state image sensor devices.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal read out. The electronic shutter function has made possible an exposure time of 1/10000 seconds. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and low smear.

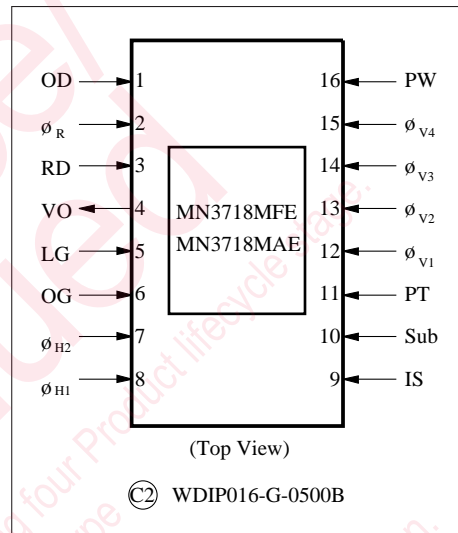
This device has a total of 410K pixels (811 horizontal × 494 vertical) and provides stable and clear images with a resolution of 480 horizontal TV-lines and 350 vertical TV-lines.

Type No.	Size	System	Color or B/W
MN3718MFE	6mm (1/3 inch)	NTSC	Color
MN3718MAE		E I A	B/W

■ Features

- Total number of pixels: 811 (horizontal) × 494 (vertical)
- High sensitivity
- Low noise
- Broad dynamic range
- Low smear
- Low image lag
- Electronic shutter function present
- No image distortion
- Small size enables design of compact equipment
- High reliability
- 16 Pin DIL ceramic package (cerdip)

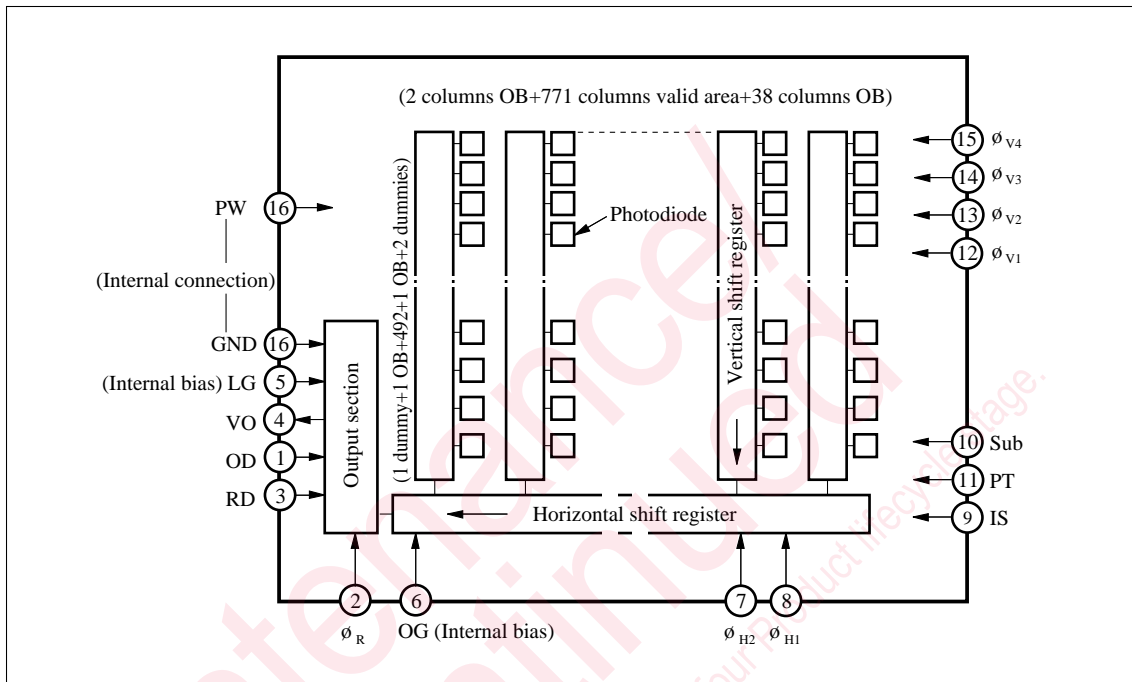
■ Pin Assignments



■ Applications

- Compact lightweight camcoders
- Cameras for surveillance, measurement, and medical use

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	OD	Output drain	9	IS	Horizontal CCD input source
2	ϕ_R	Reset pulse	10	Sub	Substrate
3	RD	Reset drain	11	PT	P-well for protection circuit
4	VO	Video output	12	ϕ_{v1}	Vertical shift register clock pulse (1)
5	LG	Output load transistor gate	13	ϕ_{v2}	Vertical shift register clock pulse (2)
6	OG	Output gate	14	ϕ_{v3}	Vertical shift register clock pulse (3)
7	ϕ_{H2}	Horizontal register clock pulse (2)	15	ϕ_{v4}	Vertical shift register clock pulse (4)
8	ϕ_{H1}	Horizontal register clock pulse (1)	16	PW	P-well

■ Absolute Maximum Ratings and Operating Conditions

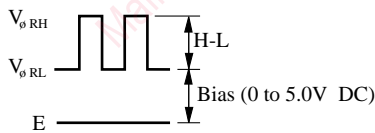
Parameter	Symbol	Rating ^{Note 2)}		Operating condition ^{Note 1)}			Unit	
		min	max	min	typ	max		
Reset drain voltage	V _{RD}	-0.2	18	14.5	15.0	15.5	V	
Output drain voltage	V _{OD}	-0.2	18	14.5	15.0	15.5	V	
Output load transistor gate voltage ^{Note 3)}	V _{LG}	(Supplied internally)					V	
Output gate voltage ^{Note 3)}	V _{OG}	(Supplied internally)					V	
Horizontal CCD input source voltage	V _{IS}	-0.2	18	14.5	15.0	15.5	V	
Protection P well voltage	V _{PT}	-10.0	0.2	ϕ _{V(L)} -1.2	ϕ _{V(L)} -1.0	ϕ _{V(L)} -0.7	V	
P well voltage	V _{PW}	Reference voltage		—	0	—	V	
Reset pulse voltage	H-L	V _{ϕR (H-L)} * 1	—	18	4.7	5.0	5.3	V
	Bias	V _{ϕR (Bias)} * 1	-0.2	—	0	Adjust	5.0	V
Horizontal register clock pulse voltage 1	V _{ϕH1 (H)}	—	18	4.7	5.0	5.3	V	
	V _{ϕH1 (L)}	-0.2	—	0	0	0	V	
Horizontal register clock pulse voltage 2	V _{ϕH2 (H)}	—	18	4.7	5.0	5.3	V	
	V _{ϕH2 (L)}	-0.2	—	0	0	0	V	
Vertical shift register clock pulse voltage 1	V _{ϕV1 (H)}	—	18	14.5	15.0	15.5	V	
	V _{ϕV1 (M)}	—	—	-0.2	0	0.2	V	
	V _{ϕV1 (L)}	-9	—	-7.3	-7.0	-6.7	V	
Vertical shift register clock pulse voltage 2	V _{ϕV2 (M)}	—	15	0.8	1.0	1.2	V	
	V _{ϕV2 (L)}	-9	—	-7.3	-7.0	-6.7	V	
Vertical shift register clock pulse voltage 3	V _{ϕV3 (H)}	—	18	14.5	15.0	15.5	V	
	V _{ϕV3 (M)}	—	—	-0.2	0	0.2	V	
	V _{ϕV3 (L)}	-9	—	-7.3	-7.0	-6.7	V	
Vertical shift register clock pulse voltage 4	V _{ϕV4 (M)}	—	15	0.8	1.0	1.2	V	
	V _{ϕV4 (L)}	-9	—	-7.3	-7.0	-6.7	V	
Substrate voltage	V _{Sub} * 2	—	—	3.0	Adjust	14.5	V	
	ϕ V _{Sub} * 2	-0.2	45	24.5	25.0	25.5	V	
Operating temperature	T _{opr}	-10	70	—	25.0	—	°C	
Storage temperature	T _{sig}	-30	80	—	—	—	°C	

Note 1) The initial setting of V_{Sub} shall be 8.0V and shall be adjusted to the minimum voltage at which no blooming is caused at a light input of 100 times the standard value. The standard light input is the one when the exposure is done at an aperture of F/4 using a light source of 2856K and 1050nt, and placing a color temperature conversion filter LB-40 (Hoya) and an IR cutting filter CAW-500 (t=2.5mm) in the light path.

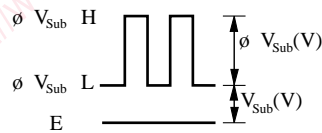
Note 2) Absolute maximum ratings: -0.2 < V_{Sub} - V_{PT} < +55 (V)
 -0.2 < V_{ϕV} - V_{PT} < +24.5 (V)

Note 3) The LG and OG pins should each be grounded via a capacitor of 0.0477μF or more.

*1



*2 V_{Sub} when using electronic shutter function

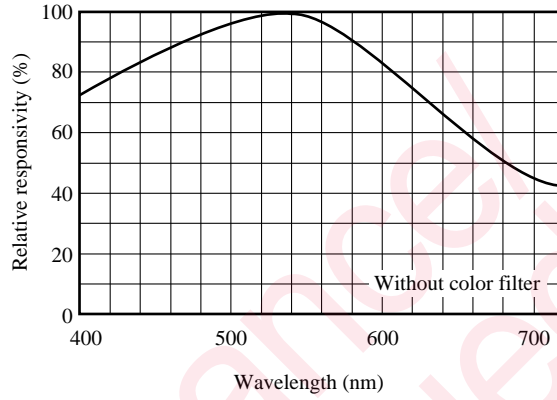


■ Optical Characteristics

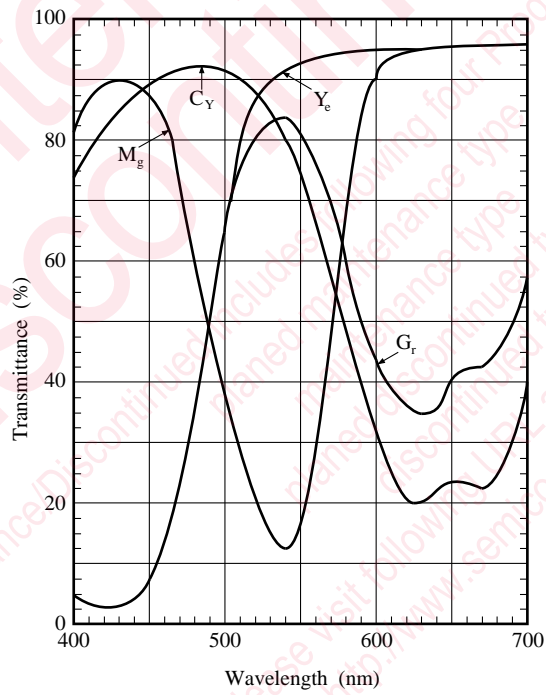
Type No.	Color or B/W	Valid pixels		S/N typ. (dB)	Saturation output typ. (mV)	Sensitivity F8 typ. (mV)	Vertical smear Sm typ. (%)	Image lag typ. (%)	Horizontal resolution typ. (TV-lines)	Vertical resolution typ. (TV-lines)
		H	V							
MN3718MFE	Color	771	492	60	700	300	0.01	0	480	350
MN3718MAE	B/W	771	492	60	1,000	350	0.01	0	550	350

■ Graphs of Characteristics

CCD Spectral Characteristics



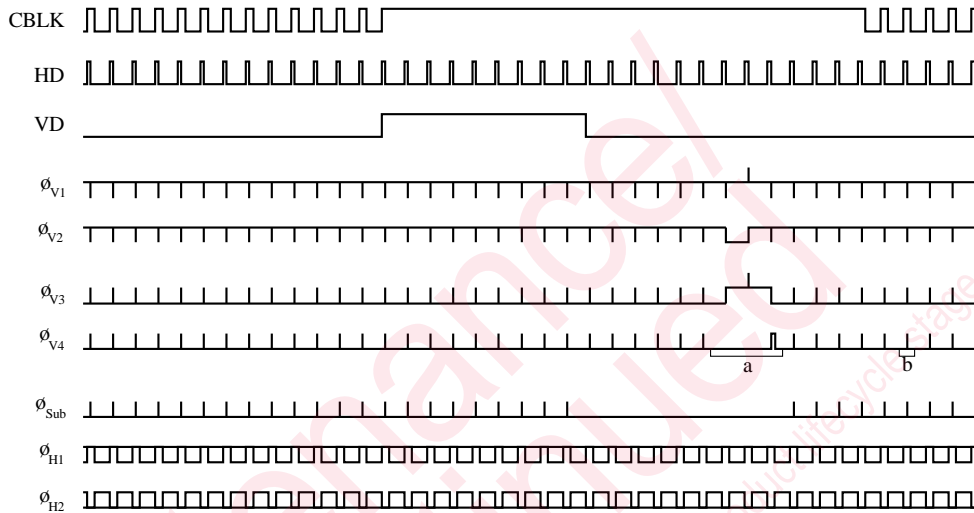
Color Filter Spectral Characteristics



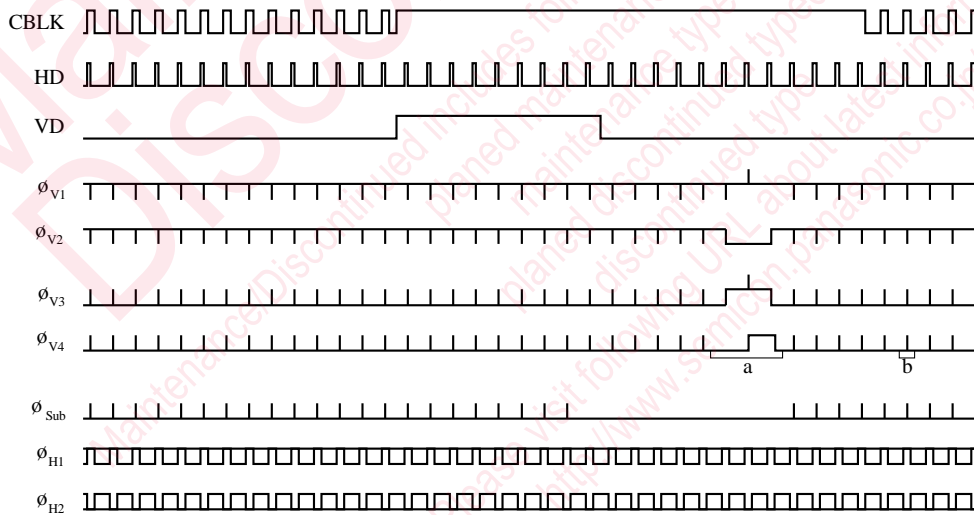
■ Example of Recommended Driving Pulses

- V Rate timing

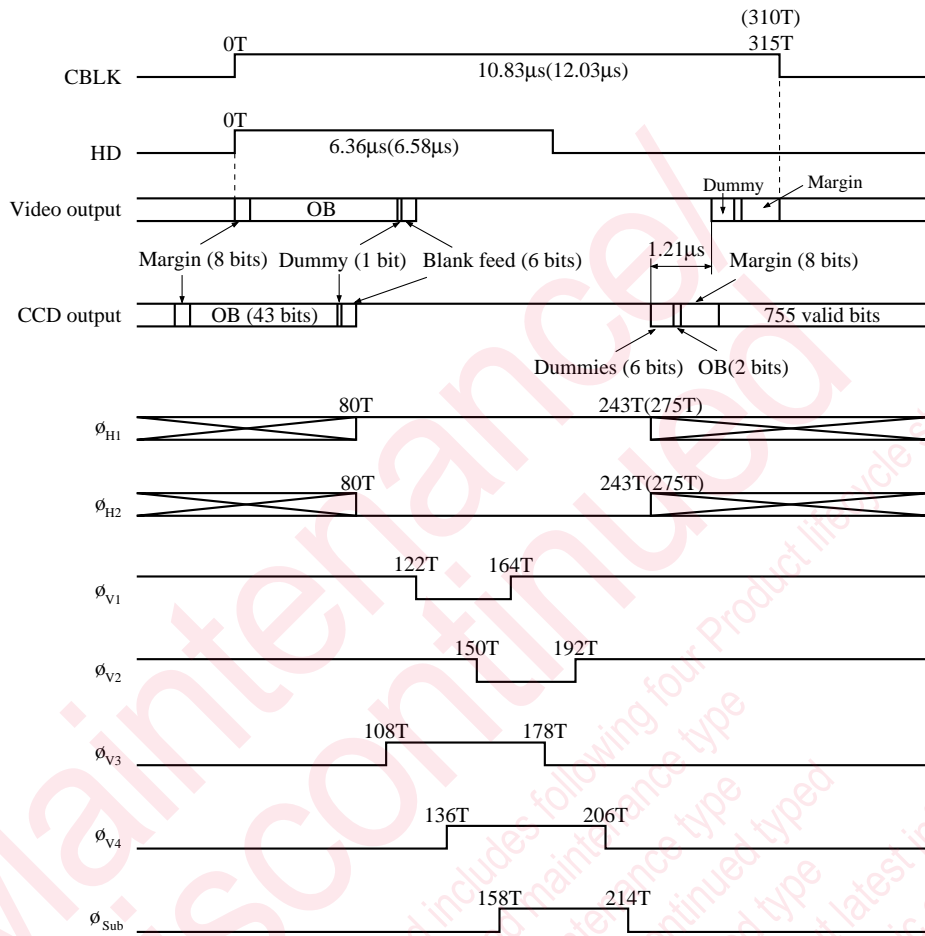
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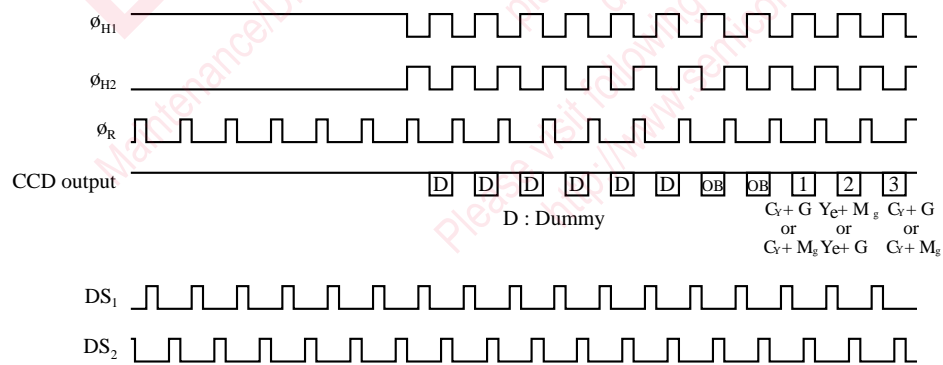
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• H Rate timing



• High speed pulse timing



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