

# NTB5605P, NTB5605

## Power MOSFET -60 V, -18.5 A

### P-Channel, D<sup>2</sup>PAK

#### Features

- Designed for Low  $R_{DS(on)}$
- Withstands High Energy in Avalanche and Commutation Modes
- AEC Q101 Qualified – NTB5605
- These Devices are Pb-Free and are RoHS Compliant

#### Applications

- Power Supplies
- PWM Motor Control
- Converters
- Power Management

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	-60	V
Gate-to-Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	-18.5	A
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	88	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		$I_{DM}$	-55	A
Operating Junction and Storage Temperature			$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 25 \text{ V}, V_{GS} = 5.0 \text{ V}, I_{PK} = 15 \text{ A}, L = 3.0 \text{ mH}, R_G = 25 \Omega$ )			$E_{AS}$	338	mJ
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)			$T_L$	260	$^\circ\text{C}$

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) – Steady State	$R_{\theta JC}$	1.7	$^\circ\text{C/W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

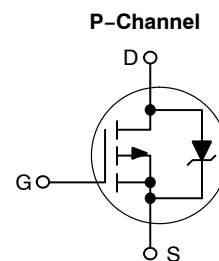
1. When surface mounted to an FR4 board using 1" pad size (Cu Area 1.127 in<sup>2</sup>).
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu Area 0.41 in<sup>2</sup>).



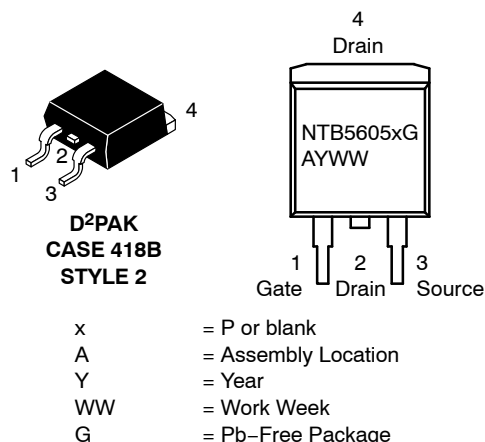
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
-60 V	120 m $\Omega$ @ -5.0 V	-18.5 A



#### MARKING DIAGRAM & PIN ASSIGNMENT



#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTB5605PT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel
NTBV5605T4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTB5605P, NTB5605

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
----------------	--------	----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(Br)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-60			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(Br)DSS</sub> /T <sub>J</sub>			-64		mV/°C	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V V <sub>DS</sub> = -60 V	T <sub>J</sub> = 25°C			-1.0	μA
			T <sub>J</sub> = 125°C				
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V				±100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-1.0	-1.5	-2.0	V
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -5.0 V, I <sub>D</sub> = -8.5 A V <sub>GS</sub> = -5.0 V, I <sub>D</sub> = -17 A		120 140	140	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -8.5 A		12		S
Drain-to-Source On Voltage	V <sub>DS(on)</sub>	V <sub>GS</sub> = -5.0 V, I <sub>D</sub> = -8.5 A			-1.3	V

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = -25 V		730	1190	pF
Output Capacitance	C <sub>oss</sub>			211	300	
Reverse Transfer Capacitance	C <sub>rss</sub>			67	120	
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = -5.0 V, V <sub>DS</sub> = -48 V, I <sub>D</sub> = -17 A		13	22	nC
Gate-to-Source Charge	Q <sub>GS</sub>			4.0		
Gate-to-Drain Charge	Q <sub>GD</sub>			7.0		

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = -5.0 V, V <sub>DD</sub> = -30 V, I <sub>D</sub> = -17 A, R <sub>G</sub> = 9.1 Ω		12.5	25	ns
Rise Time	t <sub>r</sub>			122	183	
Turn-Off Delay Time	t <sub>d(off)</sub>			29	58	
Fall Time	t <sub>f</sub>			75	150	

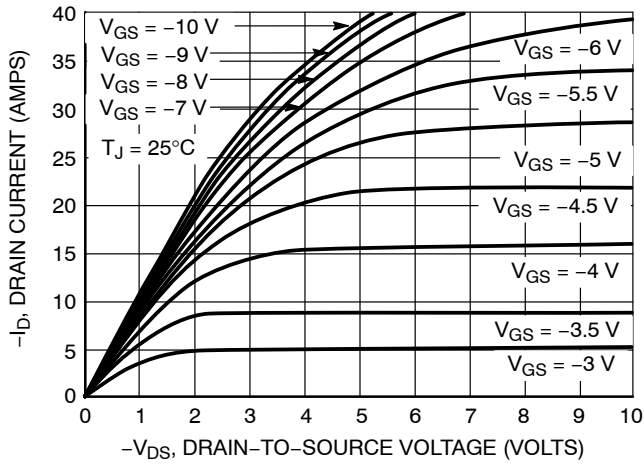
### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V I <sub>S</sub> = -17 A	T <sub>J</sub> = 25°C		-1.55	-2.5	V	
			T <sub>J</sub> = 125°C			-1.4		
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0 V, di <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = -17 A			60		ns	
Charge Time	t <sub>a</sub>					39		
Discharge Time	t <sub>b</sub>					21		
Reverse Recovery Charge	Q <sub>RR</sub>					0.14		

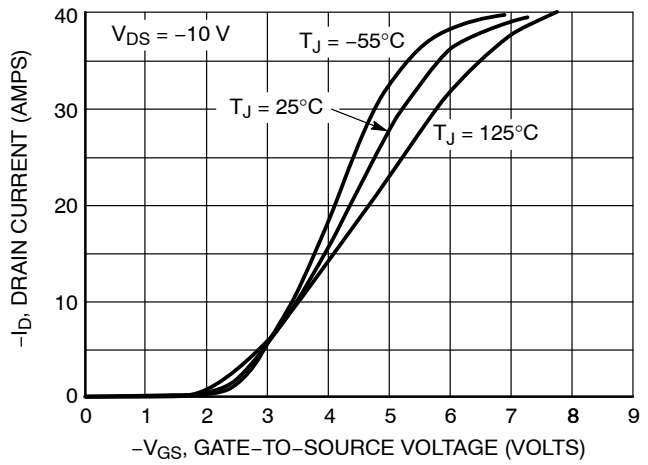
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

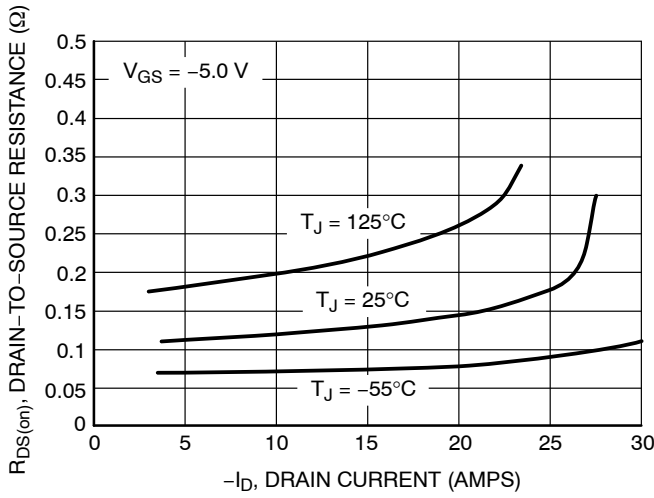
# NTB5605P, NTB5605



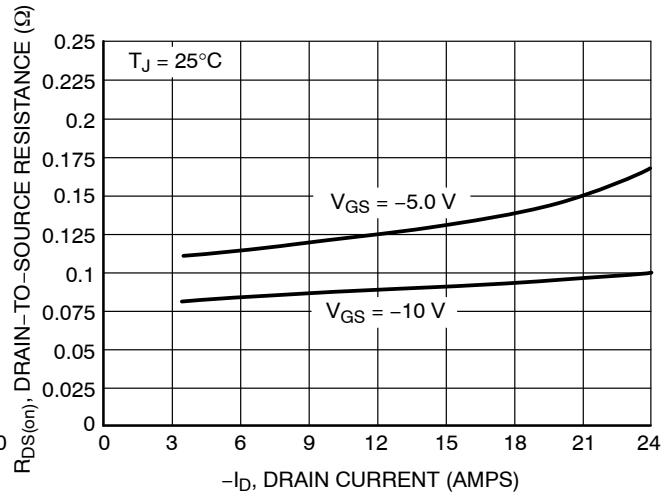
**Figure 1. On-Region Characteristics**



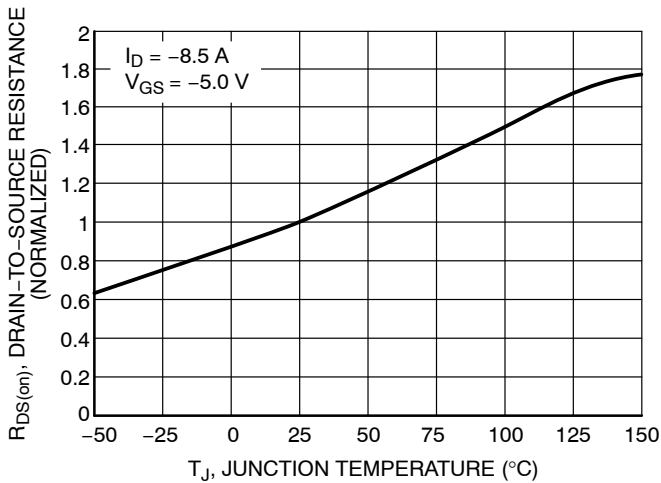
**Figure 2. Transfer Characteristics**



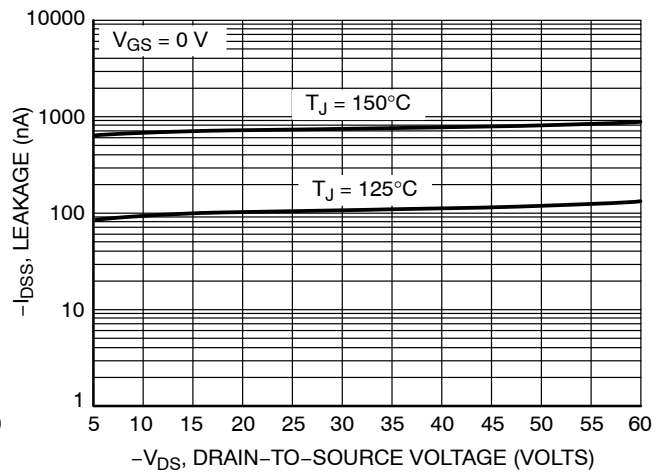
**Figure 3. On-Resistance vs. Drain Current and Temperature**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**

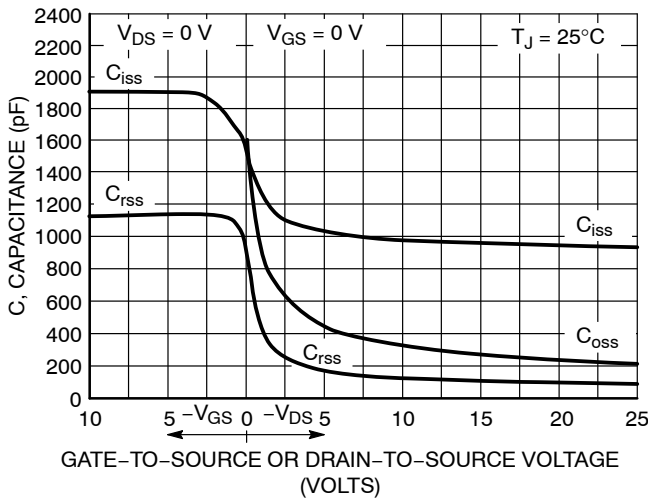


**Figure 5. On-Resistance Variation with Temperature**

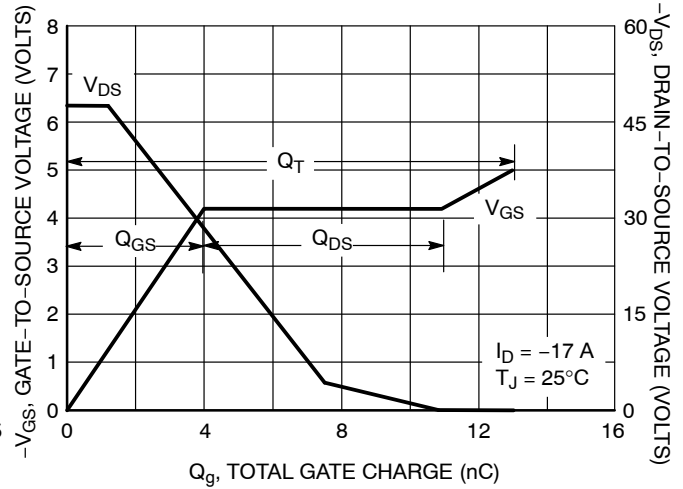


**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

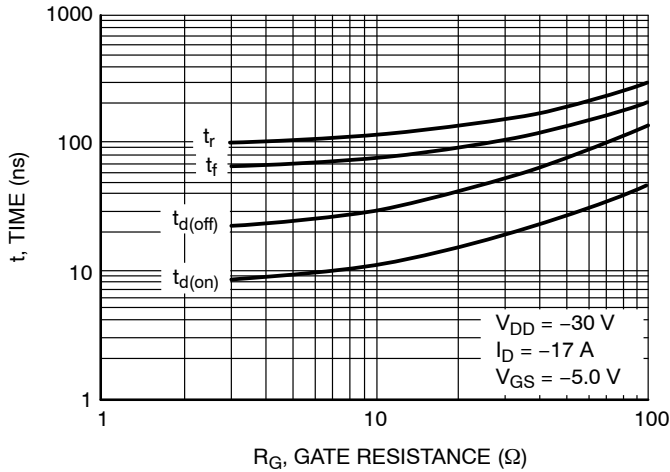
# NTB5605P, NTB5605



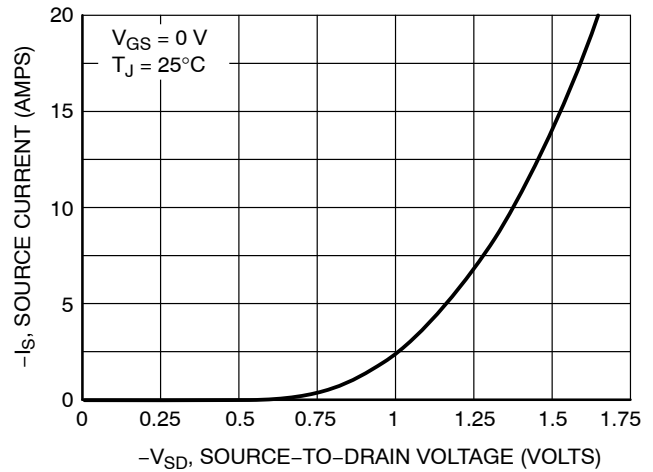
**Figure 7. Capacitance Variation**



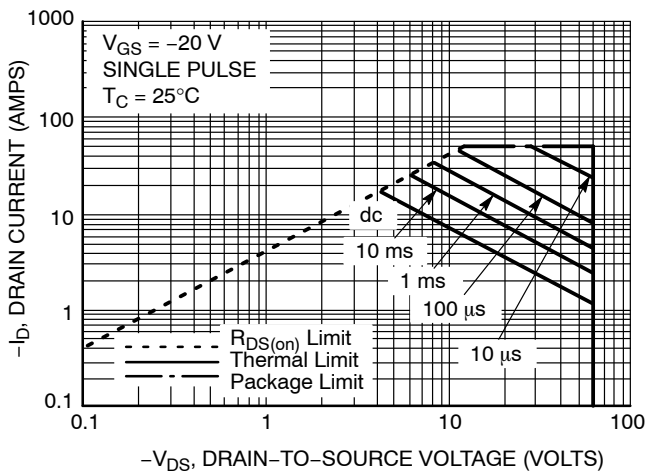
**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



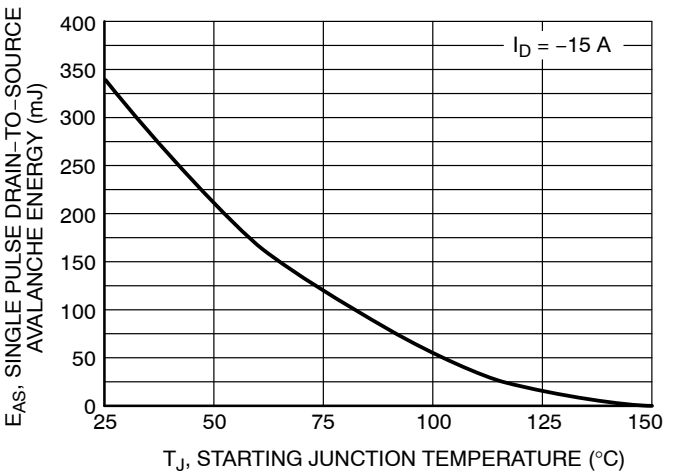
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

NTB5605P, NTB5605

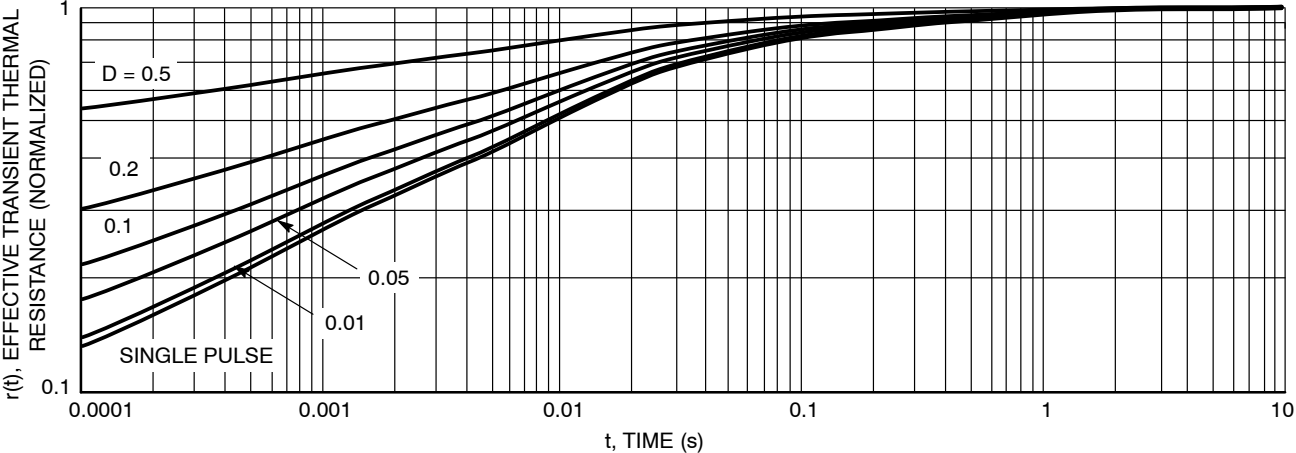


Figure 13. Thermal Response

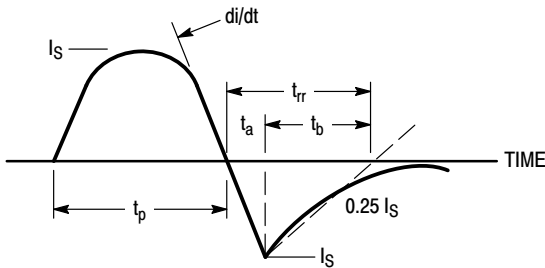
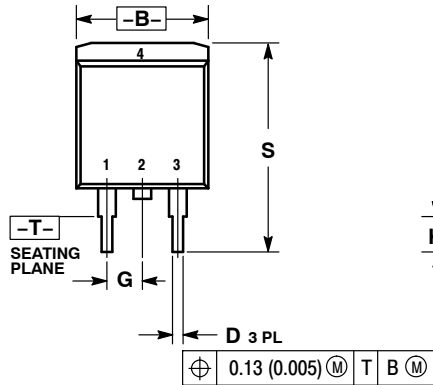


Figure 14. Diode Reverse Recovery Waveform

# NTB5605P, NTB5605

## PACKAGE DIMENSIONS

### D<sup>2</sup>PAK 3 CASE 418B-04 ISSUE K



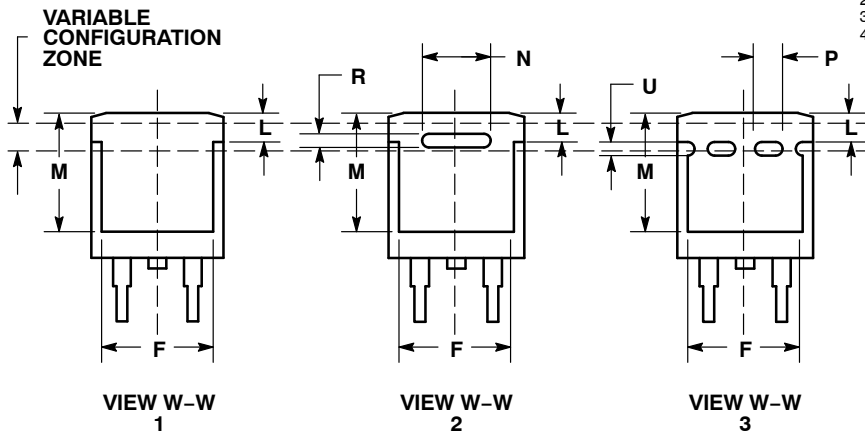
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

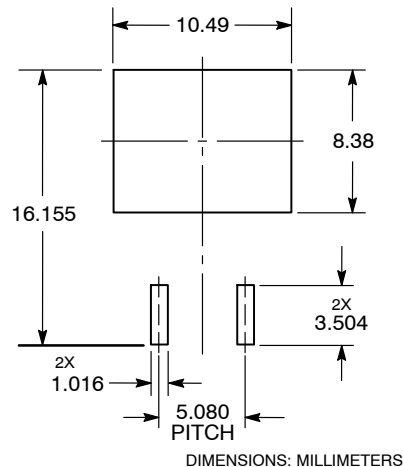
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

**STYLE 2:**

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN




### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NTB5605P, NTBV5605

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local  
Sales Representative