CMOS 8-BIT MICROCONTROLLERS
TMP90C802P/TMP90C802M

1. OUTLINE AND CHARACTERISTICS

The TMP90C802 is a high-speed advanced 8-bit micro controller applicable to a variety of equipment.

With its 8-bit CPU, ROM, RAM, timer/event counter and general-purpose serial interface integrated into a single CMOS chip, the TMP90C802 allows the expansion of external memories (up to 56K byte).

The TMP90C802P is in a DIP package.

The TMP90C802M is in a SOP (Small Outline Package).

The characteristics of the TMP90C802 include:

(1) Powerful instructions : 163 basic instructions, including
Multiplication, division, 16-bit arithmetic operations, bit manipulation instructions

(2) Minimum instruction executing time: 320 ns (at 12.5 MHz oscillation frequency)

(3) Internal ROM: 8K byte

(4) Internal RAM: 128 byte

(5) Memory expansion
External memory: 56K byte

(6) General-purpose serial interface (1 channel)
Asynchronous mode, I/O interface mode

(7) 8-bit timers (4 channels) : (1 external clock input)

(8) Port with zero cross detection circuit (1 input)

(9) Input/Output ports (32 pins)

(10) Interrupt function: 8 internal interrupts and 3 external interrupts

(11) Micro Direct Memory Access (DMA) function (4 channels)

(12) Watchdog timer

(13) Standby function (4 HALT modes)

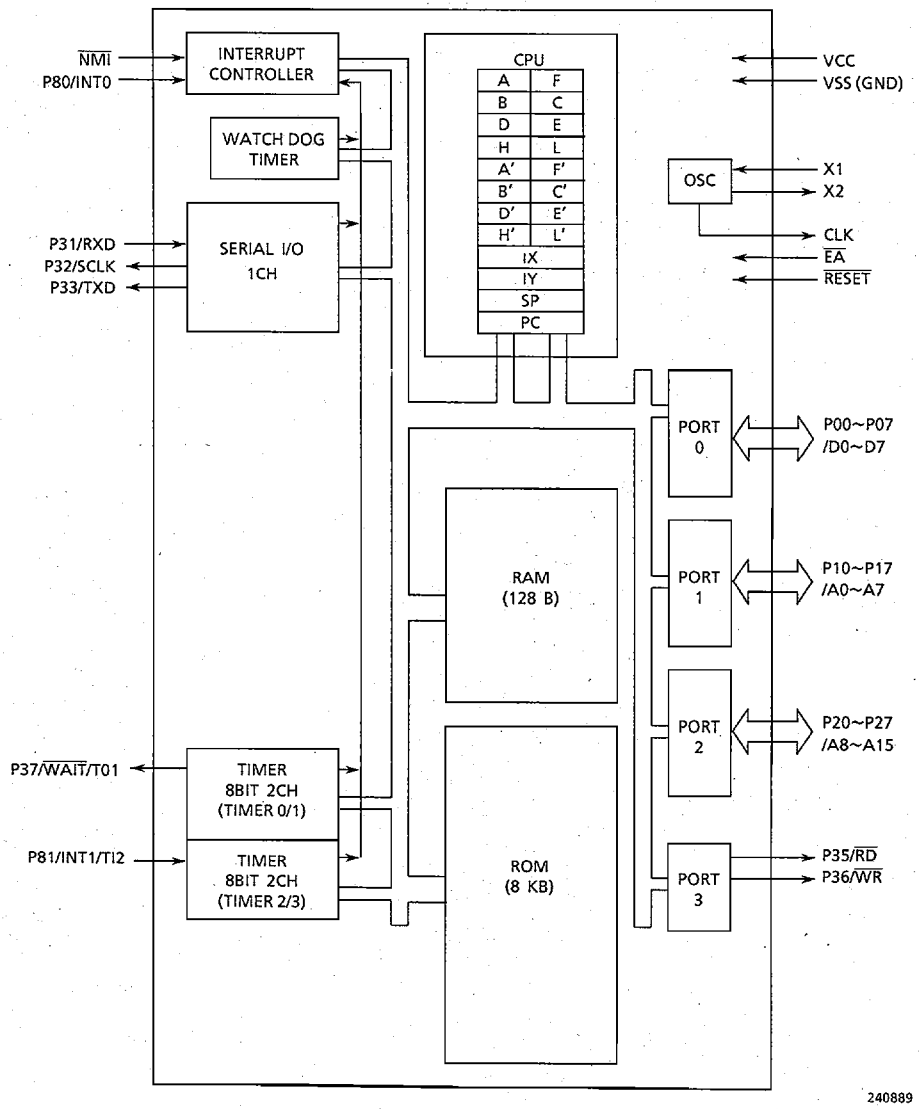

Figure 1 TMP90C802 Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input/output pins, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of the TMP90C802.

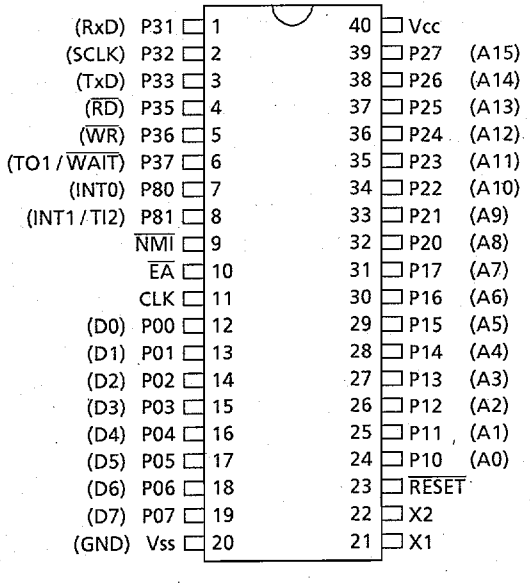

Figure 2.1 Pin Assignment

2.2 Pin Names and Functions

The names of input/output pins and their functions are summarized in Table 2.2.

Table 2.2 Pin Names and Functions (1/2)

Pin Name	No. of pins	I/O 3 states	Function
P00~P07	8	I/O	Port 0: 8-bit I/O port that allows selection of input/output on byte basis
/D0~D7		3 states	Data bus: Also functions as 8-bit bidirectional data bus for external memory
P10~P17	8	I/O	Port 1: 8-bit I/O port that allows selection on byte basis
/A0~A7		Output	Address bus: The lower 8 bits address bus for external memory
P20~P27	8	I/O	Port 2: 8-bit I/O port that allows selection on bit basis
/A8~A15		Output	Address bus: The upper 8 bits address bus for external memory
P31	1	Input	Port 31: 1-bit input port
/RxD			Receives Serial Data
P32	1	Output	Port 32: 1-bit output port
/SCLK			Serial clock output
P33	1	Output	Port 33: 1-bit output port
/TxD			Transmittes Serial Data
P35	1	Output	Port 35: 1-bit output port
/$\overline{RD}$			Read: Generates strobe signal for reading external memory
P36	1	Output	Port 36: 1-bit output port
/$\overline{WR}$			Write: Generates strobe signal for writing into external memory
P37	1	Input	Port 37: 1-bit input port
/$\overline{WAIT}$			Wait: Input pin for connecting slow speed memory or peripheral LSI
/TO1		Output	Timer output 1: Output of Timer 0 or 1
P80	1	Input	Port 80: 1-bit input port
/INT0			Interrupt request pin 0: interrupt request pin (Level/rising edge is programmable)
P81	1	Input	Port 81: 1-bit input port
/INT1			Interrupt request pin 1: interrupt request pin (Rising edge)
/TI2			Timer input 2: Counter input signal for Timer 2
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Falling edge interrupt request pin
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is pulled up internally during resetting.
$\overline{EA}$	1	Input	External access: Connects with Vcc pin in the TMP90C802 using internal ROM.

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Table 2.2 Pin Names and Functions (2/2)

Pin Name	No. of pins	I/O 3 states	Function
$\overline{\text{RESET}}$	1	Input	Reset : Initializes the TMP90C802 (Built in pull-up resister)
X1/X2	2	Input/ Output	Pin for quartz crystal or ceramic resonator (1~12.5MHz)
Vcc	1		Power supply (+ 5V)
Vss (GND)	1		Ground (0V)

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3. MEMORY MAP

The TMP90C802 supports a program or data memory of up to 64K bytes.
The program/data memory may be assigned to the address space from 0000H to FFFFH.

(1) Internal ROM

The TMP90C802 internally contains an 8Kbyte ROM. The address space 0000H~1FFFH is provided to the ROM. The CPU starts executing a program from 0000H by resetting.

The addresses 0010H~007FH in this internal ROM area are used for the entry area for the interrupt processing.

(2) Internal RAM

The TMP90C802 also contains a 128byte RAM, which is allocated to the address space FF00H~FF7FH. The CPU allows the access to whole RAM area (FF00H~FF7FH, 128 bytes) by a short operation code (opcode) in a "direct addressing mode".

The addresses from FF30H~FF7FH in this RAM area can be used as parameter area for micro DMA processing (and for any other purposes when the micro DMA function is not used).

(3) Internal I/O

The TMP90C802 provides a 48byte address space as an internal I/O area, whose addresses range from FFC0H~FFEFH. This I/O area can be accessed by the CPU using a short opcode in the "direct addressing mode".

Figure 3 is a memory map indicating the areas accessible by the CPU in the respective addressing mode.

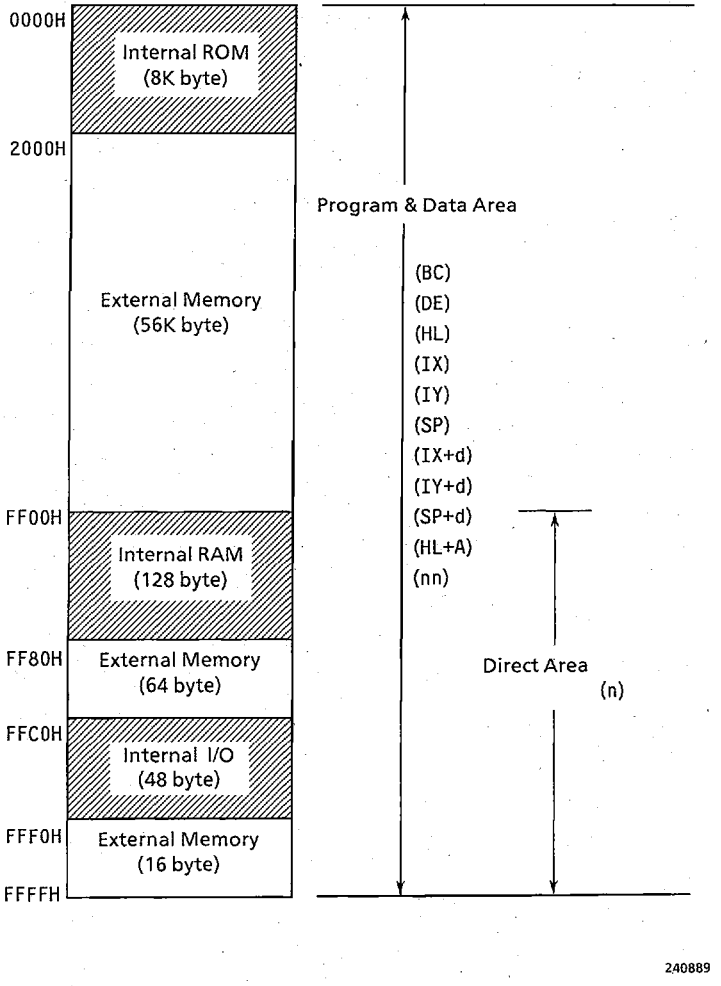

Figure 3 Memory Map

4. ELECTRICAL CHARACTERISTICS

TMP90C802P/TMP90C802M

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	−0.5~+7	V
V_{IN}	Input voltage	−0.5~V_{CC}+0.5	V
P_D	Power dissipation (Ta = 85°C)	250	mW
T_{SOLDER}	Soldering temperature (10Sec)	260	℃
T_{STG}	Storage temperature	−65~150	℃
T_{OPR}	Operating temperature	−40~85	℃

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4.2 DC Characteristics

Vcc = 5V ± 10% TA = −40~85°C (1~10MHz)
TA = −20~70°C (1~12.5MHz)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (P0)	−0.3	0.2Vcc−0.1	V	
V_{IL1}	P1, P2, P3, P8	−0.3	0.3Vcc	V	
V_{IL2}	$\overline{RESET}$, INT0, $\overline{NMI}$	−0.3	0.25Vcc	V	
V_{IL3}	$\overline{EA}$	−0.3	0.3	V	
V_{IL4}	X1	−0.3	0.2Vcc	V	
V_{IH}	Input High Voltage (P0)	0.2Vcc+1.1	Vcc+0.3	V	
V_{IH1}	P1, P2, P3, P8	0.7Vcc	Vcc+0.3	V	
V_{IH2}	$\overline{RESET}$, INT0, $\overline{NMI}$	0.75Vcc	Vcc+0.3	V	
V_{IH3}	$\overline{EA}$	Vcc−0.3	Vcc+0.3	V	
V_{IH4}	X1	0.8Vcc	Vcc+0.3	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6mA
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 0.75Vcc 0.9Vcc		V V V	I_{OH} = −400μA I_{OH} = −100μA I_{OH} = −20μA
I_{DAR}	Darlington Drive Current (8 I/O pins) (Note)	−1.0	−3.5	mA	V_{EXT} = 1.5V R_{EXT} = 1.1 kΩ
I_{LI}	Input Leakage Current	0.02 (Typ)	±5	μA	0.0≦Vin≦Vcc
I_{LO}	Output Leakage Current	0.05 (Typ)	±10	μA	0.2≦Vin≦Vcc−0.2
I_{CC}	Operating Current (RUN) Idle 1 Idle 2	17 (Typ) 1.5 (Typ) 6 (Typ)	30 5 15	mA mA mA	tosc = 10MHz (25% Up @12.5MHz)
	STOP (TA = −40~85°C) STOP (TA = 0~50°C)		50 10	μA μA	0.2≦Vin≦Vcc−0.2
V_{STOP}	Power Down Voltage (@STOP)	2 RAM BACK UP	6	V	V_{IL2} = 0.2Vcc, V_{IH2} = 0.8Vcc
R_{RST}	$\overline{RESET}$ Pull Up Registor	50	150	KΩ	
CIO	Pin Capacitance		10	pF	testfreq = 1MHz
V_{TH}	Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0	0.4	1.0 (Typ)	V	

Note : I_{DAR} is guaranteed for a total of up to 8 optional ports.

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4.3 AC Characteristics

Vcc = 5V ± 10% TA = −40~85°C (1~10MHz)
CL = 50pF TA = −20~70°C (1~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{OSC}	OSC. Period = x	80	1000	100		80		ns
t_{CYC}	CLK Period	4x	4x	400		320		ns
t_{WL}	CLK Low width	2x − 40		160		120		ns
t_{WH}	CLK High width	2x − 40		160		120		ns
t_{AC}	Address Setup to $\overline{RD}$, $\overline{WR}$	x − 45		55		35		ns
t_{RR}	$\overline{RD}$ Low width	2.5x − 40		210		160		ns
t_{CA}	Address Hold Time After $\overline{RD}$, $\overline{WR}$	0.5x − 30		20		10		ns
t_{AD}	Address to Valid Data In		3.5x − 95		255		185	ns
t_{RD}	$\overline{RD}$ to Valid Data In		2.5x − 80		170		120	ns
t_{HR}	Input Data Hold After $\overline{RD}$	0		0		0		ns
t_{WW}	$\overline{WR}$ Low width	2.5x − 40		210		160		ns
t_{DW}	Data Setup to $\overline{WR}$	2x − 50		150		110		ns
t_{WD}	Data Hold After $\overline{WR}$	30	90	30	90	30	90	ns
t_{CWA}	$\overline{RD}$, $\overline{WR}$ to Valid $\overline{WAIT}$		1.5x − 100		50		20	ns
t_{AWA}	Address to Vaild $\overline{WAIT}$		2.5x − 130		120		70	ns
t_{WAS}	$\overline{WAIT}$ Setup to CLK	70		70		70		ns
t_{WAH}	$\overline{WAIT}$ Hold After CLK	0		0		0		ns
t_{RV}	$\overline{RD}$, $\overline{WR}$ Recovery Time	1.5x − 35		115		85		ns
t_{CPW}	CLK to Port Data Output		x + 200		300		280	ns
t_{PRC}	Port Data Setup to CLK	200		200		200		ns
t_{CPR}	Port Data Hold After CLK	100		100		100		ns
t_{CHCL}	$\overline{RD}$ / $\overline{WR}$ Hold After CLK	x − 60		40		20		ns
t_{CLC}	$\overline{RD}$ / $\overline{WR}$ Setup to CLK	1.5x − 50		100		70		ns
t_{CLHA}	Address Hold After CLK	1.5x − 80		70		40		ns
t_{ACL}	Address Setup to CLK	2.5x − 80		170		120		ns
t_{CLD}	Data Setup to CLK	x − 50		50		30		ns

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- AC output level High 2.2V/Low 0.8V
- AC input level High 2.4V/Low 0.45V (D0~D7)
  High 0.8Vcc/Low 0.2Vcc (excluding D0~D7)

4.4 Zero- Cross Characteristics

Vcc = 5V ± 10% TA = −40~85°C (1~10MHz)
TA = −20~70°C (1~12.5MHz)

Symbol	Parameter	Condition	Min	Max	Unit
Vzx	Zero- cross detection input	AC coupling C = 0.1μF	1	1.8	VAC p − p
Azx	Zero- cross accuracy	50/60Hz sine wave		135	mV
Fzx	Zero- cross detection input frequency		0.04	1	KHz

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4.5 Serial Channel Timing − I/O Interface Mode

Vcc = 5V ± 10% TA = −40~85°C (1~10MHz)
CL = 50pF TA = −20~70°C (1~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Units
		Min	Max	Min	Max	Min	Max	
t_{SCY}	Serial Port Clock Cycle Time	8x		800		640		ns
t_{OSS}	Output Data Setup SCLK Rising Edge	6x − 150		450		330		ns
t_{OHS}	Output Data Hold After SCLK Rising Edge	2x − 120		80		40		ns
t_{HSR}	Input Data Hold After SCLK Rising Edge	0		0		0		ns
t_{SRD}	SCLK Rising Edge to Input DATA Valid		6x − 150		450		330	ns

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4.6 8-bit Event Counter

Vcc = 5V ± 10% TA = −40~85°C (1~10MHz)
TA = −20~70°C (1~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Units
		Min	Max	Min	Max	Min	Max	
t_{VCK}	TI2 clock cycle	8x + 100		900		740		ns
t_{VCKL}	TI2 Low clock pulse width	4x + 40		440		360		ns
t_{VCKH}	TI2 High clock pulse width	4x + 40		440		360		ns

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4.7 Interrupt Operation

Vcc = 5V ± 10% TA = −40~85℃ (1~10MHz)
TA = −20~70℃ (1~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Units
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Low level pulse width (⎍)	4x		400		320		ns
t_{INTAH}	$\overline{NMI}$, INT0 High level pulse width (⎍)	4x		400		320		ns
t_{INTBL}	INT1 Low level pulse width (⎍)	8x + 100		900		740		ns
t_{INTBH}	INT1 High level pulse width (⎍)	8x + 100		900		740		ns

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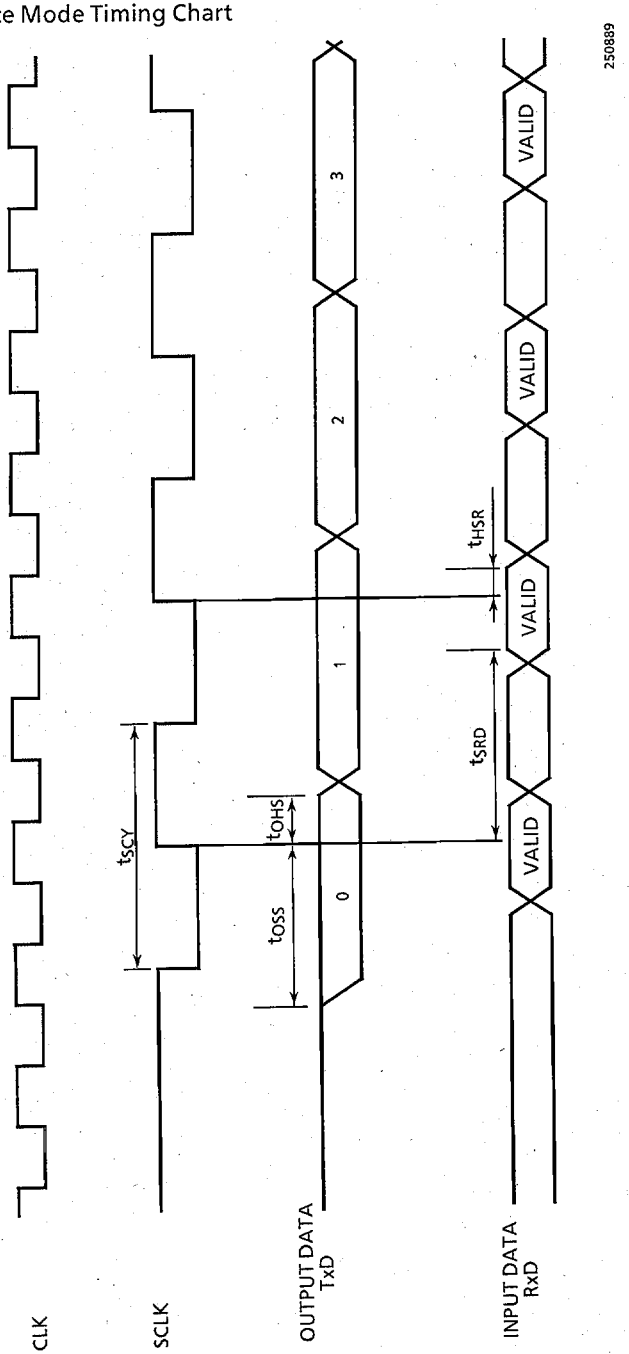
4.8 I/O Interface Mode Timing Chart



4.9 Timing Chart