

FEATURES

- Full Four-Quadrant Multiplication
- On-chip Bus Interface Logic
- +5 V to +15 V Operation
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)
- PDIP, CDIP, SOIC & PLCC Packages Available

APPLICATIONS

- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments

GENERAL DESCRIPTION

The MP7524 is a low cost, 8-bit CMOS Digital-to-Analog Converter designed for direct interface to most microprocessors.

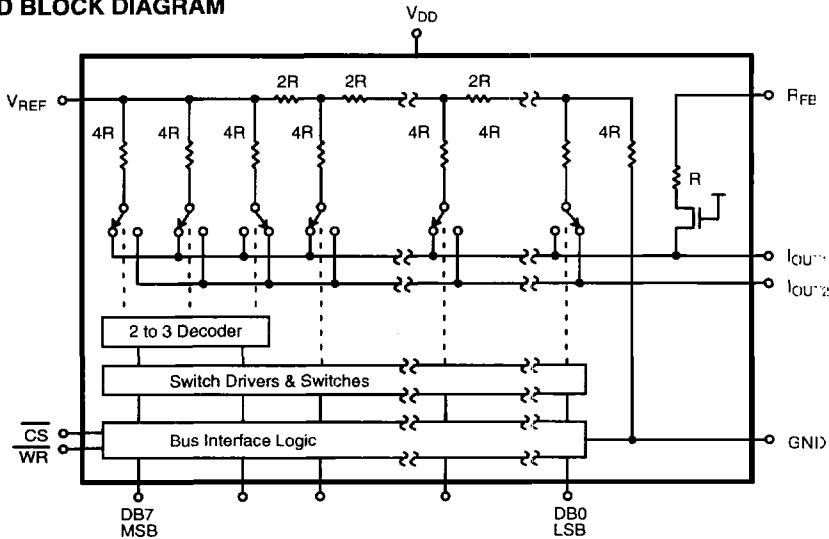
Basically an 8-bit DAC with input latches, the MP7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the MP7524 provides accuracy to 1/8 LSB with power dissipation of only 10mW.

Featuring operation from +5 V to +15 V, the MP7524 interfaces directly to most microprocessor buses or output ports. Excellent multiplying characteristics (2- or 4-quadrant) make the MP7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

Specified for operation over the commercial / industrial (-40 to +85°C) and military (-55 to +125°C) temperature ranges, the MP7524 is available in Plastic (PDIP) and Ceramic (CDIP) dual-in-line, Surface Mount (SOIC) and Plastic Leaded Chip Carrier (PLCC) packages.

4

SIMPLIFIED BLOCK DIAGRAM

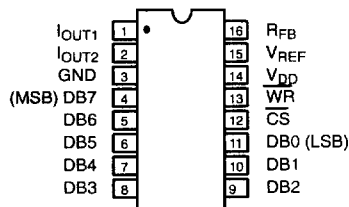


**3 Segment D/A Converter with Termination to GND
 Logical "1" at Digital Input Steers Current to IOUT1**

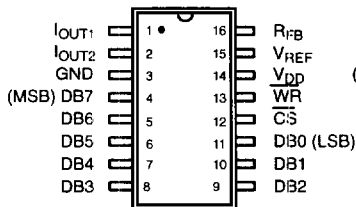
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	-40 to +85°C	MP7524JN	±1/2	±1	±1.4%
Plastic Dip	-40 to +85°C	MP7524KN	±1/4	±1	±1.4%
Plastic Dip	-40 to +85°C	MP7524LN	±1/8	±1	±1.4%
SOIC (Narrow)	-40 to +85°C	MP7524JR	±1/2	±1	±1.4%
SOIC (Narrow)	-40 to +85°C	MP7524KR	±1/4	±1	±1.4%
SOIC (Wide)	-40 to +85°C	MP7524JS	±1/2	±1	±1.4%
SOIC (Wide)	-40 to +85°C	MP7524KS	±1/4	±1	±1.4%
SOIC (Wide)	-40 to +85°C	MP7524LS	±1/8	±1	±1.4%
PLCC	-40 to +85°C	MP7524JP	±1/2	±1	±1.4%
PLCC	-40 to +85°C	MP7524KP	±1/4	±1	±1.4%
PLCC	-40 to +85°C	MP7524LP	±1/8	±1	±1.4%
Ceramic Dip	-40 to +85°C	MP7524AD	±1/2	±1	±1.4%
Ceramic Dip	-40 to +85°C	MP7524BD	±1/4	±1	±1.4%
Ceramic Dip	-40 to +85°C	MP7524CD	±1/8	±1	±1.4%
Ceramic Dip	-55 to +125°C	MP7524SD	±1/2	±1	±1.4%
Ceramic Dip	-55 to +125°C	MP7524SD/883	±1/2	±1	±1.4%
Ceramic Dip	-55 to +125°C	MP7524TD	±1/4	±1	±1.4%
Ceramic Dip	-55 to +125°C	MP7524TD/883	±1/4	±1	±1.4%
Ceramic Dip	-55 to +125°C	MP7524UD	±1/8	±1	±1.4%
Ceramic Dip	-55 to +125°C	MP7524UD/883	±1/8	±1	±1.4%

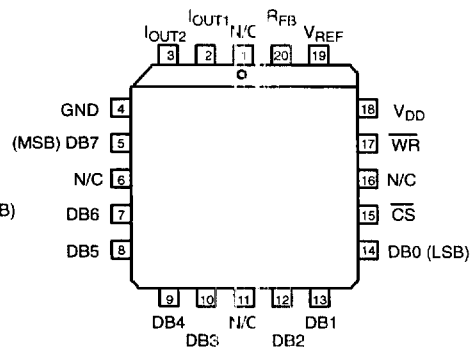
PIN CONFIGURATIONS



16 Pin CDIP, PDIP (0.300")
D16, N16



16 Pin SOIC
(Jedec, 0.150" & 0.300")
SN16, S16



20 Pin PLCC
P:20



PIN OUT DEFINITIONS

CDIP, PDIP and SOIC

PIN NO.	NAME	DESCRIPTION
1	I _{OUT1}	Current Output 1
2	I _{OUT2}	Current Output 2
3	GND	Ground
4	DB7	Data Bit 7 (MSB)
5	DB6	Data Bit 6
6	DB5	Data Bit 5
7	DB4	Data Bit 4
8	DB3	Data Bit 3
9	DB2	Data Bit 2
10	DB1	Data Bit 1
11	DB0	Data Bit 0 (LSB)
12	\overline{CS}	Chip Select
13	\overline{WR}	Write
14	V _{DD}	Power Supply
15	V _{REF}	Reference Input
16	R _{FB}	Feedback Resistance

PLCC

PIN NO.	NAME	DESCRIPTION
1	N/C	No Connection
2	I _{OUT1}	Current Output 1
3	I _{OUT2}	Current Output 2
4	GND	Ground
5	DB7	Data Bit 7 (MSB)
6	N/C	No Connection
7	DB6	Data Bit 6
8	DB5	Data Bit 5
9	DB4	Data Bit 4
10	DB3	Data Bit 3
11	N/C	No Connection
12	DB2	Data Bit 2
13	DB1	Data Bit 1
14	DB0	Data Bit 0 (LSB)
15	\overline{CS}	Chip Select
16	N/C	No Connection
17	\overline{WR}	Write
18	V _{DD}	Power Supply
19	V _{REF}	Reference Input
20	R _{FB}	Feedback Resistance

ELECTRICAL CHARACTERISTICS

($V_{DD} = +5\text{ V}$, $V_{REF} = +10\text{ V}$ unless otherwise noted)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
STATIC PERFORMANCE (1)								
Resolution (All Grades)	N	8			8		Bits	FSR = Full Scale Range
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL - Min INL) / 2
J, A, S								
K, B, T								
L, C, U								
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S								
K, B, T								
L, C, U								
Gain Error	GE						% FSR	Using Internal F_{FB} Digital Inputs = V_{INH}
Power Supply Rejection Ratio	PSRR						ppm/%	$ \Delta\text{Gain}/\Delta V_{DD} \cdot \Delta V_{DD} = \pm 10\%$ Digital Inputs = V_{INH}
Output Leakage Current (Pin 1)	I_{OUT1}						nA	Digital Inputs = V_{NL}
DYNAMIC PERFORMANCE								
Current Settling Time (2)	t_S						ns	RL = 100Ω, $C_L = 10\text{ pF}$
AC Feedthrough at I_{OUT1} (2)	F_T						LSB	Full Scale Charge to 1/2 LSB $V_{REF} = 100\text{ kHz}$, 20 Vp-p, sinewave DB0-DB7 = C, $V_{CS} = WR = 0\text{ V}$
at I_{OUT2}							LSB	
REFERENCE INPUT								
Input Resistance	R_{IN}						kΩ	
DIGITAL INPUTS (3)								
Logical "1" Voltage	V_{IH}						V	$V_{IN} = 0\text{ V}$
Logical "0" Voltage	V_{IL}						V	
Input Leakage Current	I_{LKG}						μA	
Input Capacitance (2)	C_{IN}						pF	
ANALOG OUTPUTS (2)								
Output Capacitance	C_{OUT1}						pF	DAC Inputs all C's DAC Inputs all C's DAC Inputs all C's DAC Inputs all C's
	C_{OUT1}						pF	
	C_{OUT2}						pF	
	C_{OUT2}						pF	
POWER SUPPLY (5)								
Supply Current	I_{DD}						mA	All digital inputs = 0 V or all = 5 V All digital inputs = V_{IL} or all = V_{IH}
							mA	



ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C			Tmin to Tmin	Tmax to Tmax	Units	Test Conditions/Comments
		Min	Typ	Max				
SWITCHING CHARACTERISTICS (2, 4)								
Chip Select to Write Set-Up Time J, K, L, A, B, C S, T, U	t _{CS}	170			220		ns	
		170			240			
Chip Select to Write Hold Time	t _{CH}	0			0		ns	
Data Valid to Write Set-Up Time	t _{DS}	135			170		ns	
Data Valid to Write Hold Time	t _{DH}	10			10		ns	
Write Pulse Width J, K, L, A, B, C S, T, U	t _{WR}	170			220		ns	
		170			240			

NOTES:

- (1) Full Scale Range (FSR) is 10V for unipolar mode.
- (2) Guaranteed but not production tested .
- (3) Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- (4) See timing diagram.
- (5) Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS (VDD = + 15 V, VREF = +10 V unless otherwise noted)

Parameter	Symbol	25°C		Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min		
STATIC PERFORMANCE (1)							
Resolution (All Grades)	N	8			8	Bits	FSR = Full Scale Range
Integral Non-Linearity (Relative Accuracy) J, A, S K, B, T L, C, U	INL			±1/2 ±1/4 ±1/8		LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
Differential Non-Linearity J, A, S K, B, T L, C, U	DNL			±1 ±1 ±1		LSB	All grades monolithic over full temperature range.
Gain Error	GE			±0.5		% FSR	Using Internal R _{FB} Digital Inputs = V _{NH}
Power Supply Rejection Ratio	PSRR			±200		ppm/%	ΔGain/ΔV _{DD} ΔV _{DD} = ± 10% Digital Inputs = V _{NH}
Output Leakage Current (Pin 1)	I _{OUT1}			±50nA		nA	Digital Inputs = V _{NL}
DYNAMIC PERFORMANCE							
Current Settling Time (2)	t _S			50		ns	RL=100Ω, CL= 3pF
AC Feedthrough at I _{OUT1} (2) at I _{OUT2}	FT			±1/2 ±1/2		LSB LSB	Full Scale Change to 1/2 LSB V _{REF} =100kHz, 20Vp-p, sinewave DB0 - DB7 = 0 V, CS = WR = 0 V
REFERENCE INPUT							
Input Resistance	R _{IN}	5		20	5	20	kΩ
DIGITAL INPUTS (3)							
Logical "1" Voltage	V _{IH}	+13.5			+13.5		V
Logical "0" Voltage	V _{IL}			+1.5		+1.5	V
Input Leakage Current	I _{LKG}			±1		±10	μA
Input Capacitance (2)	C _{IN}			20		20	pF
ANALOG OUTPUTS (2)							
Output Capacitance	C _{OUT1} C _{OUT1} C _{OUT2} C _{OUT2}			70 30 20 60		70 30 20 60	pF pF pF pF
							DAC Inputs a 11 s DAC Inputs a 10 s DAC Inputs a 11 s DAC Inputs a 10 s
POWER SUPPLY							
Supply Current	I _{DD}		1	2		2	mA mA
			1	2		2	All digital inputs = 0 V or all = 15 V All digital inputs = V _{IL} or all = V _{IH}



ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
SWITCHING CHARACTERISTICS (2, 4)								
Chip Select to Write Set-Up Time J, K, L, A, B, C S, T, U	t _{CS}	100			130		ns	
Chip Select to Write Hold Time	t _{CH}	0			0		ns	
Data Valid to Write Set-Up Time J, K, L, A, B, C S, T, U	t _{DS}	60			80		ns	
Data Valid to Write Hold Time	t _{DH}	60			100		ns	
Write Pulse Width J, K, L, A, B, C S, T, U	t _{WR}	10			10		ns	
		100			130		ns	
		100			150			

NOTES:

- (1) Full Scale Range (FSR) is 10V for unipolar mode.
- (2) Guaranteed but not production tested.
- (3) Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- (4) See timing diagram.
- (5) Specified values guarantee functionality. Refer to other parameters for accuracy.

4

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2) (TA = +25°C unless otherwise noted)

V _{DD} to GND	-0.5, +17 V	Storage Temperature	-65°C to +150°C
Digital Input Voltage to GND (2)	GND -0.5 to V _{DD} +0.5 V	Lead Temperature (Soldering, 10 seconds)	+300°C
I _{OUT1} , I _{OUT2} to GND	-0.5 to 7 V	Package Power Dissipation Rating to 75°C	
V _{REF} to GND	±25 V	CDIP, PDIP, SOIC, PLCC	700mW
V _{RFB} to GND	±25 V	Derates above 75°C	10mW/°C

NOTES:

- (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- (2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

APPLICATION NOTES

Refer to Section 8 for Applications Information

INTERFACE LOGIC INFORMATION

Mode Selection

MP7524 mode selection is controlled by the \overline{CS} and \overline{WR} inputs.

Write Mode

When \overline{CS} and \overline{WR} are both LOW, the MP7524 is in the WRITE mode, and the MP7524 analog circuit responds to data activity at the DB0-DB7 data bus inputs. In this mode, the MP7524 acts like a non-latched input D/A converter.

Hold Mode

When either \overline{CS} or \overline{WR} is HIGH, the MP7524 is in the HOLD mode. The MP7524 analog output holds the value corresponding to the last digital input present at DB0-DB7 prior to \overline{WR} or \overline{CS} assuming the high state.

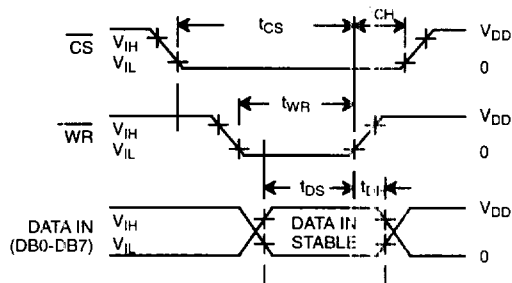


Figure 1. Write Cycle Timing Diagram

\overline{CS}	\overline{WR}	Mode	DAC Response
L	L	Write	DAC responds to data bus (DB0-DB7) inputs
H	X	Hold	Data Bus (DB0-DB7) is locked out
X	H	Hold	DAC holds last data present when \overline{WR} assumed HIGH state

L = LOW state, H = HIGH state, X = Don't care state

Table 1. Mode Selection Table

MICROPROCESSOR INTERFACE

MP7524/8080A Interface

Figure 2. shows the MP7524 used in the MCS-80 microcomputer system as a Memory Mapped Output Device. The basic CPU group consists of the 8080A CPU, 8224 clock generator and 8228 system controller/bus driver. The MP7524 \overline{WR} input is connected to the 8228 system data bus outputs. The \overline{CS} input is connected to the system address decoding

logic. Note that pull-up resistors R3 and R4 are required to ensure that the \overline{CS} and \overline{WR} input HIGH states reach 3.0V min. Pull-ups are not required on the system data bus since the 8228 VOH is 3.6 V min for DB0-DB7.

System timing is shown in Figure 3. Data is loaded into the MP7524 when the \overline{WR} and \overline{CS} inputs are both LOW. The data is latched into the MP7524 when \overline{WR} returns HIGH. MP7524 updating is accomplished by using any of the 8080A memory write instructions (such as MOV M, r).

The MP7524 can also be addressed and loaded as an isolated Output Device by connecting the MP7524 \overline{WR} input to the 8228 $\overline{I/O}$ terminal (instead of MEMW).

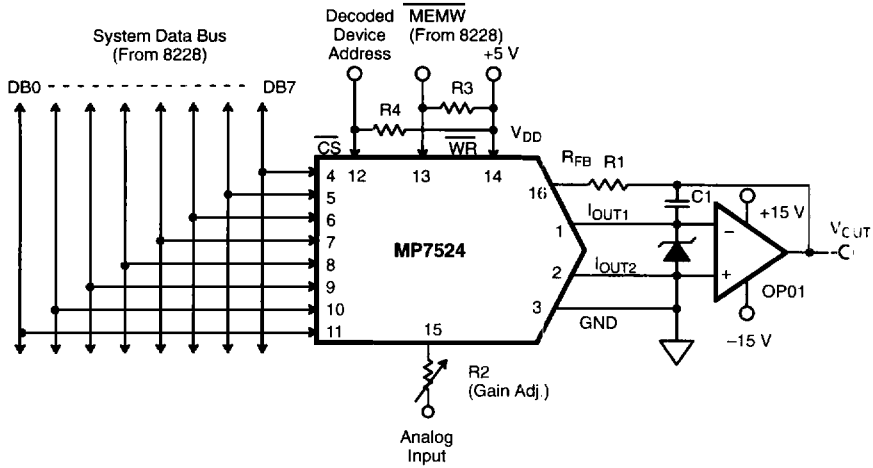


Figure 2. MP7524/8080A Interface

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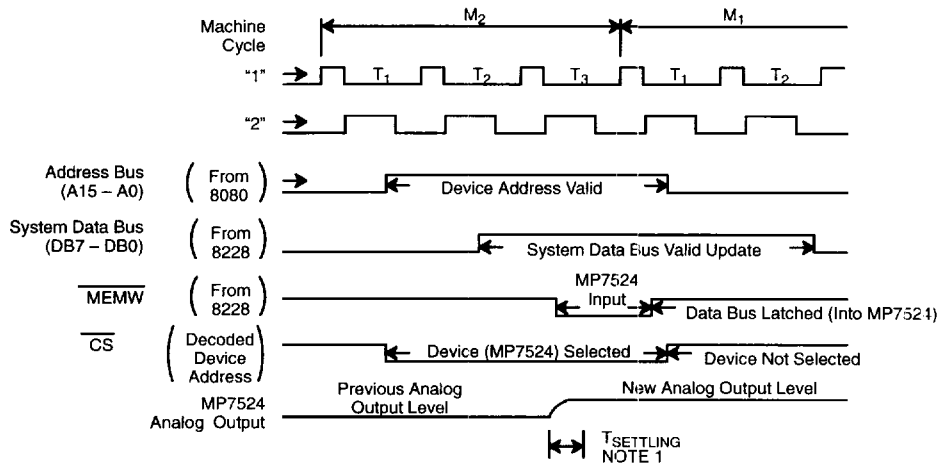


Figure 3. Timing Diagram

NOTE:
1. Settling Time Is Dependent Primarily Upon Output Amplifier Slew Rate And Settling Characteristics. Waveform Shown Is Not Representative Of Any Specific Amplifier