CMOS HIGH SPEED GATE ARRAYS
Preliminary

DESCRIPTION

The SLA9000 Series is a family of sea-of-gates arrays manufactured on S-MOS' state-of-the-art 1.0 micron double-metal SiCMOS process. The series consists of 11 arrays ranging from 1,978 to 14,690 usable gates and from 86 to 226 I/O. The SLA9000 Series has been tailored for high performance designs with typical gate delays of .65 nanoseconds. Additionally, high-speed silicon efficient RAM functions are offered as customized cells. The series has a selectable output drive capability of 2, 6, 12 or 24 milliamps (two output buffers can be used in parallel to obtain 48 milliamps). The arrays are offered in a wide variety of packages including 80-256 pin quad flat packs. The SLA9000 Series is supported by S-MOS' own design system with NavNet schematic editor, as well as most major CAD systems including Mentor, Valid, Viewlogic, FutureNet, Synopsys/Verilog and OrCAD.

FEATURES

- 1.0 micron drawn channel length (N-Channel)
- Very high speed: tpd (2-input power NAND) (typ, FO = 2 & 2mm AL) = .65 ns/gate
- High Drive
  - -24mA for a single output
  - -48mA for parallel outputs
- Low gate-to-pads ratio for high pin count applications
- Megacells compatible
- Fully migratable to S-MOS standard cell families

PRODUCT CONFIGURATION

ARRAY	RAW GATES	USABLE RANGE		TOTAL PADS
		MINIMUM	MAXIMUM	
SLA904S	4395	1978	2417	86
SLA906S	5990	2635	3174	102
SLA908S	7580	3259	3865	112
SLA909S	9358	3930	4679	126
SLA912S	11978	5030	5869	140
SLA915S	14823	6077	7115	156
SLA919S	18802	7708	8837	172
SLA922S	21956	8782	9960	186
SLA926S	25669	10268	11551	198
SLA929S	29162	11664	13123	212
SLA933S	32645	13058	14690	226

*Note: All arrays have 8 power/GND pad included within total pad count.