PROCESS CP326X

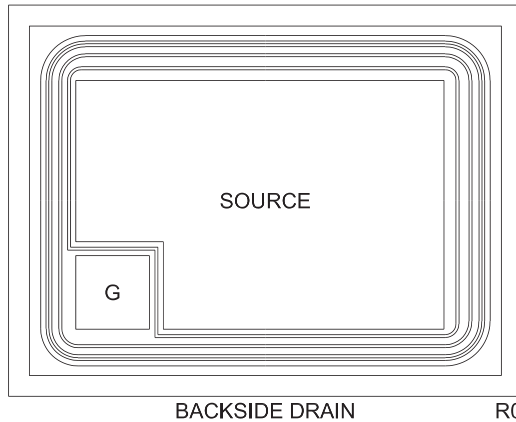
Small Signal MOSFET Transistor

N-Channel Enhancement-Mode Transistor Chip

PROCESS DETAILS

Die Size	33.5 x 25.6 MILS
Die Thickness	5.5 MILS
Gate Bonding Pad Area	4.7 x 4.7 MILS
Source Bonding Pad Area	20 x 12 MILS
Top Side Metalization	Al-Si - 35,000Å
Back Side Metalization	Au - 12,000Å

GEOMETRY



GROSS DIE PER 6 INCH WAFER
28,000

PRINCIPAL DEVICE TYPES
CMLDM7120
CMPDM7120G

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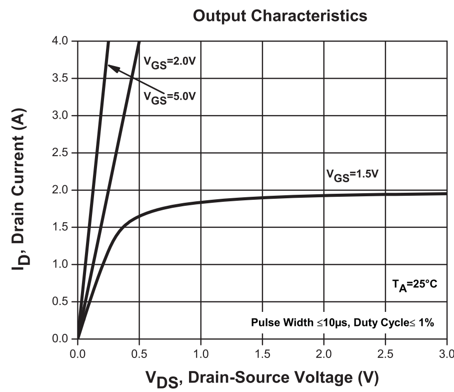
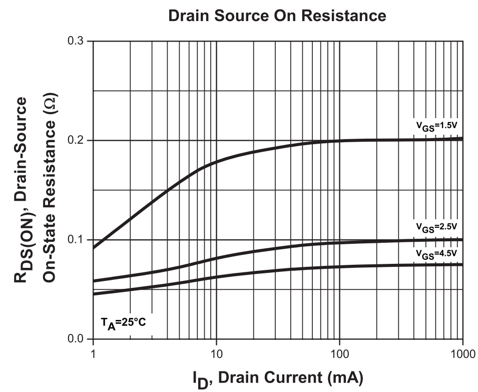
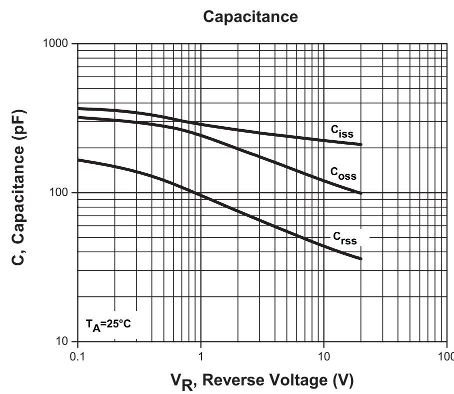
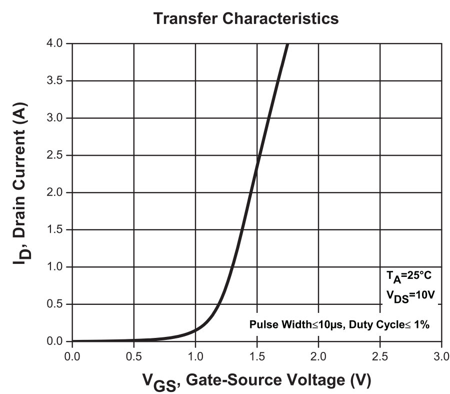
PROCESS CP326X

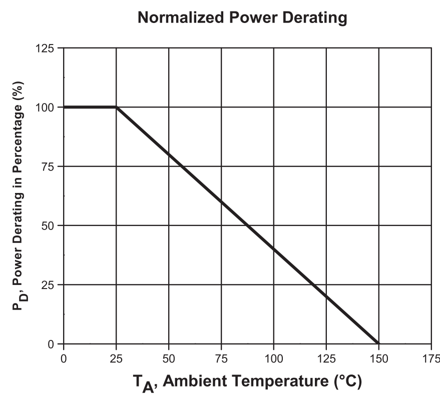
Typical Electrical Characteristics











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