64 x 4-bit FIFO
64 x 5-bit FIFO

L8C401/403
L8C402/404

FEATURES

- First-In/First Out (FIFO) using Dual-Port Memory
- Maximum Shift Rate — 50 MHz
- Asychronous and Simultaneous Read and Write
- Fully Expandable by both Word Depth and/or Bit Width
- Fast Bubble-Through Time – 16 ns
- Output Enable Available on L8C403 and L8C404
- Plug Compatible with IDT7240x, Cypress CY7C40x
- Package Styles Available:
  - 16/18-pin Plastic DIP
  - 16/18-pin CerDIP
  - 16/18-pin Plastic SOIC
  - 20-pin Plastic LCC
  - 20-pin Ceramic LCC

DESCRIPTION

The **L8C401, L8C402, L8C403,** and **L8C404** are dual-port First-In/First-Out (FIFO) memories. The FIFO memory products are organized as:

L8C401 – 64 × 4-bit
L8C402 – 64 × 5-bit
L8C403 – 64 × 4-bit with $\overline{OE}$
L8C404 – 64 × 5-bit with $\overline{OE}$

Data is shifted into the FIFO through 4-bit or 5-bit Data Input (D_0–D_3, D_4) pins on the rising edge of the Shift In (SI) signal. The stored data stack up at the Data Output (Q_0–Q_3, Q_4) pins in the same order as it entered. When the Shift Out (SO) signal is LOW, data at the next to last word shifts to the output while all other data shift down one location in the stack. The Input Ready (IR) signal acts as a flag to indicate whether the input is ready to accept new data (IR = HIGH), or to indicate when the FIFO is full (IR = LOW). The Output Ready (OR) signal acts as a flag to indicate whether the output contains valid data (OR = HIGH), or to indicate when the FIFO is empty (OR = LOW). The IR and OR signals are also used to provide a signal for cascading.

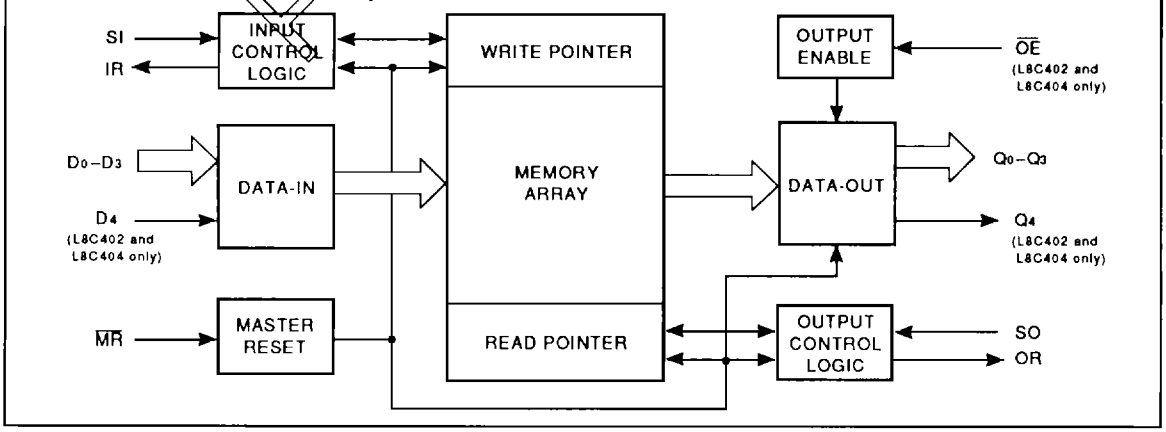
Width expansion is accomplished by logically ANDing the Input Ready (IR) and the Output Ready (OR) signals to form composite signals.

Depth expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready (IR) pin of the receiving device is connected to the Shift Out (SO) pin of the sending device, and the Output Ready (OR) pin of the sending device to the Shift In (SI) pin of the receiving device.

The FIFOs are designed with completely asychronous read and write operations, allowing the FIFO to be used as data buffers between two digital systems of differing operating speeds. The 50 MHz data rate is ideal for high-speed communication and controller applications.

Latchup and static discharge protection is provided on-chip. The FIFOs can withstand an injection current of up to 200 mA on any pin without damage.

L8C401/402/403/404 BLOCK DIAGRAM



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1 and 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
DC voltage applied to outputs in High Z state	−0.5 V to +7.0 V
DC input voltage	−3.0 V to +7.0 V
Power Dissipation	1.0 W
Output current into low outputs	20 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage (V_{CC})
Active Operation, Commercial	0°C to +70°C	5.0 V ±10%
Active Operation, Military	−55°C to +125°C	5.0 V ±10%

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = Min.	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA , V_{CC} = Min.			0.4	V
V_{IH}	Input High Voltage		2.0		6.0	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC} (Note 3)	−10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max. (Note 4)	−20		−90	mA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5 V Output Disabled (L8C403 and L8C404)	−50		+50	µA
I_{CC}	V_{CC} Current	V_{CC} = Max., f = 10 MHz (Notes 5, 6, 13, 14)			35	mA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 4.5 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 8)			7	pF

OPERATING DESCRIPTION

CONCEPT

Unlike traditional FIFOs, these devices are designed using a dual-port memory, read and write pointer, and control logic. The read and write pointers are incremented by the Shift Out (SO) and Shift In (SI) respectively. The availability of an empty space to shift data into is indicated by the Input Ready (IR) signal, while the presence of data at the output is indicated by the Output Ready (OR) signal. The conventional concept of bubble through is absent. Instead the delay for input data to appear at the output is the time required to move a pointer and propagate an Output Ready (OR) signal. The Output Enable ($\overline{OE}$) signal provides the capacity to OR tie multiple FIFOs together on a common bus.

RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty condition signified by the Output Ready (OR) signal being LOW at the same time the Input Ready (IR) signal is HIGH. In this condition, the data outputs (Q_0–Q_3, Q_4) will be in a LOW state.

SHIFT IN (SI) DATA

Data is shifted in on the rising edge of the Shift In (SI) signal. This loads input data into the first word location of the FIFO. On the falling edge of the Shift In (SI) signal, the write pointer is moved to the next word position and the Input Ready (IR) signal goes HIGH indicating the readiness to accept new data. If the FIFO is full, the Input Ready (IR) will remain LOW until a word of data is shifted out.

SHIFT OUT (SO) DATA

Data is shifted out of the FIFO on the falling edge of the Shift Out (SO) signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the Output Ready (OR) signal will go HIGH. If data is not present, the Output Ready (OR) signal will stay LOW indicating the FIFO is empty. Upon the rising edge of Shift Out (SO), the Output Ready (OR) signal goes LOW. Previous data remains on the output until the falling edge of Shift Out (SO).

BUBBLE THROUGH

Two bubble through conditions exists. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the Output Ready (OR) flag goes HIGH indicating valid data at the output.

The second bubble through condition occurs when the device is full. Shifting data out creates an empty location which propagates to the input. After a delay, the Input Ready (IR) flag goes HIGH. If the Shift In (SI) signal is HIGH at this time, data on the input will be shifted in.

APPLICATION OF THE 25–50 MHz FIFOs

Application of the FIFO requires attention to characteristics not easily specified in a data sheet, but necessary for reliable operation under all conditions.

When an empty FIFO is filled with initial information, at maximum "shift in" (SI) frequency, followed by immediate shifting out of the data also at maximum "shift out" (SO) frequency, the designer must be aware of a window of time which follows the initial rising edge of the "output ready" (OR) signal during which the SO signal is not recognized. This condition exists only at high speed operation where more than one SO may be generated inside the prohibited window. This condition does not inhibit the operation of the FIFO at full frequency operation, but rather delays the full 25–50 MHz operation until after the window has passed.

There are several implementation techniques to manage the window so that all SO signals are recognized:

1. The first involves delaying the SO operation such that it does not occur in the critical window. This can be accomplished by causing a delay, initiated by the SI signal only when the FIFO is empty, to inhibit or gate the SO activity. This, however, requires that the SO operation at least temporarily be synchronized with the input SI operation. In synchronous applications, this may well be possible and a valid solution.
2. Another solution not uncommon in synchronous applications is to only begin shifting data out of the FIFO when it is greater than half full. This is a common method of FIFO application, as earlier FIFOs could not be operated at maximum frequency when near full or empty. Although Logic Devices FIFOs do not have this limitation, any system design in this manner will not encounter the window condition described above.
3. The window may also be managed by not allowing the first SO signal to occur until the window in question has passed. This can be accomplished by delaying the SO from the rising edge of the initial "output ready" (OR) signal. This, however, involves the requirement that this only occurs on the first occurrence of data being loaded into the FIFO from any empty condition and therefore requires the knowledge of "input ready" (IR) and (SI) conditions as well as (SO).
4. Handshaking with the OR signal can be a third method of avoiding the window in question. With this technique, the rising edge of SO, or the fact that the SO signal is HIGH, will cause the OR signal to go LOW. The SO signal is not taken LOW again, advancing the internal pointer to the next data, until the OR signal goes LOW. This assures that the SO pulse that is initiated in the window will be automatically extended sufficient time to be recognized.
5. There remains the decision as to what signal will be used to latch the data from the output of the FIFO into the receiving source. The leading edge of the OR signal is most appropriate because data is guaranteed to be stable prior to and after the OR leading edge for each FIFO. This is a solution for any number of FIFOs in parallel.

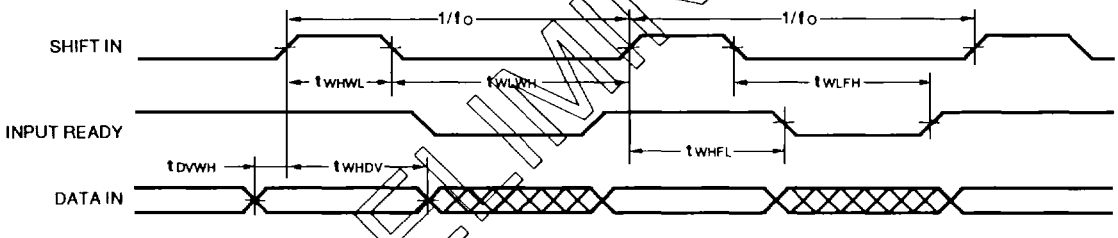
Any of the above solutions will provide a solution for correct operation of a Logic Devices' FIFO at 25–50 MHz. The specific implementation is left to the designer and dependent on the specific application needs.

SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 9)*

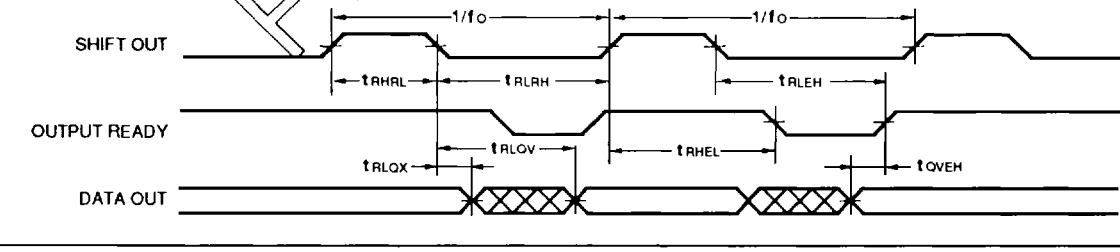
TIMING REFERENCES

Symbol	Parameter	L8C401/402/403/404- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	50 (MHz) Min	50 (MHz) Max
fo	Operating Frequency (in MHz) (Note 17)		15		20		25		35		50
tWHWL	Shift In High to Shift In Low (Note 10)	11		11		11		9		9	
tWLWH	Shift In Low to Shift In High (Note 10)	25		24		24		17		11	
tWLFH	Shift In Low to Input Ready High		40		35		28		20		18
tWHFL	Shift In High to Input Ready Low		35		28		21		18		18
tWHDV	Shift In High to Data Valid (Note 10)	30		25		20		15		13	
tDVWH	Data Valid to Shift In High (Note 10)	0		0		0		0		0	
tRHRL	Shift Out High to Shift Out Low (Note 10)	11		11		11		9		9	
tRLRH	Shift Out Low to Shift Out High	25		24		24		17		11	
tRLEH	Shift Out Low to Output Ready High		40		38		34		20		18
tRHEL	Shift Out High to Output Ready Low		35		28		19		18		18
tRLQV	Shift Out Low to Output Valid (Next Word)		55		45		35		25		17
tRLQX	Shift Out Low to Output Change (Previous Word) (Note 10)	5		5		5		5		5	
tQVEH	Output Valid to Output Ready High (Note 10)	0		0		0		0		0	

INPUT TIMING



OUTPUT TIMING

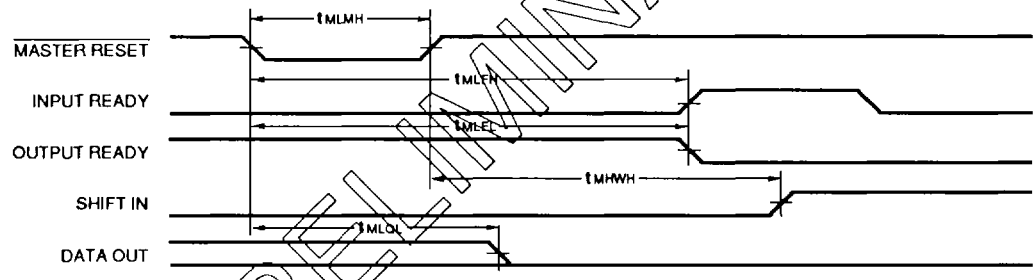


SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 9)*

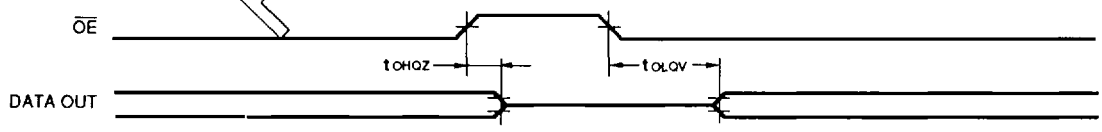
TIMING REFERENCES

Symbol	Parameter	L8C401/402/403/404- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	50 (MHz) Min	50 (MHz) Max
t_{MLMH}	Master Reset Low to Master Reset High (Notes 10, 11)	25		25		25		25		20	
t_{MLFH}	Master Reset Low to Input Ready High		35		35		35		28		25
t_{MLEL}	Master Reset Low to Output Ready Low		35		35		35		28		25
t_{MHWH}	Master Reset High to Shift In High (Note 10)	25		20		10		10		10	
t_{MLQL}	Master Reset Low to Output Low or Zero		35		30		25		20		20
t_{OHQZ}	Output Enable High to Output High Z (Notes 15, 16)		25		20		15		12		12
t_{OLQV}	Output Enable Low to Output Valid (Notes 15, 16)		30		25		20		15		12

MASTER RESET TIMING



OUTPUT ENABLE TIMING

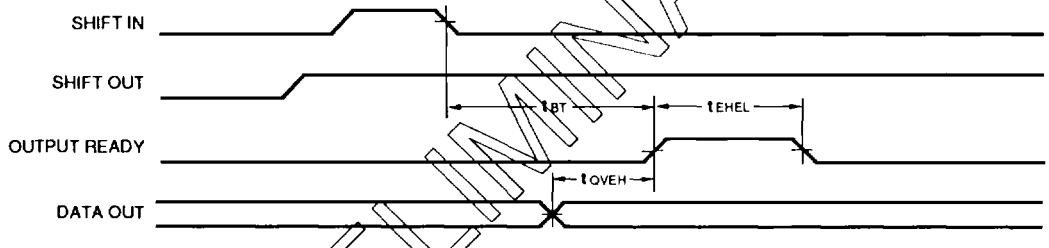


SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 9)*

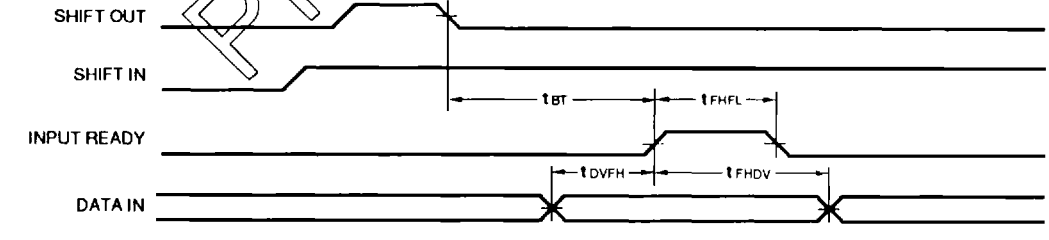
TIMING REFERENCES

Symbol	Parameter	L8C401/402/403/404- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	50 (MHz) Min	50 (MHz) Max
tBT	Bubble Through Time		65		55		40		28		16
tEHEL	Output Ready High to Output Ready Low (Note 18)	9		9		9		9		9	
tOVEH	Output Valid to Output Ready High	0		0		0		0		0	
tFHFL	Input Ready High to Input Ready Low (Note 18)	9		9		9		9		9	
tDVFH	Data Valid to Input Ready High (Note 10)	5		5		5		3		3	
tFHDV	Input Ready High to Data Valid (Note 10)	30		25		20		15		13	

BUBBLE THROUGH, DATA IN TO DATA OUT (CASCADEABLE)



BUBBLE THROUGH, DATA OUT TO DATA IN (CASCADEABLE)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and data inputs changing at the specified read and wrtie cycle rate. The device is neither full or empty for the test.

7. Tested with outputs open in the worst static input control signal combination.

8. These parameters are guaranteed but not 100% tested.

9. Test conditions assume input transition times of 5 ns or less, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{RHRL} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. When cascading devices, the reset pulse width must be increased to equal t_{MLMH} + t_{MLEL}.

12. It is not recommended that Logic Devices and other vendor parts be cascaded together. The parts are designed to be pin-for-pin compatible but temperature and voltage compensation may vary from vendor to vendor. Logic Devices can only guarantee the cascading of Logic Devices parts to other Logic Devices parts.

13. Tested with output open and minimum capacitance. $\overline{OE}$ is high for L8C403 and L8C404.

14. Icc of devices running at high frequencies can be calculated using the following equation:

Commercial:

Icc = 35 mA + (1.5 mA × [f – 10 MHz]

Military:

Icc = 40 mA + (1.5 mA × [f – 10 MHz]

15. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

16. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

17. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

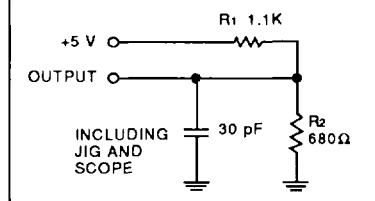


FIGURE 1b.

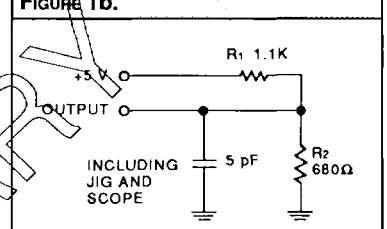
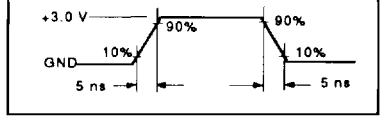


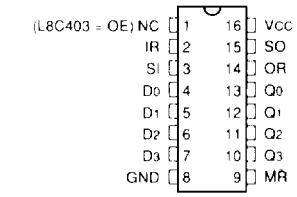
FIGURE 2.

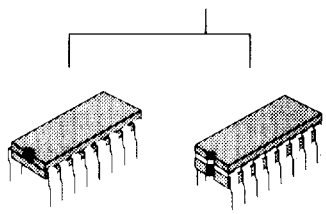


18. The user must be aware that there is no true minimum value for t_{EHEL} and t_{EHPL}. These pulses may be slight during high load under certain operating conditions and lot variations.

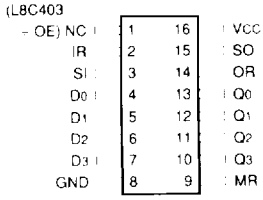
L8C401 and L8C403 ORDERING INFORMATION

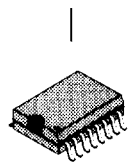
16-pin (0.3" wide)



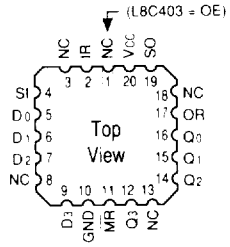


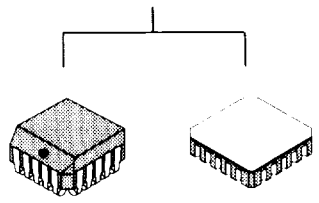
16-pin





20-pin

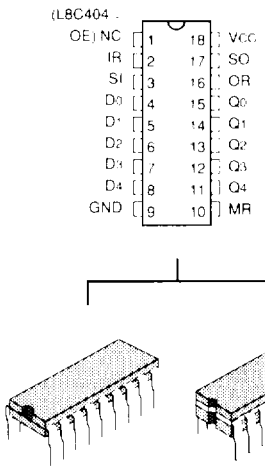




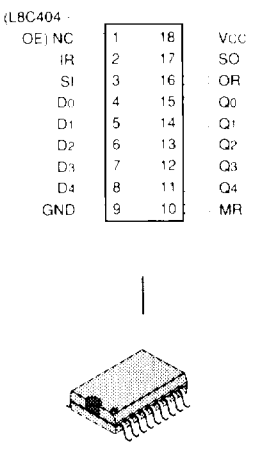
Speed (MHz)	Plastic DIP (P12)	CerDIP (C7)	Plastic SOIC (0.300" — U4)	Plastic Leaded Chip Carrier (J7)	Ceramic Leadless Chip Carrier (K8)
	0°C to +70°C — Commercial Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz	L8C401PC or L8C403PC — 15, 20, 25, 35, 50	L8C401CC or L8C403CC — 15, 20, 25, 35, 50	L8C401UC or L8C403UC — 15, 20, 25, 35, 50	L8C401JC or L8C403JC — 15, 20, 25, 35, 50	L8C401KC or L8C403KC — 15, 20, 25, 35, 50
	–55°C to +125°C — Commercial Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C401CM or L8C403CM — 15, 20, 25, 35			L8C401KM or L8C403KM — 15, 20, 25, 35
	–55°C to +125°C — Extended Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C401CME or L8C403CME — 15, 20, 25, 35			L8C401KME or L8C403KME — 15, 20, 25, 35
	–55°C to +125°C — MIL-STD-883 Compliant				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C401CMB or L8C403CMB — 15, 20, 25, 35			L8C401KMB or L8C403KMB — 15, 20, 25, 35

L8C402 and L8C404 ORDERING INFORMATION

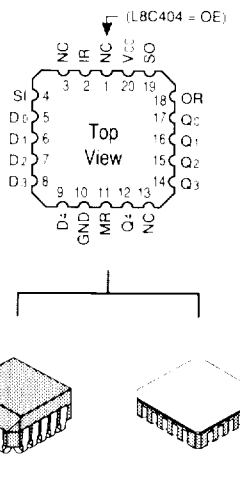
18-pin (0.3" wide)



18-pin



20-pin



Speed (MHz)	Plastic DIP (P13)	CerDIP (C8)	Plastic SOIC (0.300" — U5)	Plastic Leaded Chip Carrier (J7)	Ceramic Leadless Chip Carrier (K8)
	0°C to +70°C — Commercial Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz	L8C402PC or L8C404PC — 15, 20, 25, 35, 50	L8C402CC or L8C404CC — 15, 20, 25, 35, 50	L8C402UC or L8C404UC — 15, 20, 25, 35, 50	L8C402JC or L8C404JC — 15, 20, 25, 35, 50	L8C402KC or L8C404KC — 15, 20, 25, 35, 50
	–55°C to +125°C — Commercial Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C402CM or L8C404CM — 15, 20, 25, 35			L8C402KM or L8C404KM — 15, 20, 25, 35
	–55°C to +125°C — Extended Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C402CME or L8C404CME — 15, 20, 25, 35			L8C402KME or L8C404KME — 15, 20, 25, 35
	–55°C to +125°C — MIL-STD-883 Compliant				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C402CMB or L8C404CMB — 15, 20, 25, 35			L8C402KMB or L8C404KMB — 15, 20, 25, 35