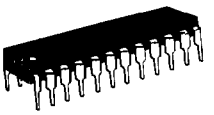
MCM6207

256K x 1 Bit Fast Static RAM

The MCM6207 is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ±10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 15, 20, and 25 ns
- Equal Address and Chip Enable Access Times
- Low Power Operation: 130 –150 mA Maximum ac
- Fully TTL-Compatible — Three-State Output
- Separate Data Input and Output



P PACKAGE
300-MIL PLASTIC
CASE 724A

J PACKAGE
300-MIL SOJ
CASE 810A

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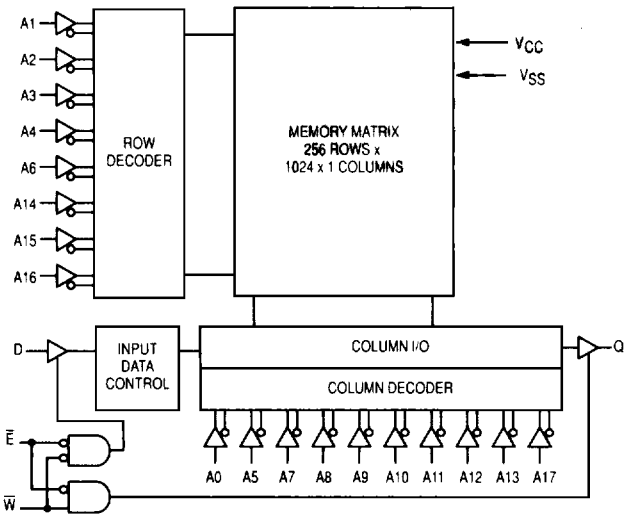
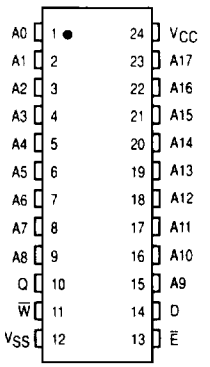
BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0—A15	Address Input
DQ0—DQ3	Data Input/Data Output
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

TRUTH TABLE (X = don't care)

$\overline{E1}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	–
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High–Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to + 7.0 V	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias (T_A = 25°C)	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70° C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V V_{CC} = MAX, f = 0 MHz)	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	- 15	- 20	- 25	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	150	140	130	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = MAX, f = f_{max})	I_{SB1}	50	45	40	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25° C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$,$\overline{W}$)	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ± 10 %, T_A = 0 to + 70° C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol		-15		-20		-25		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	20	—	25	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	15	—	20	—	25	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	8	0	9	0	10	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min for a given device and from device to device.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

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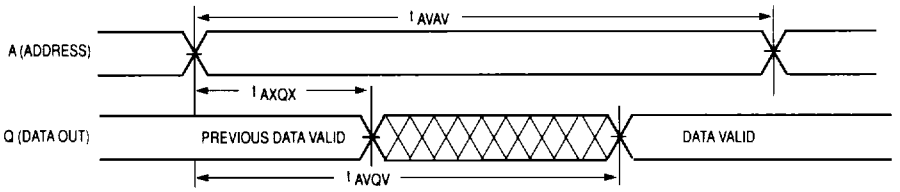
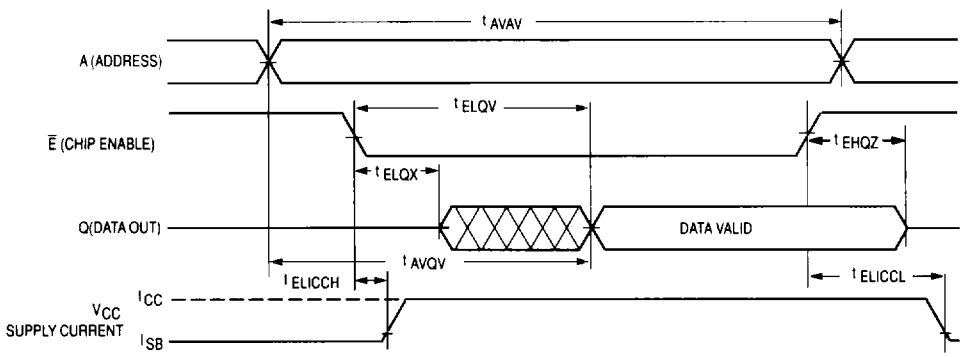
READ CYCLE 1



READ CYCLE 2 (See Notes 2 and 4)



AC TEST LOADS

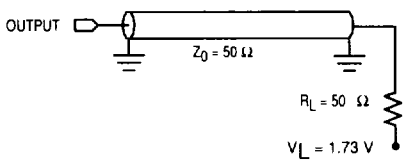


Figure 1A

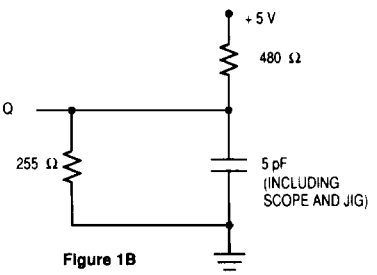
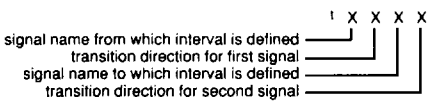


Figure 1B

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device output will be valid no later than that time.

WRITE CYCLE 1 ($\overline{W}$ Controlled) (See Note 1)

Parameter	Symbol		-15		-20		-25		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	25	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	15	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	12	—	15	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	7	0	8	0	10	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

WRITE CYCLE 2 ($\overline{E}$ Controlled) (See Notes 1)

Parameter	Symbol		-15		-20		-25		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	25	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	15	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	10	—	12	—	15	—	ns	6,7
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{WLQG} max < t_{WHQX} min, both for a given device and from device to device.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
7. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

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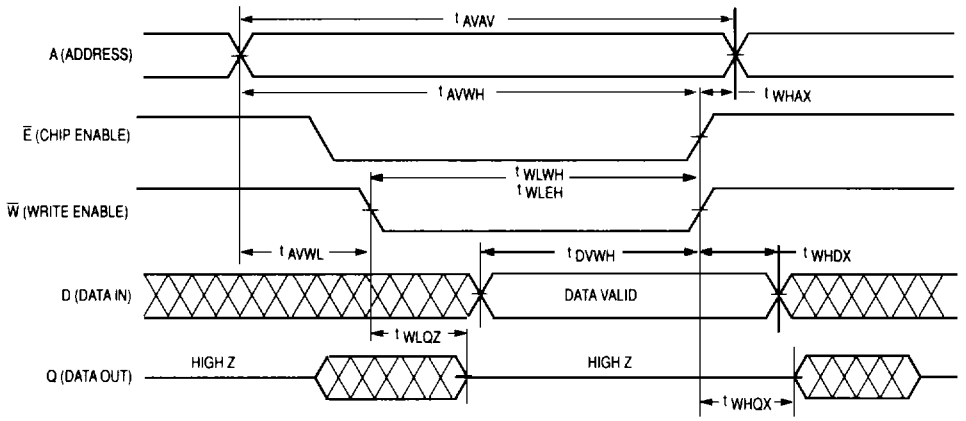
WRITE CYCLE 1 (See Note 2)



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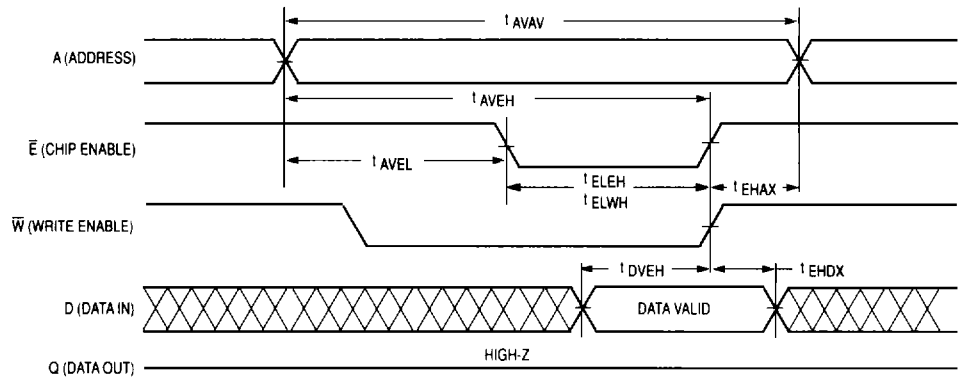
WRITE CYCLE 2 (See Note 2)



ORDERING INFORMATION (Order by Full Part Number)

MCM 6207 X XX XX

Motorola Memory Prefix — MCM

Part Number — 6207

Package (P = 300-mil Plastic DIP, J = 300-mil SOJ) — X

Speed (15 = 15 ns, 20 = 20 ns, 25 = 25 ns) — XX

Shipping Method (R2 = Tape & Reel, Blank = Rails) — XX

Full Part Numbers—			
	MCM6207P15	MCM6207J15	MCM6207J15R2
	MCM6207P20	MCM6207J20	MCM6207J20R2
	MCM6207P25	MCM6207J25	MCM6207J25R2