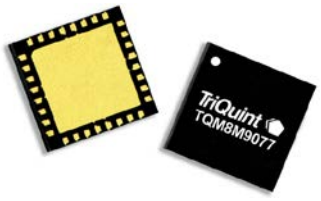
TQM8M9077

0.05 – 4 GHz Digital Variable Gain Amplifier

Applications

- Wireless Infrastructure
- Fixed Wireless
- Microwave and Satellite Radio
- IF and RF Applications
- General Purpose Wireless



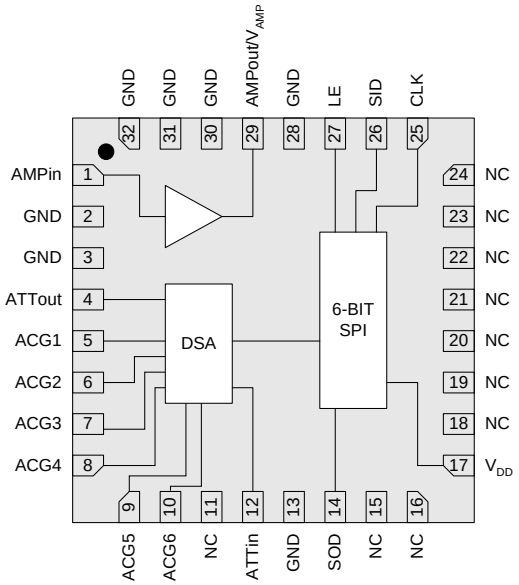
32 Pin 5 x 5 mm Leadless SMT Package

Product Features

- Integrates DSA + Amp Functionality
- 50 – 4000 MHz Broadband Performance
- 13 dB Gain at 2.14 GHz
- 3.9 dB Noise Figure at max gain setting
- +21.5 dBm P1dB
- +38.5 dBm OIP3
- +5 V Supply Voltage
- 88 mA Operating Current
- MTTF > 1000 Years

Functional Block Diagram

Top View



General Description

The TQM8M9077 is a digitally controlled variable gain amplifier (DVGA) with a broadband frequency range of 50 to 4000 MHz. The DVGA features high linearity and low noise while providing digital variable gain with 31.5 dB of range in 0.5 dB steps through a 6-bit serial mode control interface. This combination of performance parameters makes the DVGA ideal for receiver applications requiring gain control with high IIP3 and low noise figure.

The TQM8M9077 integrates a high performance digital step attenuator and a high linearity, broadband gain block. Both stages are internally matched to 50 Ohms and do not require any external matching components. A serial output port enables cascading with other serial controlled devices.

The TQM8M9077 is packaged in a RoHS-compliant, compact 5 x 5 mm surface-mount leadless package. Superior thermal design allows the product to have a minimum MTTF rating of 1000 years at a mounting temperature of +85 °C.

The TQM8M9077 is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless application.

Pin Configuration

Pin No.	Label	Pin No.	Label
1	AMPin	17	V_{DD}
4	ATTout	25	CLK
5 – 10	ACG1 – 6	26	SID
14	SOD	27	LE
12	ATTin	29	AMPout / V_{AMP}

11, 15, 16, 18–24	NC
2, 3, 13, 28, 30–32	GND
Backside Pad	Ground RF/DC

Ordering Information

Part No.	Description
TQM8M9077	Digital Variable Gain Amplifier
TQM8M9077−PCB	0.3-4.0 GHz Evaluation Board

Standard T/R size: 2500 pieces on a 13” reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150 °C
RF Input Power, CW, 50 Ω,T = 25°C	+24 dBm
Supply Voltage (V_{DD}, V_{AMP})	+6 V
Reverse Device Voltage	−0.3 V
Digital Input Voltage	V_{DD}+0.5 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{DD}	+4.75	+5	+5.25	V
I_{DD}		88		mA
Operating Temp. Range	−40		+85	°C
T_J (for >10^6 hours MTTF)			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = V_{AMP} =+5 V, Temp.=+25 °C, Configured as DSA followed by Amp

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		50		4000	MHz
Test Frequency			2140		MHz
Gain		11	13		dB
Gain Control Range			31.5		dB
Gain Accuracy		± (0.3 + 4% of Atten. Setting) Max			dB
Attenuation Step			0.5		dB
Time $_{rise\ /\ fall}$	10% / 90% RF		90		ns
Time $_{on,}$ Time $_{off}$	50% CTL to 10% / 90% RF		100		ns
Input Return Loss			17		dB
Output Return Loss			10.5		dB
Output P1dB			+21.5		dBm
Output IP3	Pout=+3 dBm/tone, Δf=1 MHz	+35.5	+38.5		dBm
Noise Figure	At max gain level		3.9		dB
Supply Current (I_{DD})		70	88	110	mA
Thermal Resistance	Channel to case			41	°C/W

Serial Control Interface

The TQM8M9077 has a CMOS SPI™ input compatible serial interface. This serial control interface converts the serial data input stream to parallel output word. The input is 3-wire (CLK, LE and SID) SPI™ input compatible. At power up, the serial control interface resets the DSA to the minimum gain state. The 6-bit SID (Serial Input Data) word is loaded into the register on rising edge of the CLK, MSB first. When LE is high, CLK is internally disabled.

Serial Control Timing Characteristics (Test conditions: V_{DD} = +5 V, Temp.=25 °C)

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		10	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	10		ns
LE Pulse Width, t_{LEPW}		30		ns
SID set-up time, t_{SDSUP}	before CLK rising edge	10		ns
SID hold-time, t_{SDHLD}	after CLK rising edge	10		ns
LE Pulse Spacing t_{LE}	LE to LE pulse spacing	630		ns
Propagation Delay t_{PLO}	LE to Parallel output valid		30	ns

Serial Control DC Logic Characteristics (Test conditions: V_{DD} = +5 V, Temp.=25 °C)

Parameter	Condition	Min	Max	Units
Input Low State Voltage, V_{IL}		0	0.8	V
Input High State Voltage, V_{IH}	Min value shown valid for V_{DD}=+5 V only	2.1	V_{DD}	V
Output High State Voltage, V_{OH}	On SOD pin	2.0	V_{DD}	V
Output Low State Voltage, V_{OL}	On SOD pin	0	0.8	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK pins	−10	+10	µA

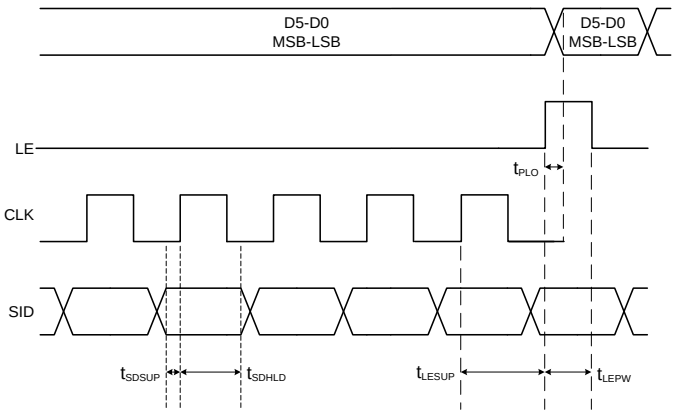
SERIN Control Logic Truth Table

6-Bit Control Word						Gain Relative to Maximum Gain
MSB					LSB	
D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	Maximum Gain
1	1	1	1	1	0	−0.5 dB
1	1	1	1	0	1	−1 dB
1	1	1	0	1	1	−2 dB
1	1	0	1	1	1	−4 dB
1	0	1	1	1	1	−8 dB
0	1	1	1	1	1	−16 dB
0	0	0	0	0	0	−31.5 dB

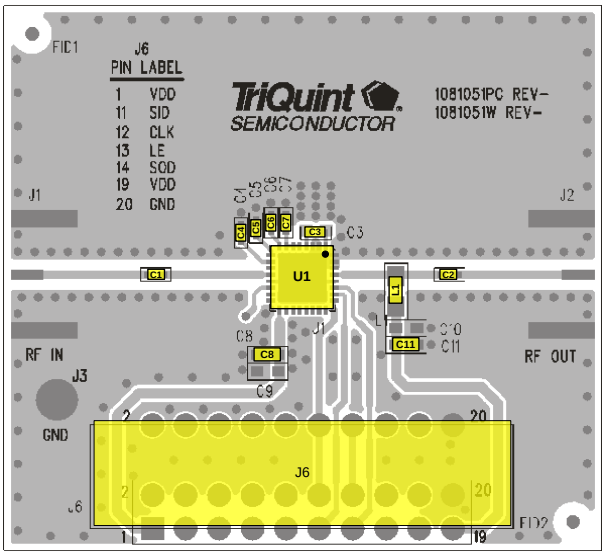
Any combination of the possible 64 states will provide a reduction in gain of approximately the sum of the bits selected.

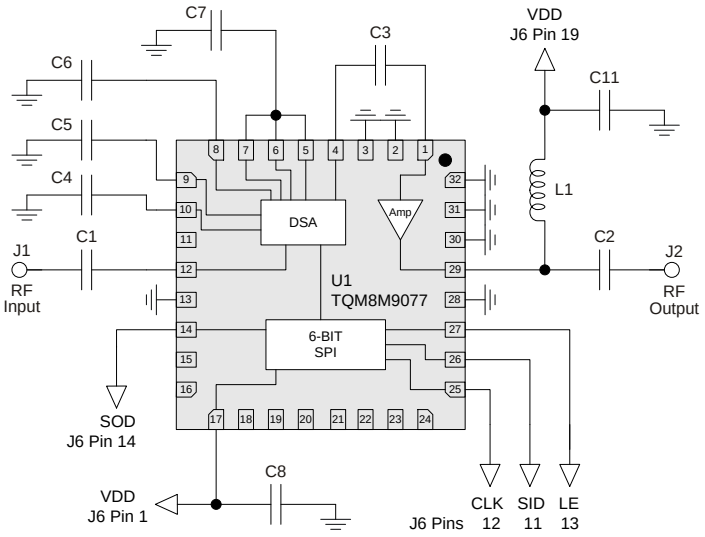
Timing Diagram

CLK is internally disabled when LE is high



TQM8M9077−PCB Evaluation Board





Notes:
1. See Evaluation Board PCB Information section for material and stack-up.
2. C4, C5, C6 and C7 may be removed for operation above 700 MHz.

Bill of Material − TQM8M9077−PCB

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	TriQuint	1081051
U1	N/A	Digital Variable Gain Amp	TriQuint	TQM8M9077
L1 (Note 1)	47 nH	Inductor, 0603	Coilcraft	0603CS-47NXJLW
C1, C2, C3	68 pF	Capacitor, 0402	various	
C4, C5, C6, C7	330 pF	Capacitor, 0402	various	
C8	1000 pF	Capacitor, 0603	various	
C11	0.01 uF	Capacitor, 0603	various	

Notes:
1. For IF applications (<300 MHz) increase L1 to 330 nH.

Typical Performance TQM8M9077-PCB

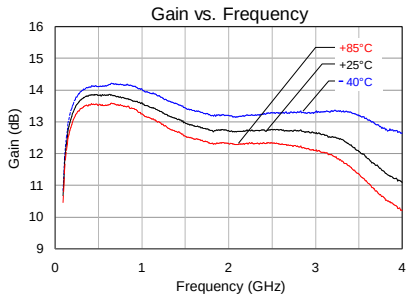
Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=88 mA (typ.), Temp=+25 °C

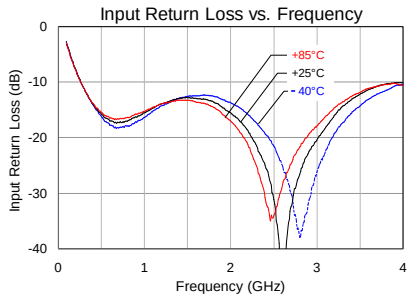
Parameter	Typical Value						Units
Frequency	500	900	2140	2700	3500	4000	MHz
Gain (1)	14.1	14.0	13.0	13.0	12.4	11.4	dB
Input Return Loss	15.8	16.2	17.6	32.5	12.2	10.1	dB
Output Return Loss	14.3	22.5	10.5	13.9	13.6	9.6	dB
Output P1dB	+21.5	+21.7	+21.5	+20.5	+19.6	+18.3	dBm
Output IP3 (2)	+40.7	+41.2	+38.5	+37.8	+36.3	+35.6	dBm
Noise Figure (3)	3.0	3.1	3.9	4.3	5.5	6.2	dB

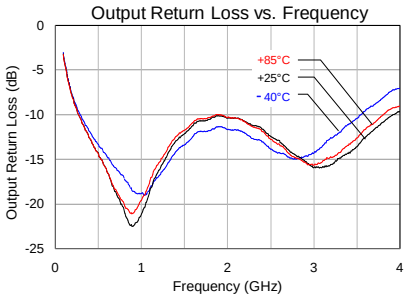
Notes:

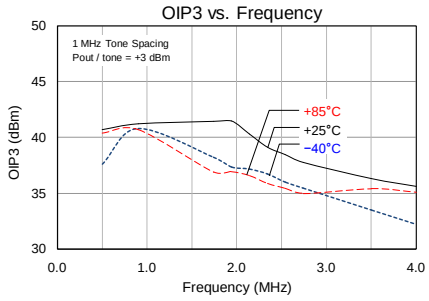
1. Gain values reflect de-embedding of 0.4 dB eval board RF I/O line losses that would not be present in target applications.
2. Pout= +3 dBm/tone, Δf=1 MHz
3. NF values reflect de-embedding of eval board RF I/O line losses that would not be present in target applications.
4. Unless otherwise stated, performance plots shown below for DVGA maximum gain state.

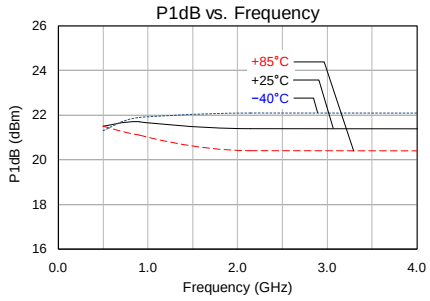
Performance Plots - TQM8M9077-PCB

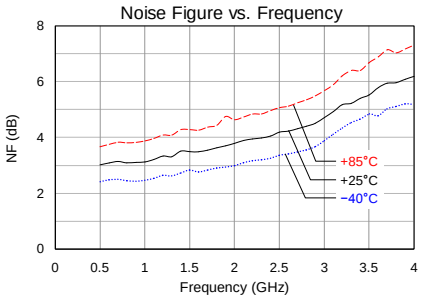


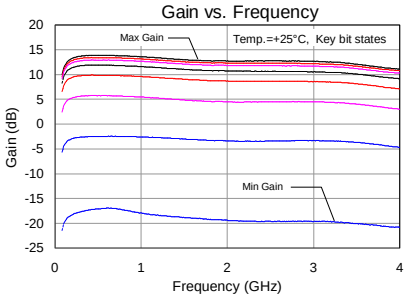


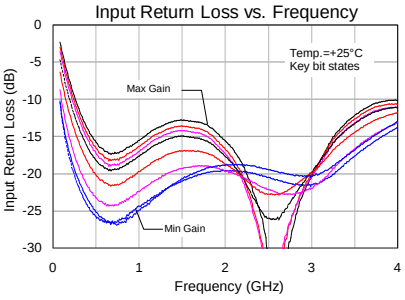


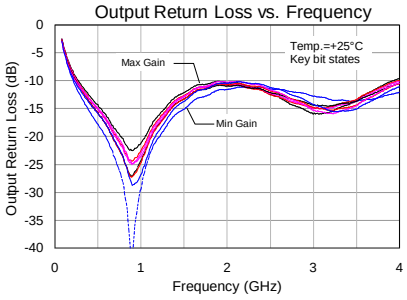






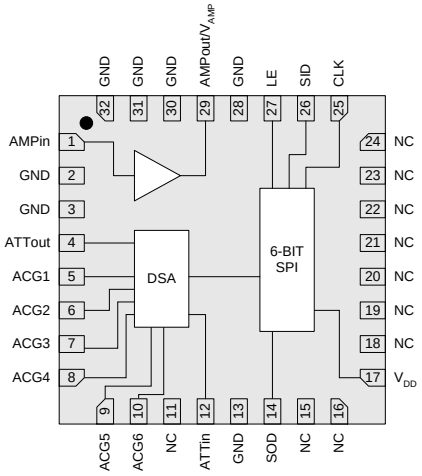






Pin Configuration and Description

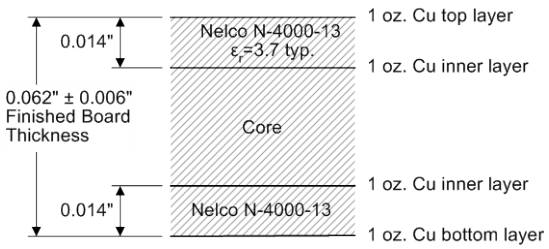
Top View



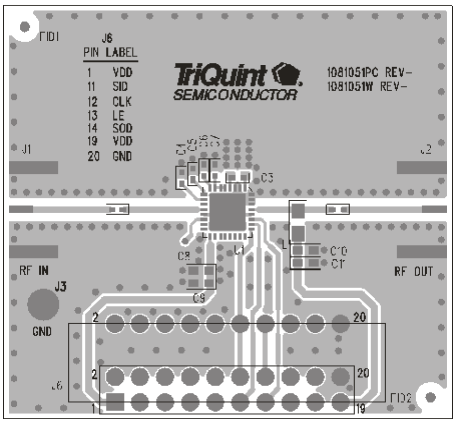
Pin No.	Symbol	Description
1	AMPin	Amp RF input. External DC block required.
2, 3,13, 28, 30, 31, 32	GND (Ground)	DC ground
11, 15, 16, 18-24	NC (No Connect)	No electrical connection. Provide land pads for PCB mounting integrity.
29	AMPout/V_{AMP}	Amp RF output / DC supply. External DC block and bias choke required.
12	ATTin	DSA Input
4	ATTout	DSA Output
5, 6, 7, 8, 9, 10	ACG1-6	Place external capacitor to Ground for applications below 700 MHz.
14	SOD	Serial Output Data
17	V_{dd}	DC supply into SPI and DSA
25	CLK	Serial Clock
26	SID	Serial Input Data
27	LE	Latch Enable
Backside Pad	RF/DC GND	RF/DC ground. Use recommended via pattern and ensure good solder attach for best thermal and electrical performance.

Evaluation Board PCB Information

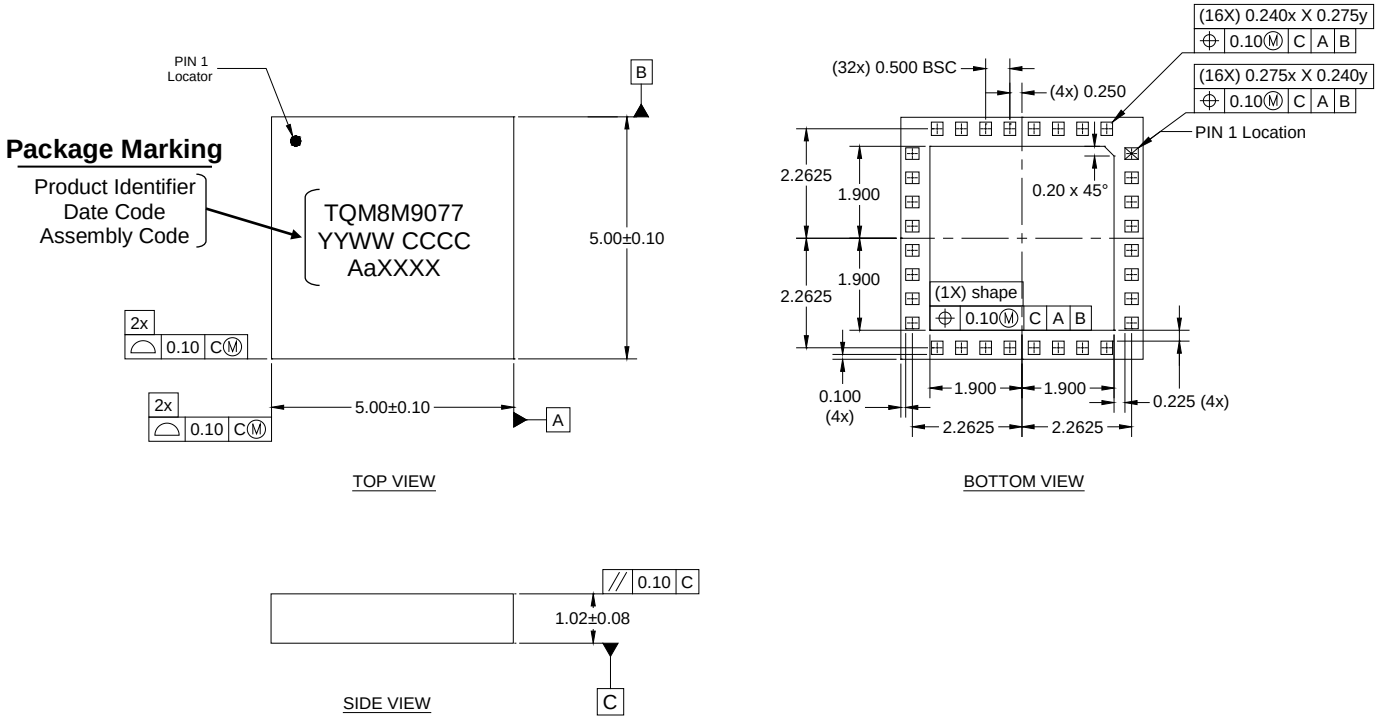
TriQuint PCB 1081051 Material and Stack-up



50 ohm line dimensions: width = .026”, spacing = .032”



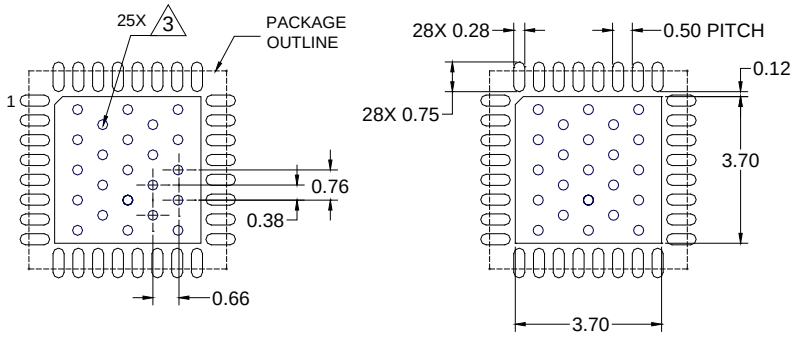
Package Marking and Dimensions



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



COMPONENT SIDE

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
1. Use 1 oz. copper minimum for top and bottom layer metal.
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
3. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: ≥ 250 V to < 500 V
Test: Human Body Model (HBM)
Standard: ESDA/JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: ≥ 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 3
Test: 260 °C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C maximum reflow temperature) and tin/lead (245 °C maximum reflow temperature) soldering processes.

Contact plating: Electrolytic plated Au over Ni

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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