# *Quad Channel Low Capacitance ESD Protection Array*

## *UM5204EECD TSOP-6/SOT23-6*

### General Description

UM5204EECD is surge rated diode arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by ESD (electrostatic discharge).
The unique design incorporates surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.
The low capacitance array configuration allows the user to protect four high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges. This device is optimized for ESD protection of portable electronics. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ± 8kV contact discharge).

### Applications

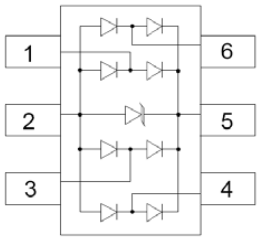
- USB 2.0
- USB OTG
- Monitors and Flat Panel
- Displays digital Visual Interface (DVI)
- High-Definition Multimedia Interface (HDMI)
- SIM Ports IEEE 1394 Firewire Ports

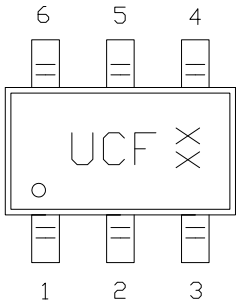
### Features

- Transient protection for high-speed data lines to
  IEC 61000-4-2 (ESD) ± 15kV (air), ± 8kV (contact)
- Array of surge rated diodes with internal TVS Diode
- Protects up to four I/O lines & power line
- Low capacitance (<2pF) for high-speed interfaces
- No insertion loss to 2.0GHz
- Low leakage current and clamping voltage
- Low operating voltage: 5.0V
- Solid-state silicon-avalanche technology

### Pin Configurations

### Top View




XX: Week Code
UM5204EECD
TSOP-6/SOT23-6

## Ordering Information

| Part Number | Working Voltage | Packaging Type | Channel | Marking Code | Shipping Qty |
|---|---|---|---|---|---|
| UM5204EECD | 5.0V | TSOP-6/SOT23-6 | 4 | UCF | 3000pcs /7Inch Tape & Reel |

## Absolute Maximum Ratings

| | | | |
|---|---|---|---|
| Peak Pulse Power (tp = 8/20μS) | $P_{pk}$ | 150 | Watts |
| Peak Pulse Current (tp = 8/20μS ) | $I_{PP}$ | 6 | A |
| ESD per IEC 61000-4-2 (Air)<br>ESD per IEC 61000-4-2 (Contact) | $V_{ESD}$ | ±15<br>±8 | kV |
| Operating Temperature | $T_J$ | -55 to +125 | °C |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C |

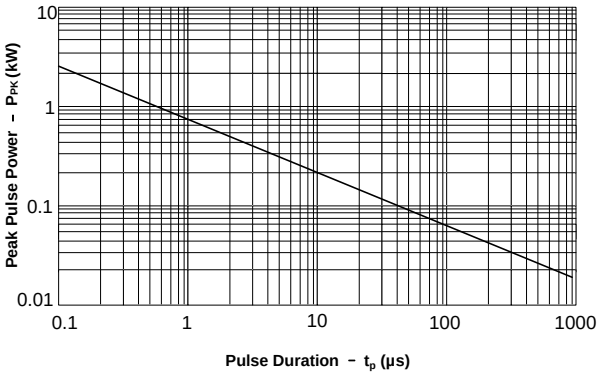
## Electrical Characteristics （Note 1）

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Reverse Stand-Off Voltage | $V_{RWM}$ | | | | 5.0 | V |
| Reverse Breakdown Voltage | $V_{BR}$ | It = 1mA, Pin 5 to Pin2 | 6.0 | | | V |
| Reverse Leakage Current | $I_R$ | $V_{RWM}$ = 5V, T=25°C, Pin5 to Pin2 | | | 2 | μA |
| Clamping Voltage | $V_C$ | $I_{PP}$ = 1A, 8/20μS, Any pin to pin2 | | | 15 | V |
| Clamping Voltage | $V_C$ | $I_{PP}$ = 6A, 8/20μS, Any pin to pin2 | | | 25 | V |
| Junction Capacitance | $C_j$ | $V_R$ = 0V, f = 1MHz, Any I/O pin to pin2 | | | 2 | pF |
| | | $V_R$ = 0V, f = 1MHz , Between I/O pins | | | 1 | pF |
| | | $V_R$ = 0V, f = 1MHz, Pin5to pin2 | | 60 | | pF |
| | | $V_R$ = 2.5V, f = 1MHz, Pin5to pin2 | | 40 | | pF |
| Reverse Recovery Time | Trr | Pin2to Pin5 | | 40 | | ns |
| | | Pin2to I/O Pin | | 160 | | ns |
| | | Pin5to I/O Pin | | 45 | | ns |

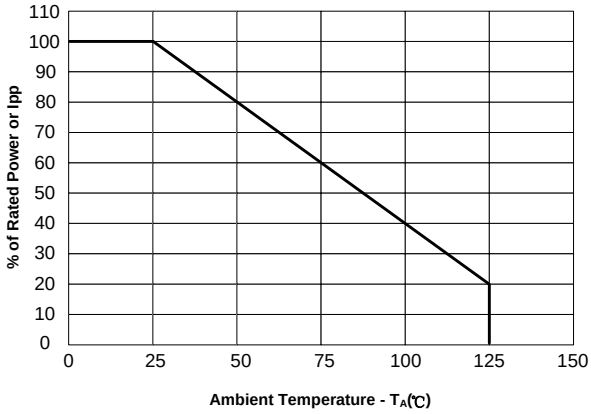
Note 1: I/O pins are pin 1, 3, 4, and 6

## Typical Operating Characteristics

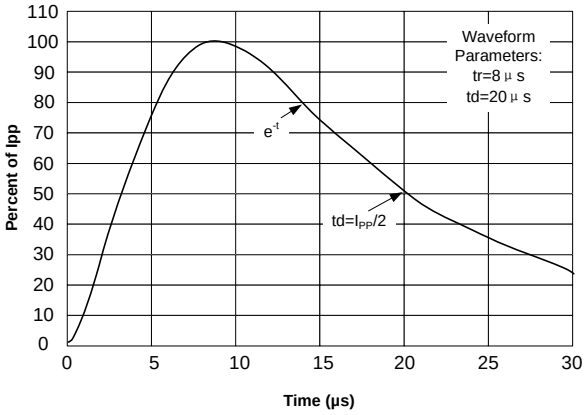
**Non-Repetitive Peak Pulse Power vs. Pulse Time**



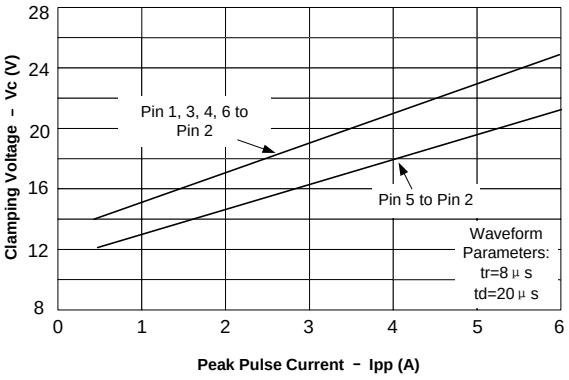

**Power Derating Curve**



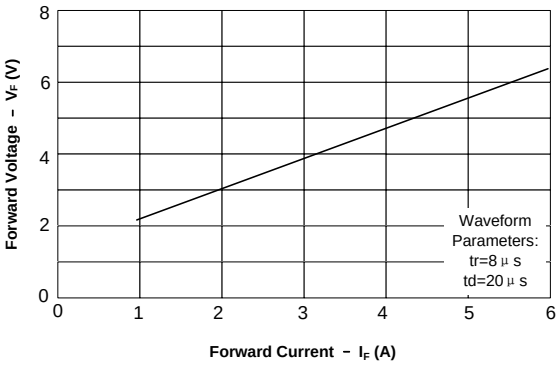

**Pulse Waveform**



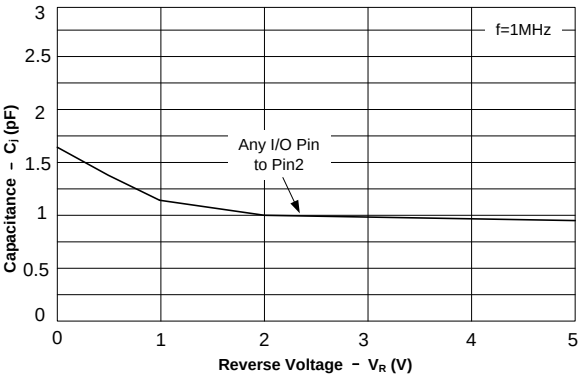

**Clamping Voltage vs. Peak Pulse Current**




**Forward Voltage vs. Forward Current**




**Junction Capacitance vs. Reverse Voltage**



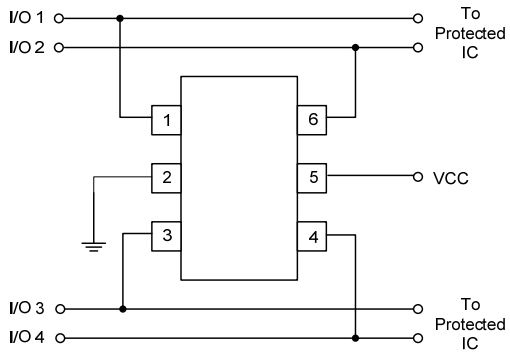
## Applications Information

### Device Connection Options for Protection of Four High-Speed Data Lines

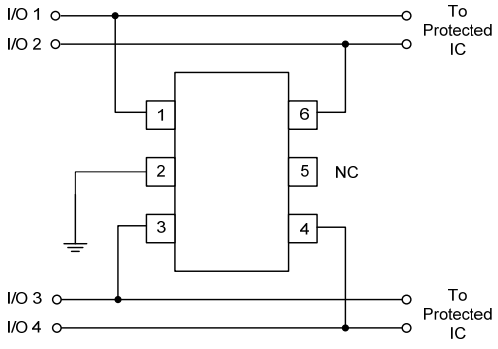
This device is designed to protect data lines by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. Pin 2 should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pin 5. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 5 directly to the positive supply rail (VCC). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. In applications where the supply rail does not exit the system, the internal TVS may be used as the reference. In this case, pin 5 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).
3. In applications where complete supply isolation is desired, the internal TVS is again used as the reference and VCC is connected to one of the I/O inputs. An example of this configuration is the protection of a SIM port. The Clock, Reset, I/O, and VCC lines are connected at pins 1, 3, 4, and 6. Pin 2 is connected to ground and pin 5 is not connected.

**Protection of Four Data Lines and Power Supply Line**




**Protection of Four Data Lines using Internal TVS Diode as Reference**



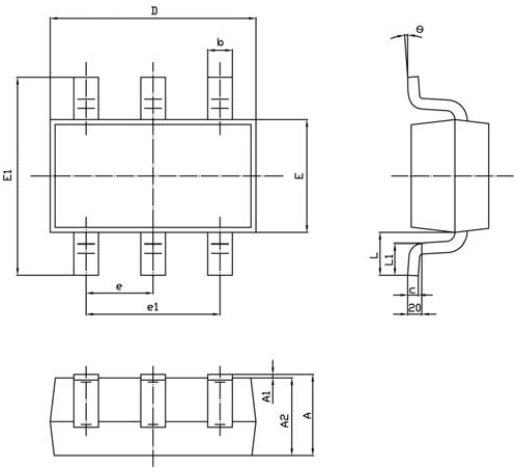

### Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

## Package Information

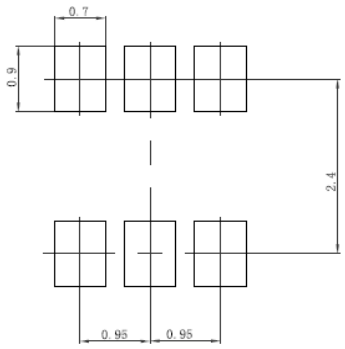
### UM5204EECD TSOP-6/SOT23-6

**Outline Drawing**



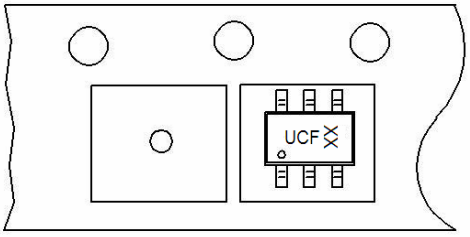

| Symbol | DIMENSIONS | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | Min | Max | Min | Max |
| A | 1.050 | 1.250 | 0.041 | 0.049 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 1.050 | 1.150 | 0.041 | 0.045 |
| b | 0.300 | 0.500 | 0.012 | 0.020 |
| c | 0.100 | 0.200 | 0.004 | 0.008 |
| D | 2.820 | 3.020 | 0.111 | 0.119 |
| E | 1.500 | 1.700 | 0.059 | 0.067 |
| E1 | 2.650 | 2.950 | 0.104 | 0.116 |
| e | 0.950REF | | 0.037REF | |
| e1 | 1.800 | 2.000 | 0.071 | 0.079 |
| L | 0.600REF | | 0.023REF | |
| L1 | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0° | 8° | 0° | 8° |

**Land Pattern**




NOTES:
1. Compound dimension: 2.92×1.60;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

**Tape and Reel Orientation**



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