EUTECH
MICROELECTRONICS

5-W Stereo Class-D Audio Amplifier with 64-Step DC Volume Control

DESCRIPTION

The EUA2105 is a high efficiency, 2 channel bridged-tied load (BTL), class-D audio power amplifier. Operating from a 12V power supply, EUA2105 is capable of delivering 5W/ channel of continuous output power to a 8Ω load with 1% THD+N. The EUA2105 features a differential input architecture offering improved noise immunity over a single-ended (SE) input amplifier. Stereo speaker volume is controlled with a dc voltage applied to the volume control terminal offering a range of gain from -68dB to32 dB.

The EUA2105 also features short-circuit and thermal protection preventing the device from being damaged during a fault condition. The EUA2105 is available in thermally efficient 28-pin TSSOP package.

FEATURES

- Wide Supply Voltage: 8V to 15V
- Unique Modulation Scheme Reduces EMI Emission
- 5W/ch into an 8Ω Load From 12V Supply
- Efficient, Class-D Operation Eliminates Heatsinks
- 64-Step DC Volume Control From -68dB to 32dB
- Thermal and Short-Circuit Protection
- Integrated Click and Pop Suppression
- 28-pin TSSOP Package with Thermal Pad
- RoHS compliant and 100% lead(Pb)-free

APPLICATIONS

- LCD Monitors/TVs
- All-in-One PCs

Typical Application Circuit

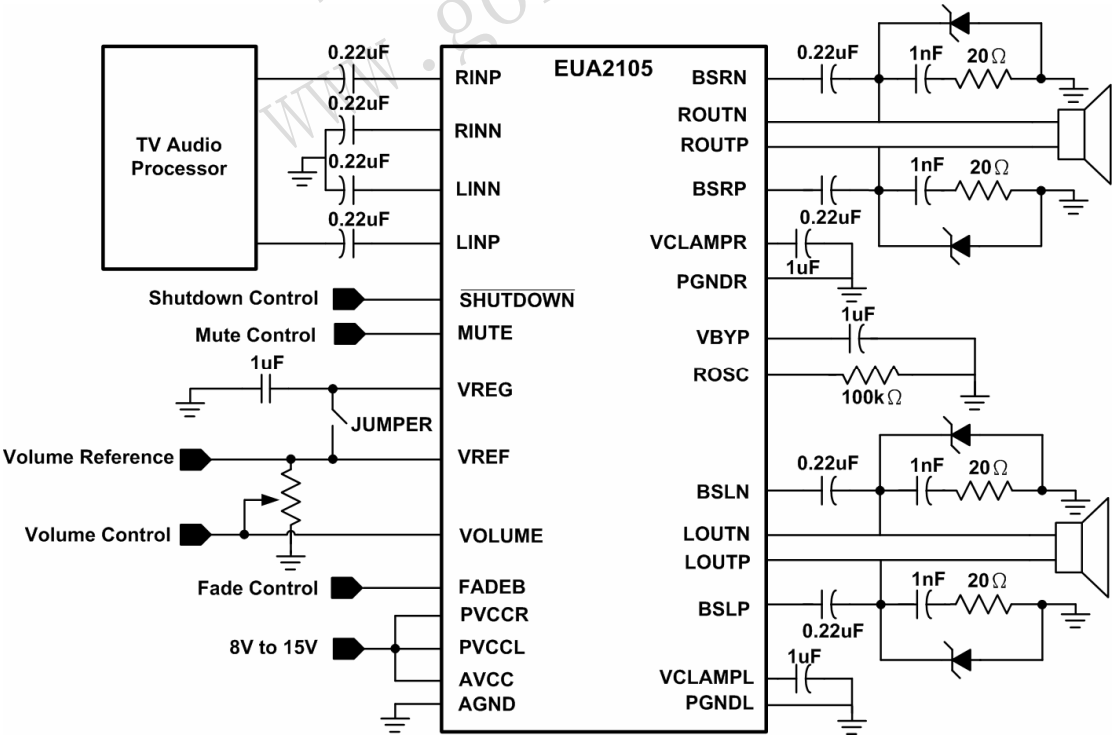
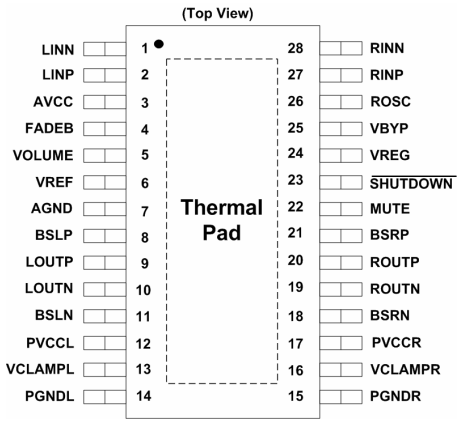


Figure1.

Pin Configurations

Package Type	Pin Configurations
TSSOP-28	

Pin Description

PIN	TSSOP-28	I/O	DESCRIPTION
LINN	1	I	Negative audio input for left channel.
LINP	2	I	Positive audio input for left channel.
AVCC	3	-	High-voltage analog power supply. Not internally connected to PVCCR or PVCCL.
FADEB	4	I	Input for controlling volume ramp rate when cycling SD or during power-up. A logic low on this pin places the amplifier in fade mode. A logic high on this pin allows a quick transition to the desired volume setting.
VOLUME	5	I	DC voltage that sets the gain of the amplifier.
VREF	6	I	Analog reference for gain control section.
AGND	7	-	Analog ground for digital/analog cells in core.
BSLP	8	I/O	Bootstrap I/O for left channel, positive high-side FET.
LOUTP	9	O	Class-D 1/2-H-bridge positive output for left channel.
LOUTN	10	O	Class-D 1/2-H-bridge negative output for left channel.
BSLN	11	I/O	Bootstrap I/O for left channel, negative high-side FET.
PVCCL	12	-	Power supply for left channel H-bridge, not internally connected to PVCCR or AVCC.
VCLAMPL	13	-	Internally generated voltage supply for left channel bootstrap capacitor.
PGNDL	14	-	Power ground for left channel H-bridge.
PGNDR	15	-	Power ground for right channel H-bridge.
VCLAMPR	16	-	Internally generated voltage supply for right channel bootstrap capacitor.
PVCCR	17	-	Power supply for right channel H-bridge, not connected to PVCCL or AVCC.
BSRN	18	I/O	Bootstrap I/O for right channel, negative high-side FET.
ROUTN	19	O	Class-D 1/2-H-bridge negative output for right channel.
ROUTP	20	O	Class-D 1/2-H-bridge positive output for right channel.
BSRP	21	I/O	Bootstrap I/O for right channel, positive high-side FET.
MUTE	22	I	Mute signal for quick disable/enable of outputs (HIGH = outputs high-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
$\overline{\text{SHUTDOWN}}$	23	I	Shutdown signal for IC (LOW = disabled, HIGH = operational). TTL logic levels with compliance to AVCC.
VREG	24	O	4-V regulated output for use by internal cells, FADEB and MUTE pins only. Not specified for driving other external circuitry.

Pin Description (continued)

PIN	TSSOP-28	I/O	DESCRIPTION
VBYP	25	O	Reference for preamplifier. Nominally equal to 1.39V. Also controls start-up time via external capacitor sizing.
ROSC	26	I/O	I/O for current setting resistor of ramp generator.
RINP	27	I	Positive audio input for right channel.
RINN	28	I	Negative audio input for right channel.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA2105QIR1	TSSOP-28	xxxxx EUA2105	-40 °C to +85°C

EUA2105 □ □ □ □

- Lead Free Code
  1: Lead Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  Q:TSSOP

Absolute Maximum Ratings

- Supply Voltage Range, AV_{CC},PV_{CC} ---------- -0.3 V to 18V
- Input Voltage Range, VREF, VOLUME, FADEB ---------- 0V to 5.5V
- Input Voltage Range, $\overline{SHUTDOWN}$, MUTE ---------- -0.3 V to V_{CC}+ 0.3V
- Input Voltage Range, RINN, RINP, LINN, LINP---------- -0.3 V to 6V
- Continuous total power dissipation ---------- See Dissipation Rating Table
- Free-air Temperature Range, T_A ---------- -40°C to +85°C
- Junction Temperature Range, T_J ---------- -40°C to +150°C
- Storage Temperature Rang, T_{stg} ---------- -65°C to +85°C
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- +260°C
- ESD Susceptibility (HBM) ---------- >2kV

Typical Dissipation Ratings

Package	$T_A \leq 25°C$	Derating Factor	T_A= 70°C	T_A= 85°C
TSSOP-28	2.8W	26.3 mW/ °C	1.8W	1.4W

Recommended Operating Conditions

		Min	Max	Unit
Supply voltage	PV_{CC}, AV_{CC}	8	15	V
Volume reference voltage	VREF	2.7	4.2	V
Volume control pins, input voltage	VOLUME		4.2	V
High-level input voltage, V_{IH}	$\overline{SHUTDOWN}$	2		V
	MUTE	2		
	FADEB	2.5		
Low-level input voltage, V_{IL}	$\overline{SHUTDOWN}$		0.8	V
	MUTE		0.8	
	FADEB		1.5	
High-level input current, I_{IH}	MUTE, V_I=5V, V_{CC}=14V		10	µA
	$\overline{SHUTDOWN}$, V_I=14V, V_{CC}=14V		80	
	FADEB, V_I=5V, V_{CC}=14V		10	
Low-level input current, I_{IL}	MUTE, $\overline{SHUTDOWN}$, FADEB V_I=0V, V_{CC}=14V		1	µA
Oscillator frequency, f_{OSC}		200	300	kHz
Operating free-air temperature, T_A		-40	85	°C

DC Characteristics T_A = +25°C , V_{CC}=12V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2105			Unit
			Min	Typ	Max.	
$\lvert V_{OS} \rvert$	Output offset voltage (measured differentially)	INN and INP connected together, Gain=36 dB		5	50	mV
PSRR	Power supply rejection ratio	V_{CC} = 11.5V to 12.5V		-60		dB
	Bypass reference for input amplifier	VBYP, no load	1.3	1.4	1.6	V
	4-V internal supply voltage	VREG, no load	3.9	4.2	4.6	V
ICC	Supply quiescent current	MUTE=0V, $\overline{SHUTDOWN}$ =2V no load, filter or snubber		20	28	mA

DC Characteristics T_A = +25°C , V_{CC}=12V, R_L=8Ω (Unless otherwise noted) (continued)

Symbol	Parameter	Conditions		EUA2105 Min	EUA2105 Typ	EUA2105 Max.	Unit
$ICC_{(MUTE)}$	MUTE mode quiescent current	MUTE=3.5V, $\overline{SHUTDOWN}$ =2V			5	10	mA
$ICC_{(SD)}$	Supply quiescent current in shutdown mode	$\overline{SHUTDOWN}$ =0.8V			500	1000	μA
r_{DS}(on)	Drain-source on-state resistance	V_{CC}=12V, I_O=1A, T_J=25°C	High side		400	500	mΩ
			Low side		400	500	
			Total		800	1000	

AC Characteristics T_A = +25°C , V_{CC}=12V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2105 Min	EUA2105 Typ	EUA2105 Max	Unit
^{k}SVR	Supply ripple rejection ratio	V_{CC}=11.5V to 12.5V from 10Hz to 1kHz, Gain=36dB		-60		dB
$P_{O(max)}$	Maximum Continuous output power	THD+N=1%, f=1kHz, R_L=8Ω		5		W
		THD+N=10%, f=1kHz, R_L=8Ω		6		
THD+N	Total harmonic distortion +noise	R_L=8Ω, f=1kHz, P_O=3W (half-power)		0.2%		
Vn	Output integrated noise floor	20Hz to 22kHz,No weighting filter, Gain=0.5dB		-73		dBV
	Crosstalk, Left↔Right	Gain=20dB, P_O=1W, R_L=8Ω		-100		dB
	Thermal trip point			150		°C
	Thermal hystersis			40		°C

Block Diagram

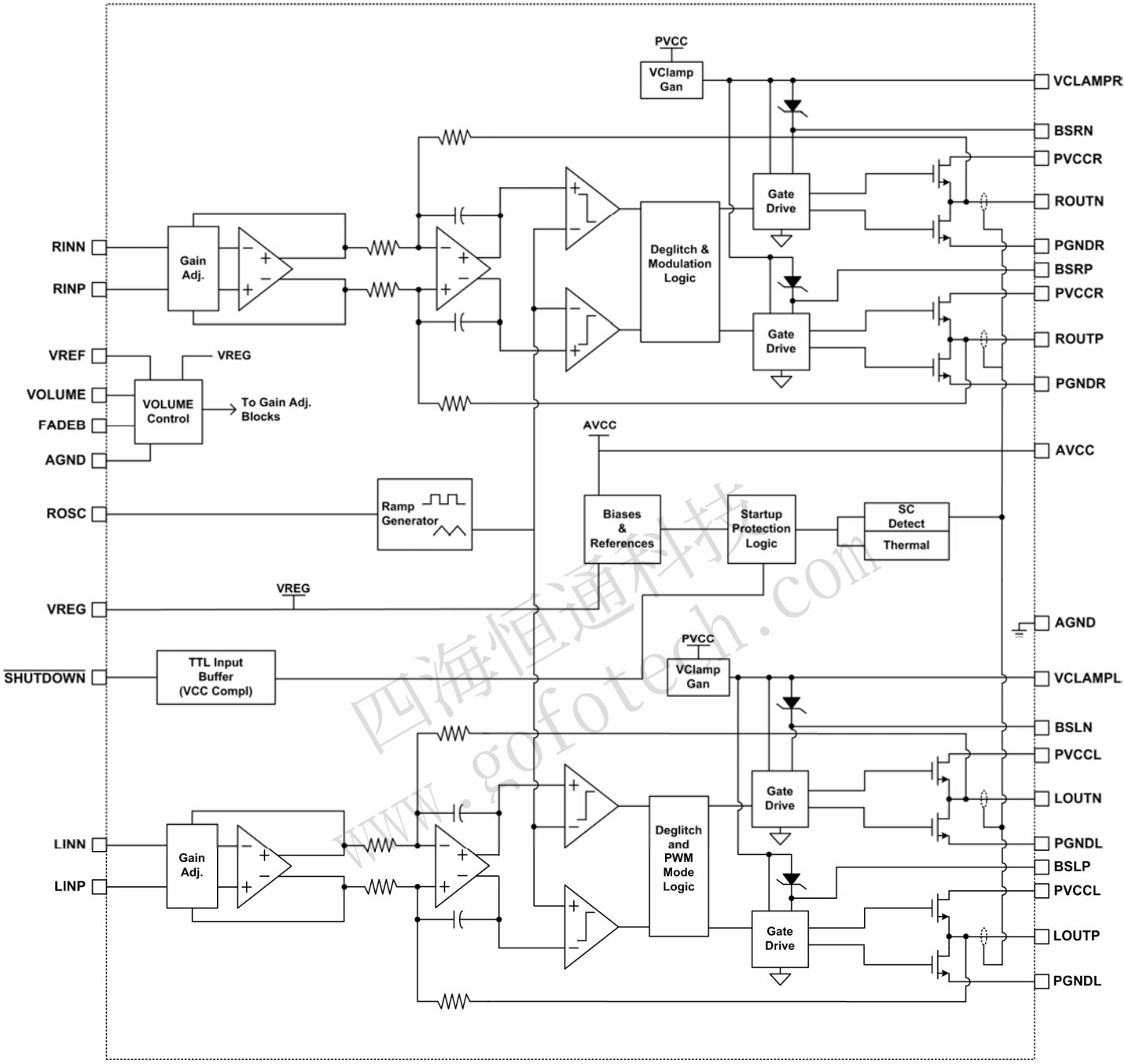


Figure2.

Table 1. DC Volume Control

VOLUME POSITION	VOLUME INPUT VOLTAGE(V)	INCREASING VOLUME (VOLUME PIN VOLTAGE AS A PERCENTAGE OF VREF) (%)	DECREASING VOLUME (VOLUME PIN VOLTAGE AS A PERCENTAGE OF VREF) (%)	Gain (dB)
0	0.100 x VREF	0.0 - 11.1	0.0 - 10.2	-68.6
1	0.113 x VREF	11.1 - 12.3	10.2 - 11.5	-66.0
2	0.126 x VREF	12.3 - 13.6	11.5 - 12.8	-63.5
3	0.138 x VREF	13.6 - 14.9	12.8 - 14.0	-60.9
4	0.151 x VREF	14.9 - 16.2	14.0 - 15.3	-58.4
5	0.164 x VREF	16.2 - 17.4	15.3 - 16.5	-55.9
6	0.176 x VREF	17.4 - 18.7	16.5 - 17.8	-53.3
7	0.189 x VREF	18.7 - 20.0	17.8 - 19.1	-50.8
8	0.202 x VREF	20.0 - 21.2	19.1 - 20.4	-48.2
9	0.214 x VREF	21.2 - 22.5	20.4 - 21.6	-45.7
10	0.227 x VREF	22.5 - 23.8	21.6 - 22.9	-43.2
11	0.240 x VREF	23.8 - 25.0	22.9 - 24.2	-40.6
12	0.252 x VREF	25.0 - 26.3	24.2 - 25.4	-38.1
13	0.265 x VREF	26.3 - 27.6	25.4 - 26.7	-35.6
14	0.278 x VREF	27.6 - 28.8	26.7 - 28.0	-33.0
15	0.290 x VREF	28.8 - 30.1	28.0 - 29.2	-30.5
16	0.303 x VREF	30.1 - 31.4	29.2 - 30.5	-27.9
17	0.316 x VREF	31.4 - 32.6	30.5 - 31.8	-25.4
18	0.328 x VREF	32.6 - 33.9	31.8 - 33.0	-22.9
19	0.341 x VREF	33.9 - 35.2	33.0 - 34.3	-20.3
20	0.354 x VREF	35.2 - 36.5	34.3 - 35.6	-17.8
21	0.366 x VREF	36.5 - 37.7	35.6 - 36.8	-15.2
22	0.379 x VREF	37.7 - 39.0	36.8 - 38.1	-12.7
23	0.392 x VREF	39.0 - 40.3	38.1 - 39.4	-10.2
24	0.405 x VREF	40.3 - 41.5	39.4 - 40.7	-7.6
25	0.417 x VREF	41.5 - 42.8	40.7 - 41.9	-5.1
26	0.430 x VREF	42.8 - 44.1	41.9 - 43.2	-2.5
27	0.443 x VREF	44.1 - 45.3	43.2 - 44.5	0.0
28	0.455 x VREF	45.3 - 46.6	44.5 - 45.7	1.3
29	0.468 x VREF	46.6 - 47.9	45.7 - 47.0	2.5
30	0.481 x VREF	47.9 - 49.1	47.0 - 48.3	3.8
31	0.493 x VREF	49.1 - 50.4	48.3 - 49.5	5.0
32	0.506 x VREF	50.4 - 51.7	49.5 - 50.8	6.3
33	0.519 x VREF	51.7 - 52.9	50.8 - 52.1	7.5
34	0.531 x VREF	52.9 - 54.2	52.1 - 53.3	8.8
35	0.544 x VREF	54.2 - 55.5	53.3 - 54.6	10.0
36	0.557 x VREF	55.5 - 56.8	54.6 - 55.9	11.3
37	0.569 x VREF	56.8 - 58.0	55.9 - 57.1	12.5
38	0.582 x VREF	58.0 - 59.3	57.1 - 58.4	13.8
39	0.595 x VREF	59.3 - 60.6	58.4 - 59.7	15.0
40	0.608 x VREF	60.6 - 61.8	59.7 - 60.9	16.3
41	0.620 x VREF	61.8 - 63.1	60.9 - 62.2	17.5
42	0.633 x VREF	63.1 - 64.4	62.2 - 63.5	18.8
43	0.646 x VREF	64.4 - 65.6	63.5 - 64.8	20.0
44	0.658 x VREF	65.6 - 66.9	64.8 - 66.0	20.6
45	0.671 x VREF	66.9 - 68.2	66.0 - 67.3	21.2
46	0.684 x VREF	68.2 - 69.4	67.3 - 68.6	21.8
47	0.696 x VREF	69.4 - 70.7	68.6 - 69.8	22.4
48	0.709 x VREF	70.7 - 72.0	69.8 - 71.1	23.0
49	0.722 x VREF	72.0 - 73.2	71.1 - 72.4	23.6
50	0.734 x VREF	73.2 - 74.5	72.4 - 73.6	24.2
51	0.747 x VREF	74.5 - 75.8	73.6 - 74.9	24.8
52	0.760 x VREF	75.8 - 77.1	74.9 - 76.2	25.4
53	0.772 x VREF	77.1 - 78.3	76.2 - 77.4	26.0
54	0.785 x VREF	78.3 - 79.6	77.4 - 78.7	26.6
55	0.798 x VREF	79.6 - 80.9	78.7 - 80.0	27.2
56	0.811 x VREF	80.9 - 82.1	80.0 - 81.2	27.8
57	0.823 x VREF	82.1 - 83.4	81.2 - 82.5	28.4
58	0.836 x VREF	83.4 - 84.7	82.5 - 83.8	29.0
59	0.849 x VREF	84.7 - 85.9	83.8 - 85.1	29.6
60	0.861 x VREF	85.9 - 87.2	85.1 - 86.3	30.2
61	0.874 x VREF	87.2 - 88.5	86.3 - 87.6	30.8
62	0.887 x VREF	88.5 - 89.7	87.6 - 88.9	31.4
63	0.899 x VREF	89.7 - 91.0	88.9 - 90.1	32.0

Typical Characteristics

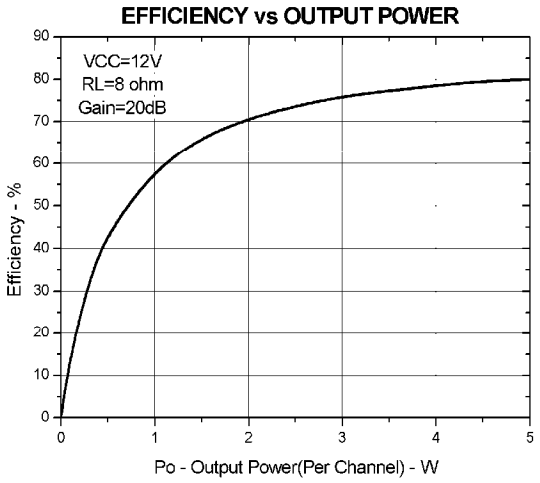
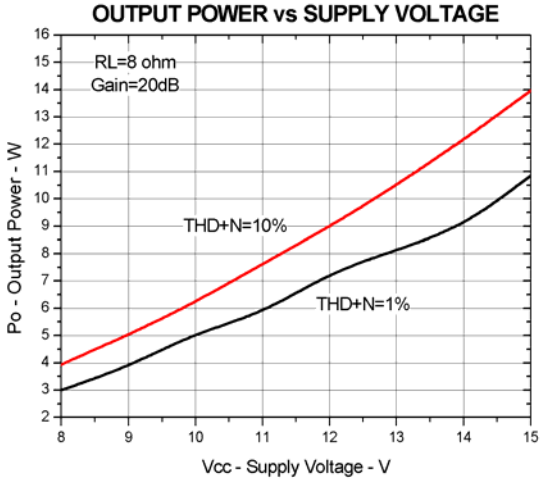


Figure3.



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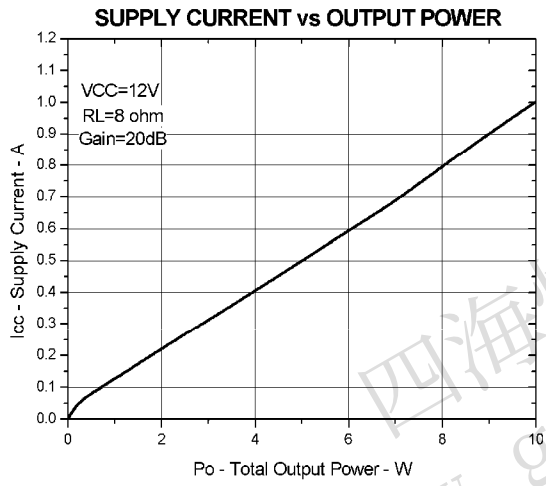

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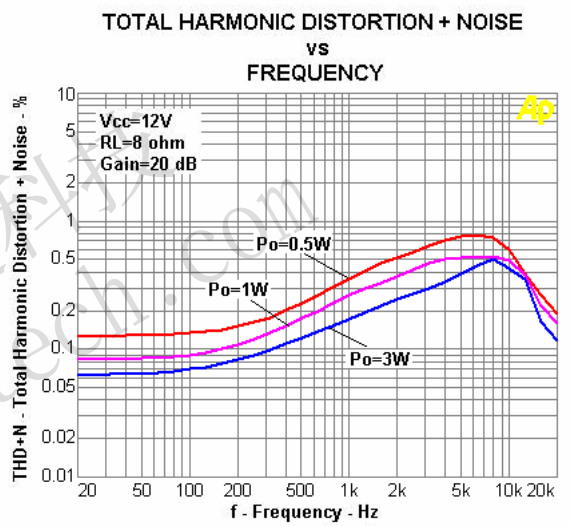
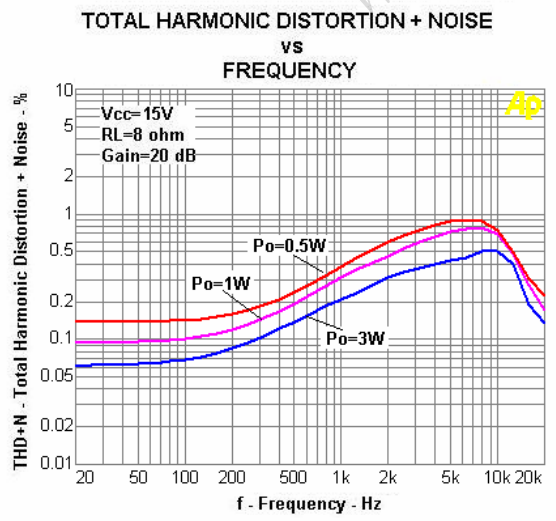


Figure6



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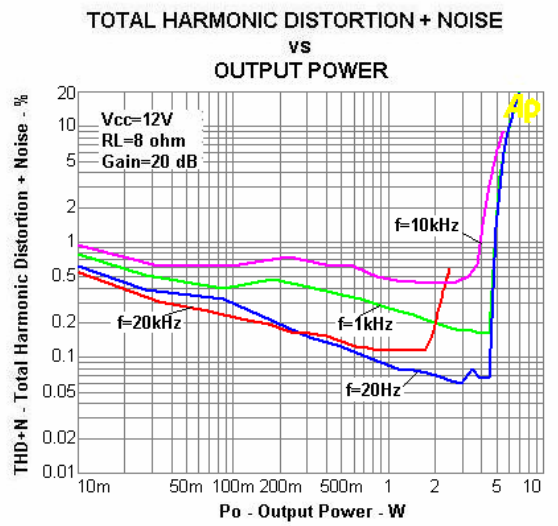

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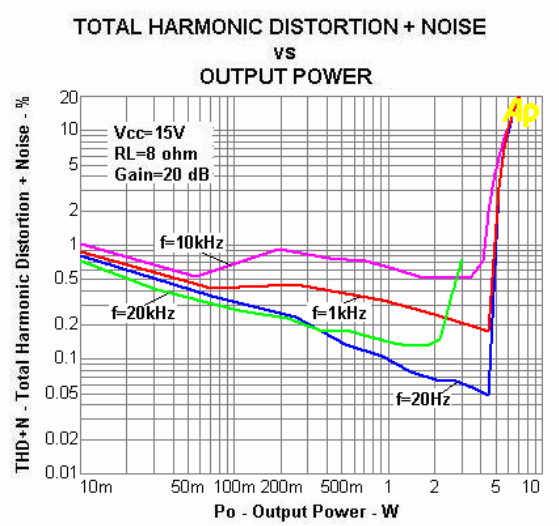

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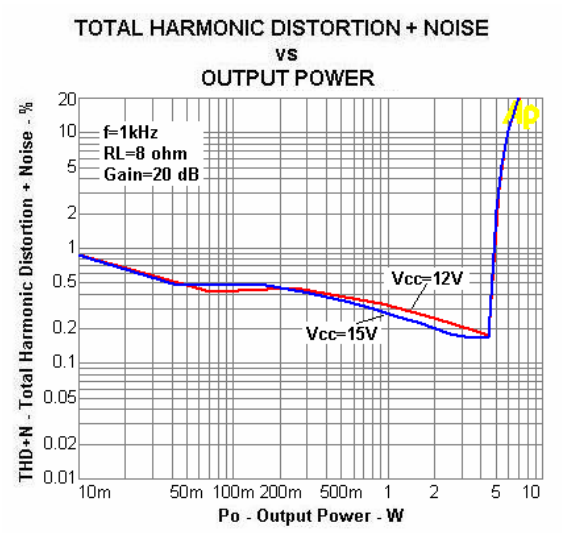

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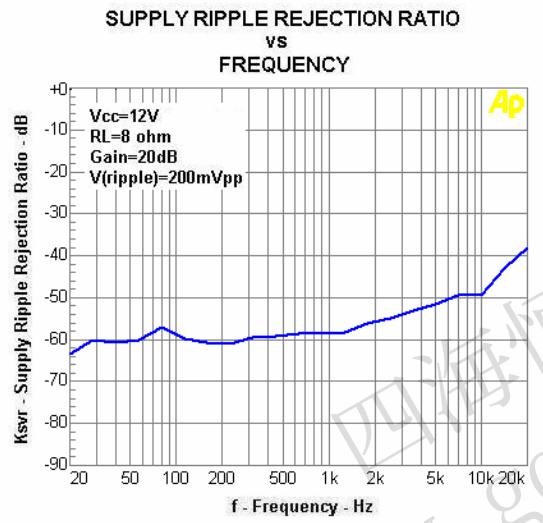

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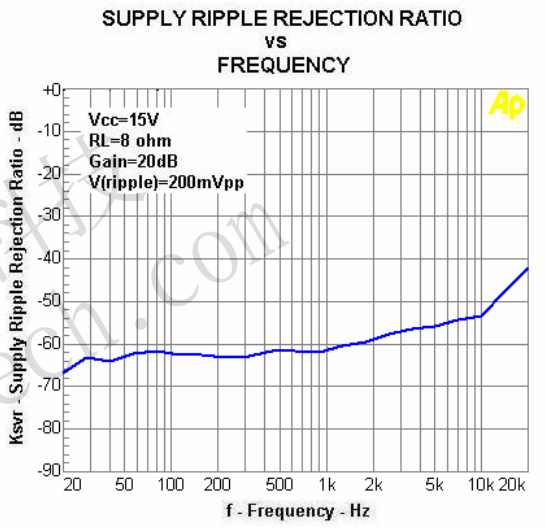

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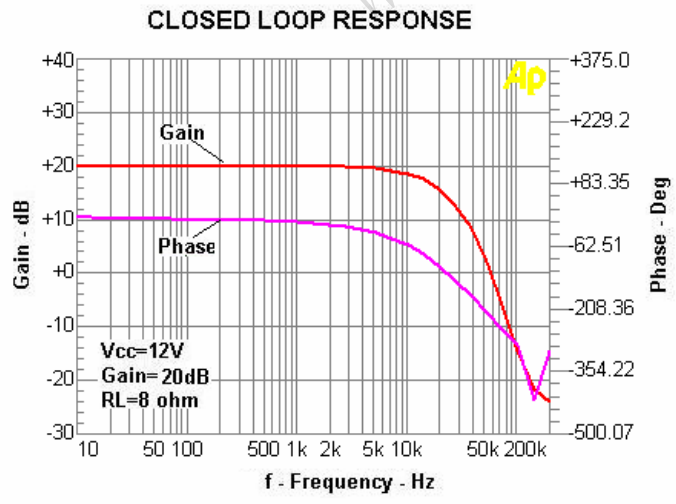

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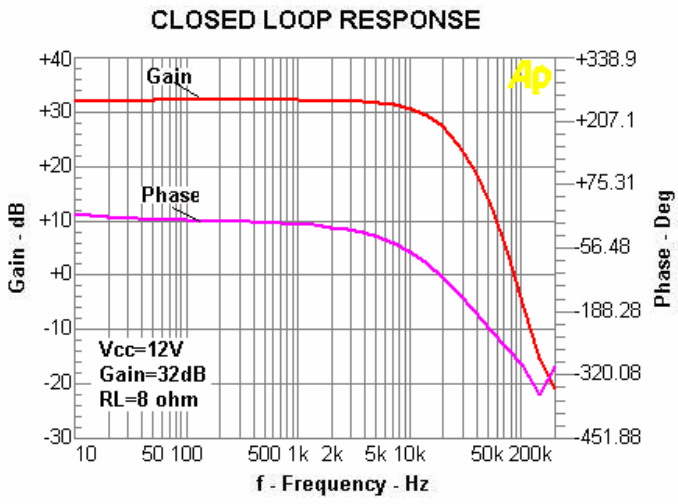

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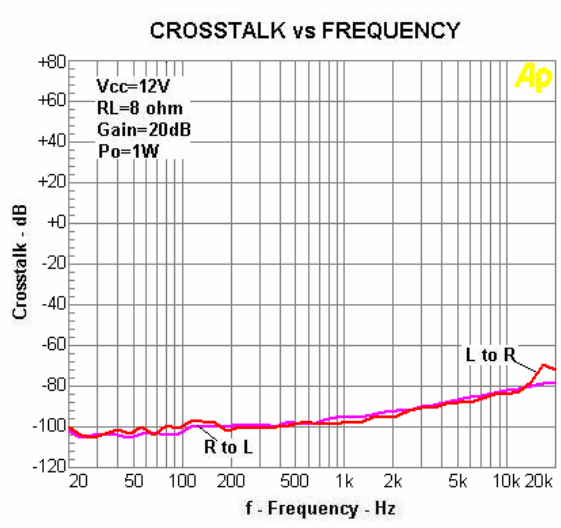

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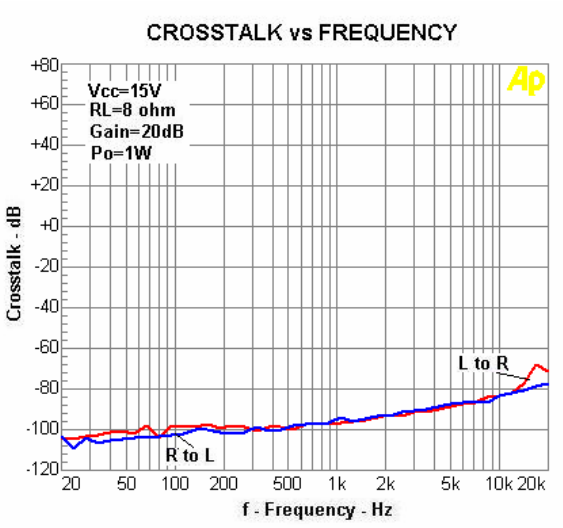

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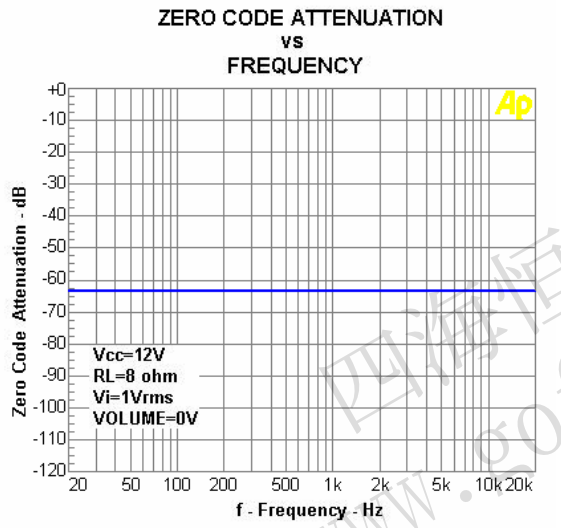

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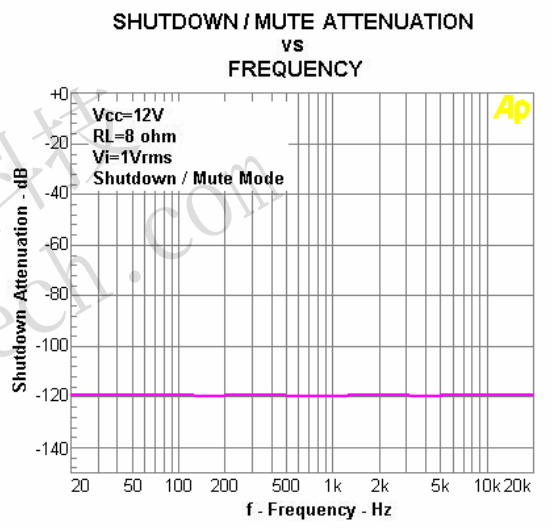

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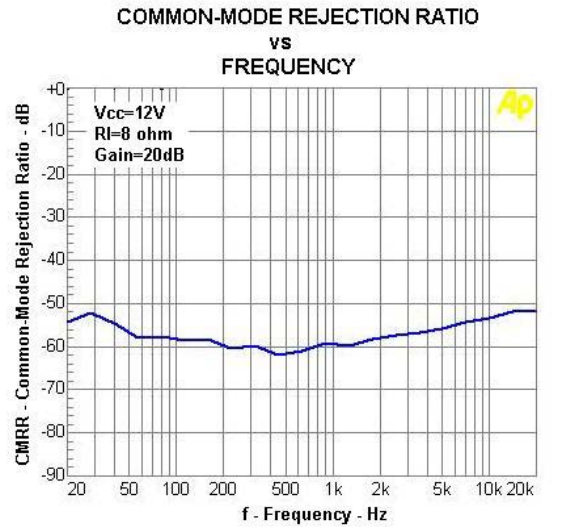

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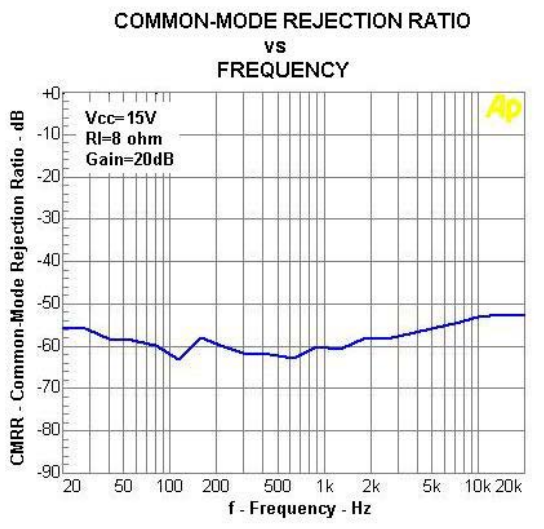


Figure20.

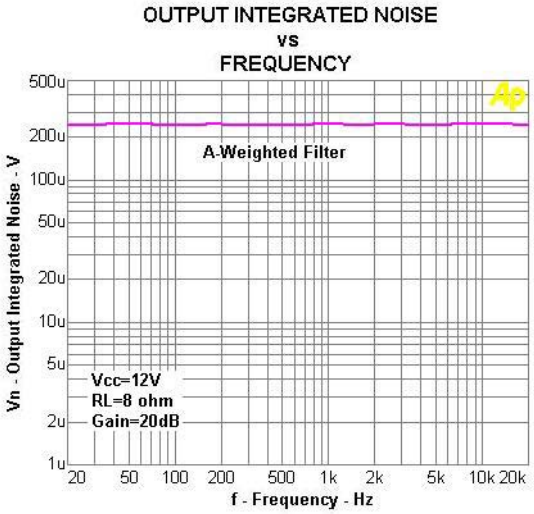


Figure21.

Application Information

Volume Control Operation

The VOLUME terminal controls the internal amplifier gain. This pin is controlled with a dc voltage, which should not exceed VREF. Table 1 lists the gain as determined by the voltage on the VOLUME pin in reference to the voltage on VREF.

If using a resistor divider to fix the gain of the amplifier, the VREF terminal can be directly connected to VREG and a resistor divider can be connected across VREF and AGND. (See Figure 25 in the Application Information Section). For fixed gain, calculate the resistor divider values necessary to center the voltage between the two percentage points given in the first column of Table 1.

If using a DAC to control the class-D gain, VREF and AGND should be connected to the reference voltage for the DAC and the GND terminal of the DAC, respectively. For the DAC application, VREG would be left unconnected to VREF. The reference voltage of the DAC provides the reference to the internal gain circuitry through the VREF input and any fluctuations in the DAC output voltage will not affect the EUA2105 gain. The percentages in the first column of Table 1 should be used for setting the voltages of the DAC when the voltage on the VOLUME terminal is increased. The percentages in the second column should be used for the DAC voltages when decreasing the voltage on the VOLUME terminal. Two lookup tables should be used in software to control the gain based on an increase or decrease in the desired system volume.

If using an analog potentiometer to control the gain, it should be connected between VREF and AGND. VREF can be connected to VREG or an external voltage source, if desired. The 3rd and 4th column in Table 1 should be used to determine the point at which the gain changes depending on the direction that the potentiometer is turned. If the voltage on the center tap of the potentiometer is increasing, the 3rd column in Table 1 should be referenced to determine the trip points. If the voltage is decreasing, the trip points in the 4th column should be referenced.

The trip point, where the gain actually changes, is different depending on whether the voltage on the VOLUME terminal is increasing or decreasing as a result of hysteresis about each trip point. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. A pictorial representation of the volume control can be found in Figure 22.

The timing of the volume control circuitry is controlled by an internal 30-Hz clock. This clock determines the rate at which the gain changes when adjusting the voltage on the external volume control pins. The gain updates every clock cycle (nominally 33 ms) to the next step until the final desired gain is reached. For example, if the EUA2105 is currently in the 0 dB gain step and the VOLUME pin is adjusted for maximum gain at +32 dB, the time required for the gain to reach +32 dB is 36 steps x 33ms/step = 1.188 seconds.

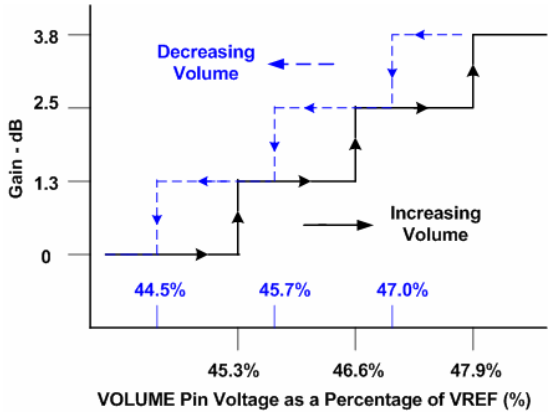


Figure 22. DC Volume Control Operation

FADE Operation

The FADEB terminal is a logic input that controls the operation of the volume control circuitry during transitions to and from the shutdown state and during power-up.

A logic low on this terminal places the amplifier in the fade mode. During power-up or recovery from the shutdown state (a logic high is applied to the $\overline{\text{SHUTDOWN}}$ terminal), the volume is smoothly ramped up from the mute state, -68 dB, to the desired volume setting determined by the voltage on the volume control terminal. Conversely, the volume is smoothly ramped down from the current state to the mute state when a logic low is applied to the $\overline{\text{SHUTDOWN}}$ terminal.

A logic high on this pin disables the volume fade effect during transitions to and from the shutdown state and during power-up. During power-up or recovery from the shutdown state (a logic high is applied to the $\overline{\text{SHUTDOWN}}$ terminal), the transition from the mute state, -68 dB, to the desired volume setting is less than 1 ms. Conversely, the volume ramps down from current state to the mute state within 1 ms when a logic low is applied to the $\overline{\text{SHUTDOWN}}$ terminal.

$\overline{\text{SHUTDOWN}}$ Operation

The EUA2105 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state. $\overline{\text{SHUTDOWN}}$ should never be left unconnected, because amplifier operation would be unpredictable. For the best power-off pop performance, the amplifier should be placed in the shutdown mode prior to removing the power supply voltage.

MUTE Operation

The MUTE pin is an input for controlling the output state of the EUA2105. A logic high on this pin disables the outputs. A logic low on this pin enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade.Quiescent current is listed in the dc characteristics specification table. The MUTE pin should never be left floating.

For power conservation, the $\overline{\text{SHUTDOWN}}$ pin should be used to reduce the quiescent current to the absolute minimum level. The volume will fade, slowly increase or decrease, when leaving or entering the shutdown state if the FADEB terminal is held low. If the FADEB terminal is held high, the outputs will transition very quickly. Refer to the FADEB operation section.

Short-Circuit Protection

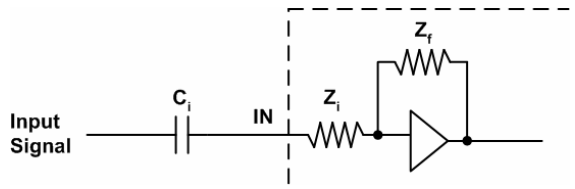
The EUA2105 has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-VCC shorts. When a short circuit is detected on the outputs, the part immediately disables the output drive. This is a latched fault and must be reset by cycling the voltage on the $\overline{\text{SHUTDOWN}}$ pin or MUTE pin.

Thermal Protection

Thermal protection on the EUA2105 prevents damage to the device when the internal die temperature exceeds 150°C. There is a 10°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 40°C. The device begins normal operation at this point with no external system interaction.

Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 80 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.

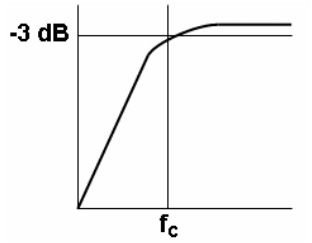


The -3dB frequency can be calculated using Equation 1. Use the Z_I values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \quad \text{---------- (1)}$$

Input Capacitor, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 2.



$$f_c = \frac{1}{2\pi Z_i C_i} \quad \text{----------(2)}$$

The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 64 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad \text{----------(3)}$$

In this example, C_I is 0.12µF; so, one would likely choose a value of 0.22µF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I.

Power Supply Decoupling

The EUA2105 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads.

For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1µF placed as close as possible to the device V_{CC} lead works best. For filtering lower-frequency noise signals, a larger capacitor of 10µF or greater placed near the audio power amplifier is recommended.

BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors, that require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF~1uF ceramic capacitor, rated for at least 16V, must be connected from each output to its corresponding bootstrap input.

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

VCLAMP Capacitors

The EUA2105 also features two regulators used for gate voltage clamping in order to ensure the maximum gate-to-source voltage for the NMOS output transistors is not exceeded. Two 1µF capacitors must be connected from VCLAMPL (pin 13) and VCLAMPR (pin 16) to ground and must be rated for at least 16V. The voltages at the VCLAMP terminals may vary with V_{CC} and may not be used for powering any other circuitry.

Output Pin Snubbers

1nF capacitors in series with 20Ω resistors form the outputs of the EUA2105 IC to ground are switching snubbers. These are illustrated in Figure 23.They linearize switching transitions and reduce overshoot and ringing. By doing so they improve THD+N and EMC. They increase quiescent current by 5 to 15mA depending on power supply voltage.

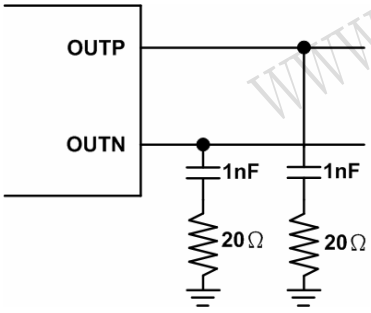


Figure23.

VBYP Capacitor

The internal bias generator (VBYP) nominally provides a 1.4V internal bias for the preamplifier stages. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the VBYP terminal is critical for achieving the best device performance. During power up or recovery from the shutdown state, the VBYP capacitor determines the rate at which the amplifier starts up. The charge rate of the capacitor is calculated using the standard charging formula for a capacitor, I = C x dV/dT. The charge current is nominally equal to 125µA and dV is equal to VBYP. For example, a 1µF capacitor on VBYP would take 10 ms to reach the value of VBYP and turn on outputs. The turn-on time will <30 ms for a 1µF capacitor on the VBYP terminal.

A secondary function of the VBYP capacitor is to filter high-frequency noise on the internal 1.4V bias generator. A value of at least 1µF is recommended for the VBYP capacitor. For the best power-up and shutdown pop performance, the VBYP capacitor should be greater than or equal to the input capacitors.

Using Low-ESR Capacitors

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance. For best performance over the extended temperature range, select X7R capacitors.

Output Filter

Most applications require a ferrite bead filter. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (<1 MHz) EMI-sensitive circuits and/or there are long wires from the amplifier to the speaker.

When both an LC filter and a ferrite bead filter are used, the LC filter should be placed as close as possible to the IC followed by the ferrite bead filter.

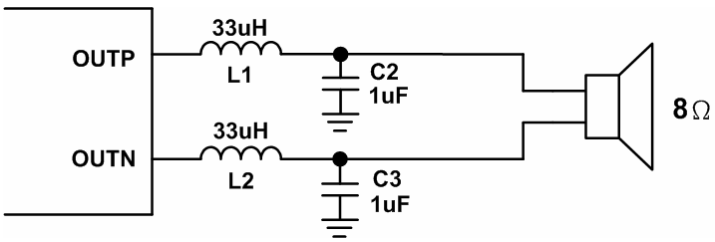


Figure24.

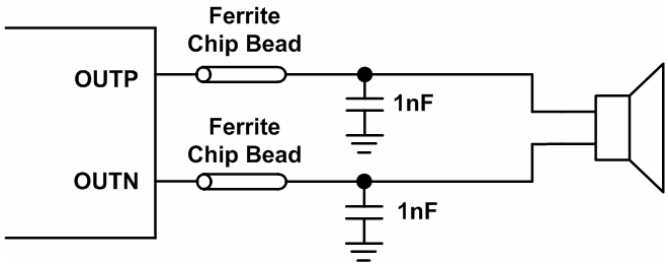


Figure25.

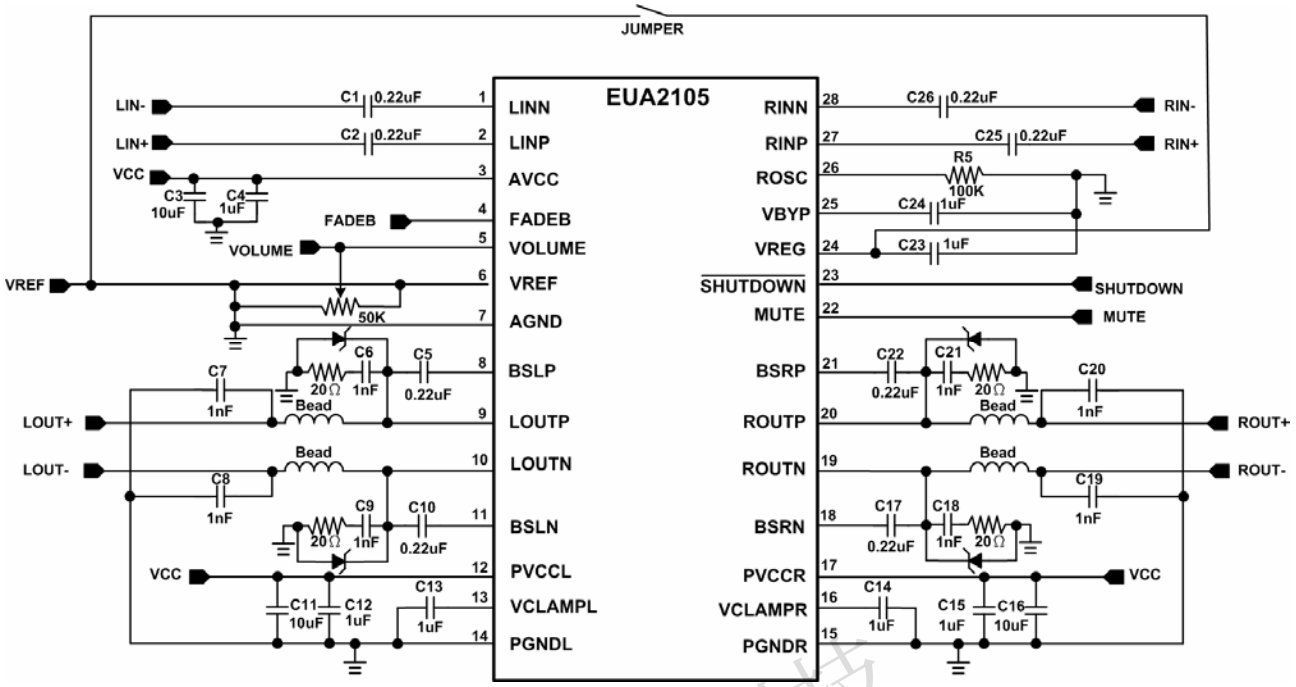
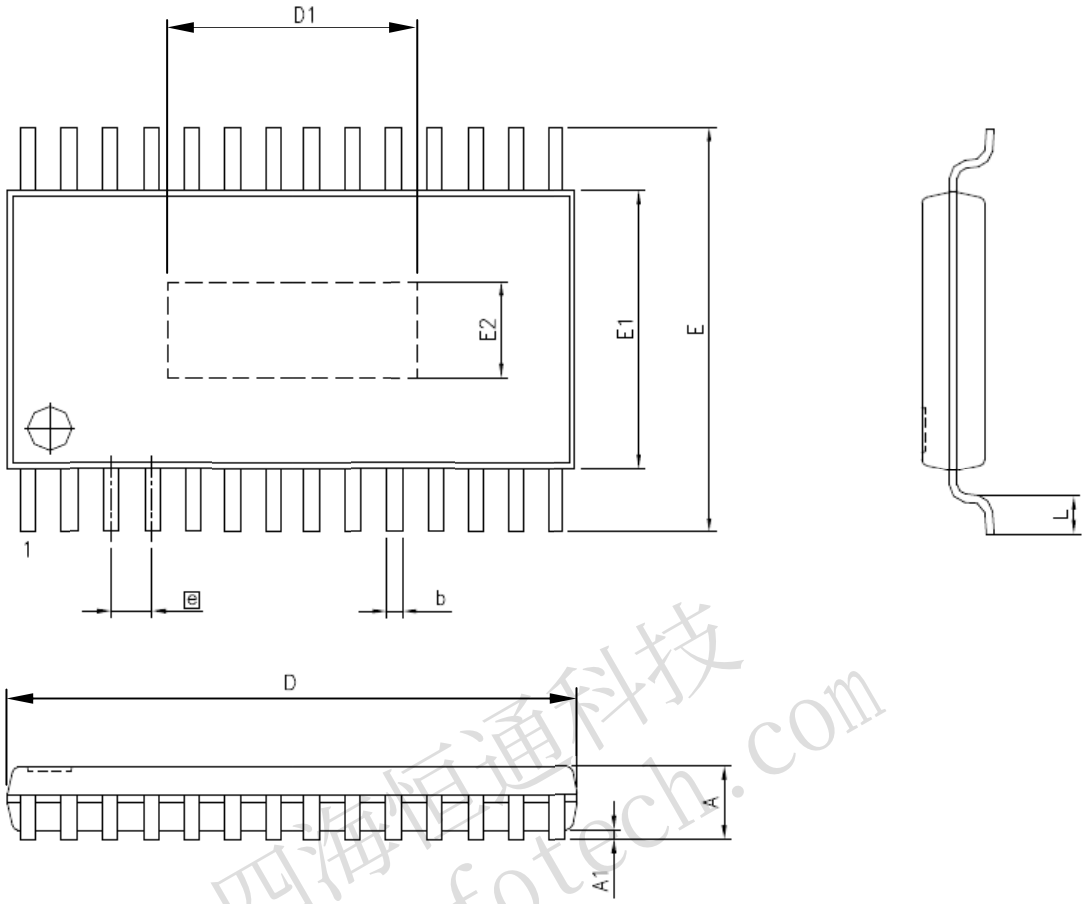


Figure26.

Package Information

TSSOP-28



	MILLIMETERS		INCHES	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	-	1.20	-	0.047
A1	0.00	0.15	0.000	0.006
b	0.19	0.30	0.007	0.012
E1	4.40		0.173	
D	9.60	9.80	0.378	0.386
D1	3.05	3.55	0.120	0.139
E	6.20	6.60	0.244	0.260
E2	2.62	3.12	0.103	0.122
e	0.65		0.026	
L	0.45	0.75	0.018	0.030