SP97508

110MHz 8-BIT FLASH ADC

The SP97508 is an 8-bit flash ECL analog-to-digital converter. It incorporates 256 individual comparators, a reference chain and a full D-type output latch. The ADC is capable of sampling at 100MHz with full (Nyquist) analog bandwidth and has an excellent dynamic performance. A conventional unity mark/space ratio clock can be used and the output data can be programmed for true or inverse binary and twos' complement coding.

FEATURES

- Full Scale Input Bandwidth 120MHz (3dB)
- No Missing Codes
- Production Tested with 30MHz Analog Input
- Low Input Capacitance: 32pF (Max.)
- No External Sample and Hold Needed
- Low Power Consumption: 1.4W (Typ.)
- True/Inverse Binary and Twos' Complement Coding
- Operating Temperature Range: -40°C to +85°C

APPLICATIONS

- Radar Video Digitising
- Instrumentation
- Nucleonics
- Studio Quality Video

ORDERING INFORMATION

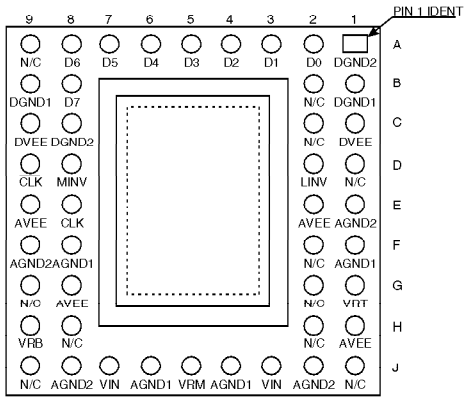
SP97508B HG (Industrial - J-Lead Quad Cerpac)
SP97508B AC (Industrial - Pin Grid Array)

ABSOLUTE MAXIMUM RATINGS

Power supply V_{EE}	0V to -7V
Analog input V_{IN}	+0.5V to V_{EE}
Reference voltages V_{RT}, V_{RM}, V_{RB}	+0.5V to V_{EE}
Reference range V_{RT} - V_{RB}	2.5V
Digital inputs CLK, $\overline{CLK}$, MINV, LINV	+0.5V to -4V
MidRef input current I_{VRM}	-10mA to +10mA
Digital output current I_D	0 to -20mA
Voltage between AGND and DGND	-50mV to +50mV
Voltage between AV_{EE} and DV_{EE}	-50mV to +50mV

THERMAL CHARACTERISTICS

Storage temperature range		-65°C to +150°C
Max. junction operating temperature		+175°C
Lead temperature (soldering 60s)		300°C
SP97508B HG	θ_{JA}	46°C/W
	θ_{JC}	11°C/W
SP97508B AC	θ_{JA}	40°C/W



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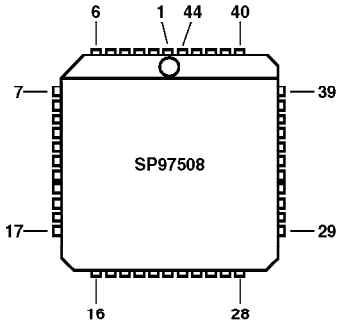

HG44

Pin	Function	Pin	Function	Pin	Function
1	NC	16	DGND	31	AGND
2	LINV	17	DGND	32	V_{IN}
3	NC	18	NC	33	AGND
4	DV_{EE}	19	DV_{EE}	34	V_{RM}
5	DGND	20	MINV	35	AGND
6	DGND	21	NC	36	V_{IN}
7	NC	22	$\overline{CLK}$	37	AGND
8	D0 LSB	23	CLK	38	NC
9	D1	24	NC	39	NC
10	D2	25	V_{RB}	40	NC
11	D3	26	AV_{EE}	41	AV_{EE}
12	D4	27	AV_{EE}	42	AV_{EE}
13	D5	28	NC	43	NC
14	D6	29	NC	44	V_{RT}
15	D7 MSB	30	NC		

Fig.1 Pin connections - top view

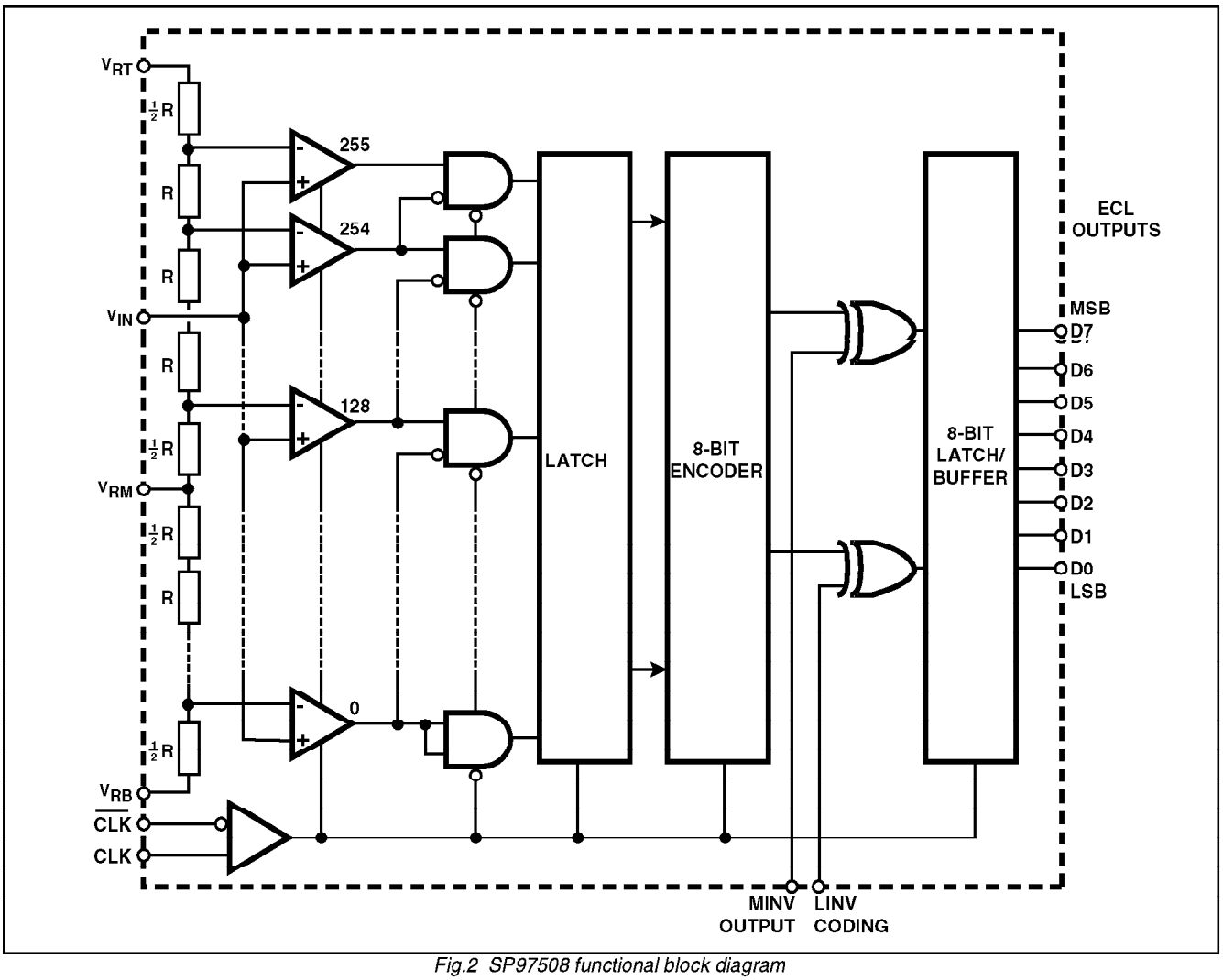

Fig.2 SP97508 functional block diagram

PIN DESCRIPTIONS (Pin numbers refer to HG44 package only)

Pin name	Function
AV_{EE}	Analog V_{EE}, -5.2V (typ.).
LINV	Input pin for polarity inversion of output data bits D0 to D6 (see Table 1).
DV_{EE}	Digital V_{EE}, -5.2V (typ.).
DGND	Digital ground, separated from the analog ground (AGND).
D0-D7	data output pins, ECL levels, D7 = MSB, D0 = LSB. External pulldown resistors are required, e.g. 680Ω to DV_{EE}.
MINV	Input pin for polarity inversion of D7 (MSB) (see Table 1). ECL '0' level is held when MINV is open circuit.
CLK	Clock input pin, ECL levels. Analog input signal, V_{IN}, acquired on rising edge (see Fig.8).
$\overline{CLK}$	Inverse clock input pin , ECL levels.
V_{RB}	Reference voltage (bottom), -2V (typ).
AGND	Analog ground.
V_{IN}	Analog input, range (V_{RT} - V_{RB}) p-p.
V_{RM}	Midpoint of the reference voltage; can be used for linearity adjustment.
V_{RT}	Reference voltage (top), 0V (typ.).
NC	Not Connected. Pins 1 and 18 should be connected to DGND, all others AGND.

RECOMMENDED OPERATING CONDITIONS

Supply voltage	-5.2V ± 0.25V	AGND to DGND	0mV ± 50mV
Reference (V_{RT})	0V ± 0.1V	Analog input	2V p-p max.
Reference (V_{RB})	-2.0V ± 0.2V	Output load	680Ω to -5.2V
AV_{EE} to DV_{EE}	0mV ± 50mV		

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25°C, V_{EE} = -5.2V, V_{RT} = 0V, V_{RB} = -2V, full temperature range = -40°C to +85°C

Characteristic	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min.	Typ.	Max.		
Power Supply								
Supply current	I_{EE}	25	1	180	270	300	mA	
		Full	4	165		310	mA	
Analog Input								
Input bias current	I_{IN}	25	1	80	150	285	µA	
		Full	4	50		350	µA	
Input bandwidth (3dB)		25	4		120		MHz	
Input capacitance	C_{IN}	25	4		29	32	pF	V_{IN} = 0V
Input resistance	R_{IN}	25	4		75		kΩ	V_{IN} = 0V
Reference Chain								
Ladder resistance	R_R	25	1	90	105	135	Ω	
		Full	4	70		155	Ω	
Ladder offset (top & bottom)	$V_{RT/B}$	25	3		7.5		mV	
Clock Input								I/P voltage swing = 1Vp-p
Logic '1' voltage	V_{IH}	25	4	-3.05		DGND	V	
Logic '0' voltage	V_{IL}	25	4	-3.85		-0.8	V	
Logic '1' current	I_{IH}	25	1			380	µA	V_{IH} = -0.8V
		Full	4	310	360	390	µA	V_{IH} = -0.8V
Logic '0' current	I_{IL}	25	4			280	µA	V_{IL} = -1.8V
		Full	4	220	260	290	µA	V_{IL} = -1.8V
Min. pulse width (high)		25	4		3		ns	
Min. pulse width (low)		25	4		2.3		ns	
Digital Outputs								
Logic '1' voltage	V_{OH}	25	1	-0.90	-0.83		V	R_L = 680Ω to DV_{EE}
		Full	4	-1.00			V	
Logic '0' voltage	V_{OL}	25	4		-1.80	-1.90	V	R_L = 680Ω to DV_{EE}
		Full	4			-1.65	V	
Switching Performance								
Max. conversion rate	f_C	25	4	110			MHz	f_{IN} = 50MHz at FS
Aperture delay	t_{ad}	25	5		1.9		ns	
Aperture uncertainty	t_{au}	25	4		30		ps rms	
Output data delay	t_d	25	4		2.9		ns	R_L = 680Ω to DV_{EE}
Output data rise time	t_r	25	4		2.0		ns	R_L = 680Ω to DV_{EE}
Output data fall time	t_f	25	4		1.6		ns	R_L = 680Ω to DV_{EE}
Output data time skew	t_s	25	4		0.4		ns	R_L = 680Ω to DV_{EE}
Static Performance								f_C = 4MHz, f_{IN} = 1kHz ramp
Differential non-linearity	DNL	25	1	-0.85	±0.5	0.85	LSB	No missing codes
		Full	4	-1.0		1.0	LSB	No missing codes
Integral non-linearity	INL	25	1	-1.4		1.3	LSB	
		Full	4	-1.8		1.6	LSB	
Missing codes		25	1	No missing codes				Guaranteed
Gain error		25	1	-1.5		1.5	%FS	
Offset error		25	1	-15		0	mV	
Dynamic Performance								f_C = 100MHz
Transient response (rise)		25	4		2.4		ns	} f_{IN} = 50MHz
Transient response (fall)		25	4		2.1		ns	} square wave at FS
Slew rate			4		1.0		V/ns	}
Differential non-linearity	DNL	25	1	-0.9		1.4	LSB	} f_{IN} = 30MHz
Integral non-linearity	INL	25	1	-3.0		3.0	LSB	} sinewave at FS
Signal-to-noise ratio	SNR	25	4		45.8		dB	f_{IN} = 1MHz at FS
		25	1	41	44.5		dB	f_{IN} = 10MHz at FS
		25	4		39.0		dB	f_{IN} = 30MHz at FS
Total harmonic distortion	THD	25	4		53.5		dBc	f_{IN} = 1MHz at FS
		25	1	46	48.5		dBc	f_{IN} = 10MHz at FS
		25	4		40.4		dBc	f_{IN} = 30MHz at FS
Effective number of bits	ENCOB	25	4		7.3		bits	f_{IN} = 1MHz at FS
		25	1	6.5	7.1		bits	f_{IN} = 10MHz at FS
		25	4		6.2		bits	f_{IN} = 30MHz at FS
Bit error rate	BER	25	4		1 in 10^9			f_{IN} = 50MHz at $\frac{3}{4}$ FS

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis is 3dB down on the DC level.

Aperture Delay

The delay between the rising edge of the CLOCK signal and the instant at which the analog input is sampled.

Aperture Jitter

The sample-to-sample variation in aperture delay.

Bit Error Rate (BER)

The number of spurious code errors produced for any given input sinewave frequency at a given clock frequency. In this case it is the number of codes occuring outside the histogram cusp for a $^3/_4$ FS sinewave.

Differential Non-Linearity (DNL)

The deviation of any code width from ideal 1LSB step.

Effective Number of Bits (ENOB)

This is a measure of the device's dynamic performance and may be obtained from the SNR or form a sine wave curve fit test, according to the following expressions:

$$\text{ENOB} = \frac{\text{SNR-1.76}}{6.02} \quad \text{or} \quad \text{ENOB} = \text{N-log}_2 \frac{\text{rms error (actual)}}{\text{rms error (ideal)}}$$

where N is the conversion resolution and the rms error is the deviation of the output from an input sine wave.

Integral Non-Linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Output Delay

The delay between the 50% point of the falling edge of the clock signal and the 50% point of any data output change.

Reference Ladder Offset

The voltage error at the ends of the resistor chain caused by the end terminations, the lead frame and the bond wire.

Signal-to-Noise Ratio (SNR)

The ratio of the RMS signal amplitude to the RMS value of 'noise' which is defined as the sum of all other spectral components, including harmonics but excluding DC with a full scale analog input signal.

Total Harmonic Distortion (THD)

The RMS value of all the harmonics compared with the RMS value of the fundamental.

Transient Response

The time required by the outputs to move from 10(90)% to 90(10)% of the full scale range.

Test Levels

- **Level 1** - 100% production tested at 25°C
- **Level 2** - 100% production tested at 25°C and sample tested at specified temperatures
- **Level 3** - Sample tested only
- **Level 4** - Parameter is guaranteed by characterisation or design
- **Level 5** - Parameter is a typical value only

APPLICATION NOTES

Analog Input (Figs.3, 4 and 5)

The maximum amplitude and offset of the input is defined by the reference voltages (V_{RB} to V_{RT}). The optimum input is 2V p-p with a DC offset of -1V. The analog input circuit of the SP97508 consists of 256 buffered comparator inputs, as shown in Fig. 3.

The internal buffering to the device results in the typical input characteristics of Figs. 4 and 5. The dependence of input capacitance on voltage level is typical of flash converters and so requires that the analog input is driven from a low impedance source such as the SL9999.

Failure to drive the input capacitance properly causes increased levels of harmonic distortion, most noticeable in the second harmonic.

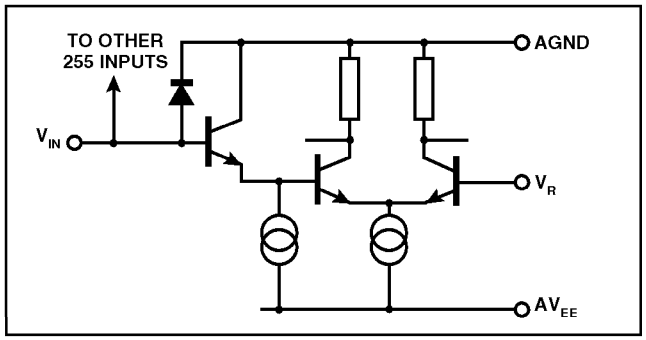

Fig.3 Analog input

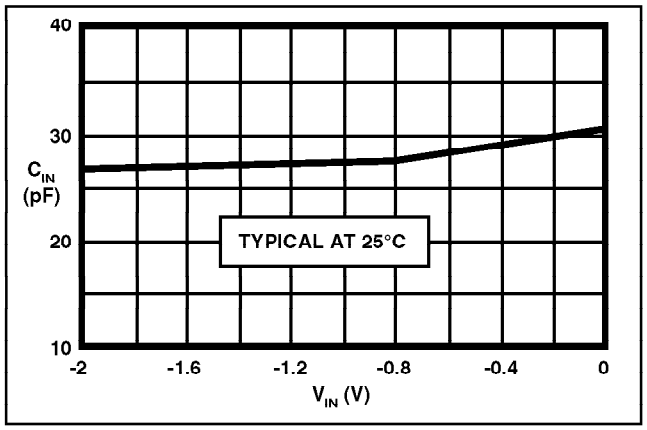

Fig.4 Analog input capacitance

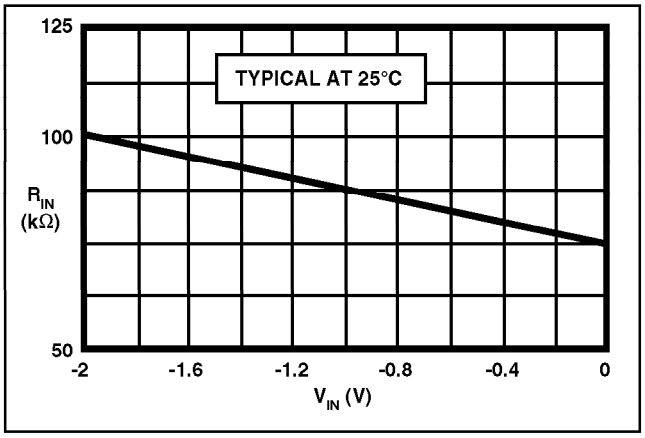

Fig.5 Analog input resistance (AC)

Reference Pins (Fig. 6)

Between V_{RT} and V_{RB} there are 256 series resistors forming the reference chain. The total resistance may be between 90Ω and 120Ω. A mid-reference pin (V_{RM}) is also provided as an option for precision setting of integral linearity. Both V_{RM} and V_{RB} should be adequately decoupled to analog ground. For optimum performance, V_{RT} is connected directly to analog ground and V_{RB} is driven from a -2V DC supply. For precise reference setting, this supply should be adjustable by ±0.2V.

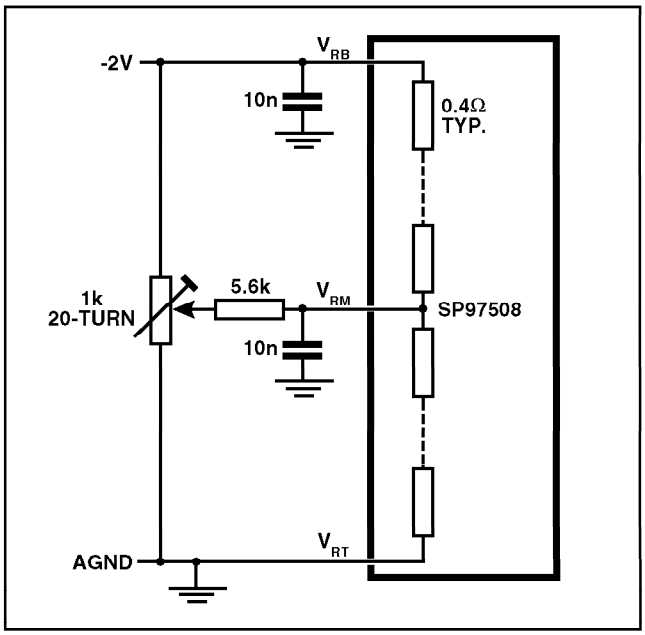

Fig.6 Reference connections

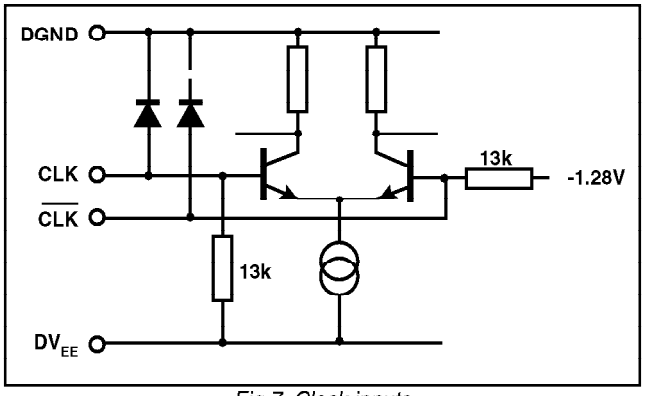

Fig.7 Clock inputs

Clock Inputs CLK and $\overline{CLK}$ (Figs. 7 and 8)

The SP97508 can be driven from either differential or single-ended ECL clocks. In either mode, the clock lines should be terminated with the line's characteristic impedance close to the device clock pins. For full 100MHz operation, a conventional unity mark/space ratio clock can be used.

Single-ended drive can be simply provided by adding a 1nF chip or encapsulated chip capacitor from the $\overline{CLK}$ pin to DGND. The $\overline{CLK}$ pin will then self-bias at -1.28V, which is the mid-threshold for ECL. The device can then be clocked by an ECL signal into the CLK input.

Timing (Fig.8)

The analog input is acquired by the device shortly after the rising edge of the CLK signal. The internal latch causes a one cycle delay, hence the output data is valid one clock cycle after the acquisition of the analog signal.

The output data is further delayed by the clock-to-output delay (t_D = 2.9ns typ.). This gives the advantage that the same timing and phase of the SP97508 CLK signal can be used to acquire the output data.

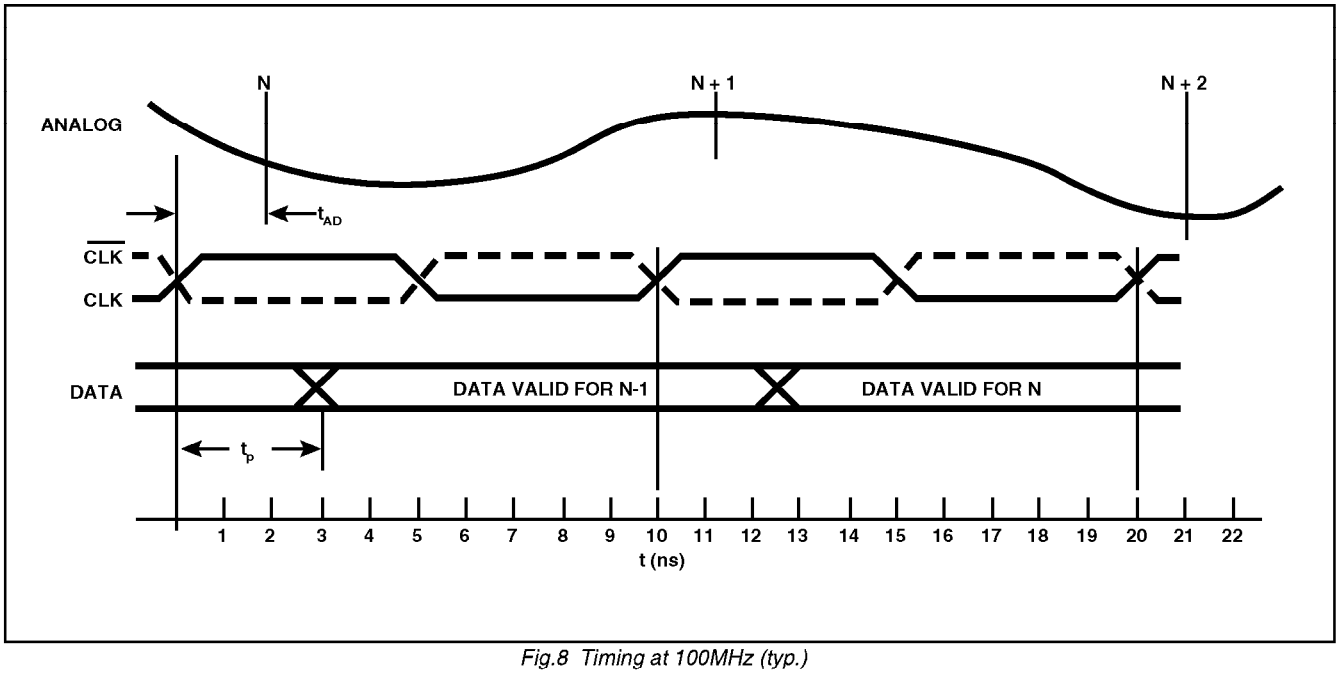

Fig.8 Timing at 100MHz (typ.)

Output Coding (Table 1 and Fig.9)

With MINV and LINV left open circuit, the output will be coded in standard binary with all 1s code corresponding to the most positive input $V_{IN}=V_{RT}=0V$.

An inverse binary output can be provided by connecting both MINV and LINV to ground.

Two's complement coding (inverted MSB) can be provided by connecting only the MINV pin to ground and inverse two's complement coding can be achieved by connecting only the LINV pin to ground.

V_{IN}	Binary MINV = O/C (0) LINV = O/C (0)	Inv 2s' comp. MINV = O/C (0) LINV = GND (1)	2s' comp. MINV = GND (1) LINV = O/C (0)	Inv binary MINV = GND (1) LINV = GND (1)
0V	111 11	100 00	011 11	000 00
	111 10	100 01	011 10	000 01
	-	-	-	-
	-	-	-	-
	-	-	-	-
	100 00	111 11	000 00	011 11
	011 11	000 00	111 11	100 00
	-	-	-	-
	-	-	-	-
	-	-	-	-
	000 01	011 10	100 01	111 10
-2V	000 00	011 11	100 00	111 11

Table 1

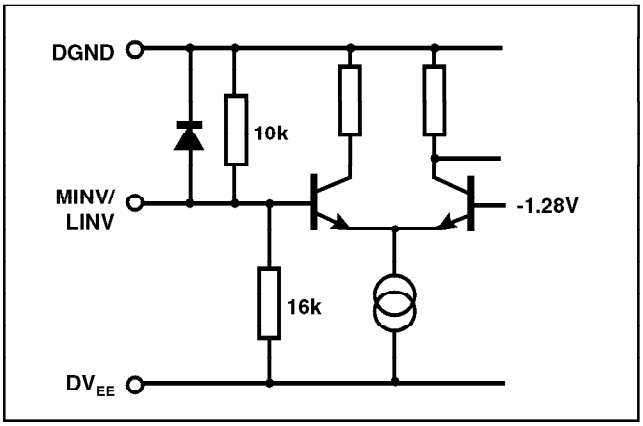

Fig.9 MINV/LINV input

8-Bit ECL Outputs (Fig.10)

The outputs are standard ECL open emitters and therefore require pull-down resistors connected from the outputs to -5.2V or -2V digital supply. Single in-line resistors of value 680Ω to 1kΩ are recommended for termination to DV_{EE}. The outputs are capable of driving 200Ω terminations connected to a -2V supply.

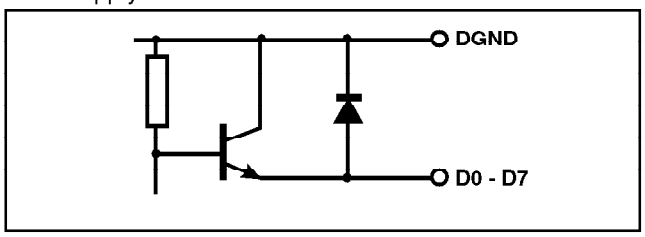

Fig.10 Digital output

TYPICAL PERFORMANCE CHARACTERISTICS

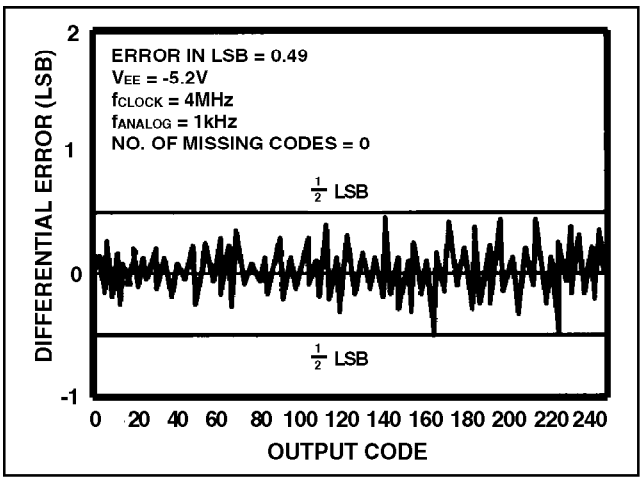

Fig.11 Static differential linearity in LSB: typical production device

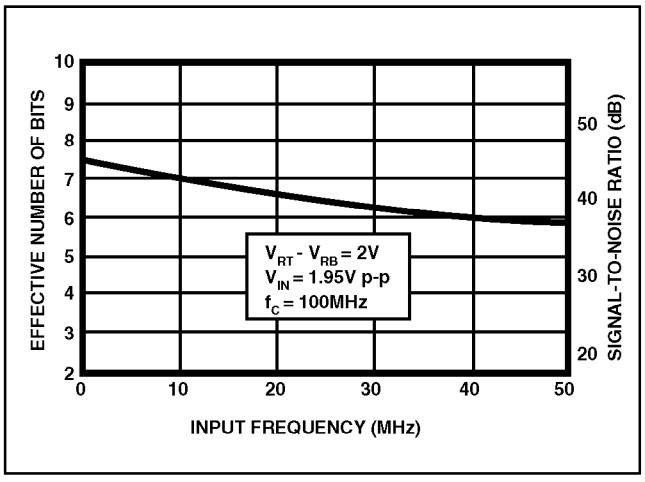

Fig.12 Effective number of bits (ENOB) and signal-to-noise ratio (SNR) v. input frequency

CIRCUIT BOARD CONSTRUCTION

As with most PCB construction for analog-to-digital conversion, the best performance from the SP97508 can be achieved by separating the ground plane into two sections: analog ground (AGND), and digital ground (DGND). This aids the device performance by reducing the degree of noise due to digital switching fed back to the analog section of the converter.

The digital noise is produced mainly by the ECL binary outputs, which, ideally, should be terminated by a 680Ω load to the -5.2V digital supply, DV_{EE}.

The device supplies are also a source of digital feedback, as they can be modulated by the digital output current. It is wise, therefore, to decouple the SP97508 close to the device supply pins with good quality, high frequency capacitors.

Notes on Construction

1. Use split analog and digital ground planes connected together close to the device. Do not run the analog input next to the clock or data lines.
2. All NC pins must be grounded: connect pins 1 and 18 to DGND, all others to AGND.
3. Connect digital and analog supplies together at a point on the PCB away from the device.
4. Use 10nF capacitors for supply decoupling.
5. Use stripline techniques for siginal paths longer than 5cm (2 inches)
6. Use 4.7µF electrolytic capacitors to decouple the -5.2V V_{EE} supplies

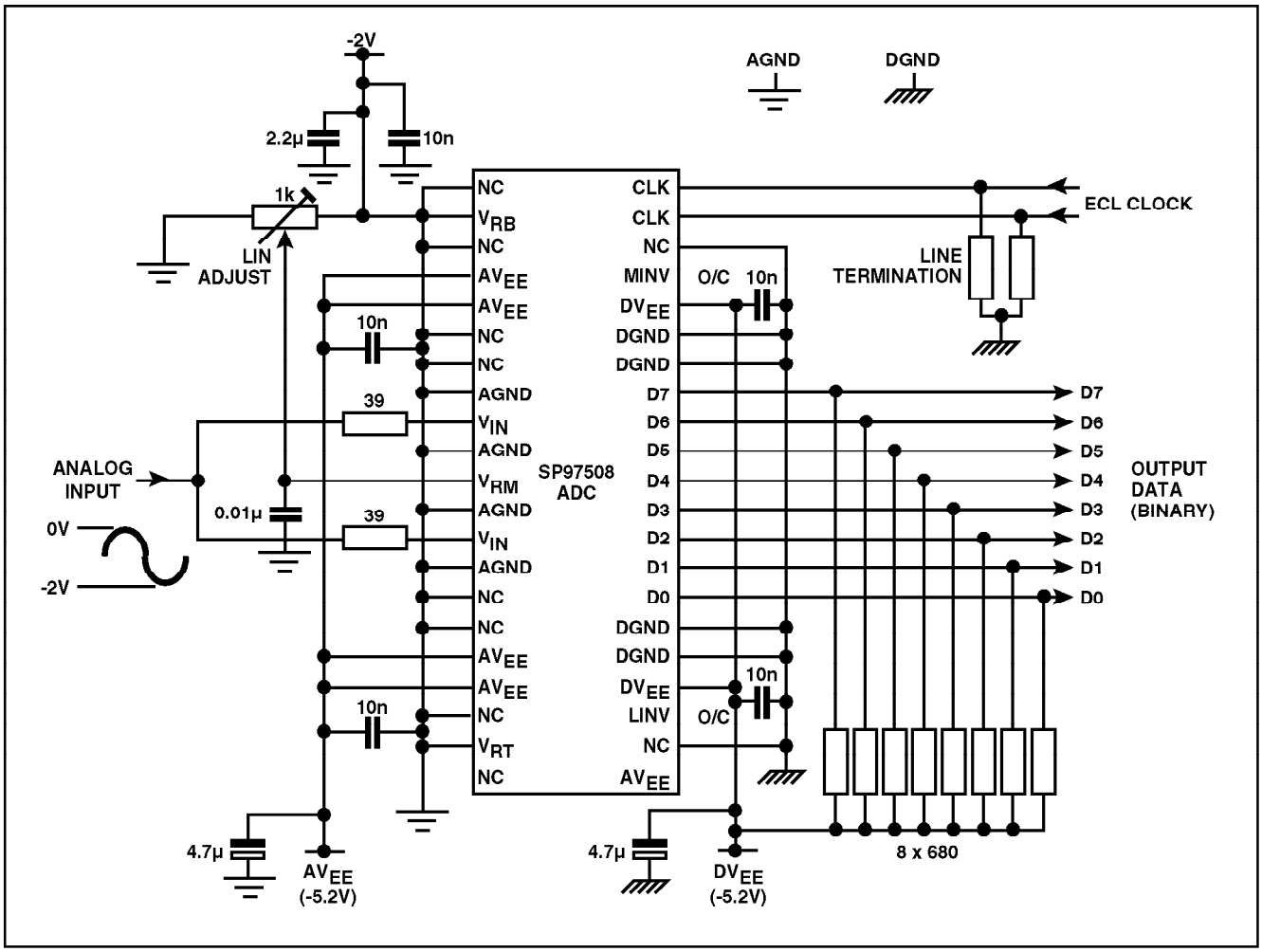

Fig.13 Test and Application circuit

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