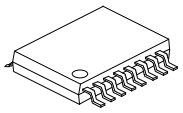
VGA PORT COMPANION CIRCUIT



SSOP-16

■ DESCRIPTION

The UTC **CCVGA7C5** is an ESD solution for the VGA port connector. This device integrates ESD protection for all signals,

Two non-inverting drivers provide buffering for the HSYNC and VSYNC signals from the video controller IC. These buffers accept TTL input levels and convert them to CMOS output levels that swing between Ground and V_{CC}. These drivers have a nominal 60Ω output impedance to match the characteristic impedance of the HSYNC and VSYNC lines of the video cables typically used. The inputs of these drivers also have high impedance pull−ups (50kΩ nom.) pulling up to the VAUX rail.

In addition, the DDC_CLOCK and DDC_DATA channels have 1.8kΩ resistors pulling these inputs up to the main 5V (V_{CC}) rail.

The upper ESD diodes for the R, G and B channels are connected to a separate supply rail (V_{RGB}) to facilitate interfacing to graphics controller ICs with low voltage supplies. The remaining channels are connected to the main 5 V rail (V_{CC}). The lower diodes for the R, G and B channels are also connected to a dedicated ground pin (GNDA) to minimize crosstalk due to common ground impedance.

ESD protection is implemented with current steering diodes designed to safely handle the high peak surge currents associated with the IEC−1000−4−2 Level−4 ESD Protection Standard (±8kV contact discharge). When the channels are subjected to an electrostatic discharge, the ESD current pulse is diverted via the protection diodes into the positive supply rails or ground where they may be safely dissipated.

■ FEATURES

* 7 Channels of ESD Protection Designed to Meet IEC−1000−4−2 Level−4 ESD Requirements (±8kV Contact Discharge)
* Three Independent Supply Pins (V_{CC}, V_{RGB} and V_{AUX}) to Facilitate Operation with Sub−Micron Graphics Controller ICs
* Very Low Loading Capacitance from ESD Protection Diodes at Less than 5pF Typical
* TTL to CMOS Level−Translating Buffers for the HSYNC and VSYNC Lines
* High impedance Pull−Ups (50kΩ Nominal to VAUX) for HSYNC and VSYNC Inputs
* Pull−Up Resistors (1.8kΩ Nominal to V_{CC}) for DDC_CLK and DDC_DATA Lines

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
CCVGA7C5L-R16-T	CCVGA7C5G-R16-T	SSOP-16	Tube
CCVGA7C5L-R16-R	CCVGA7C5G-R16-R	SSOP-16	Tape Reel

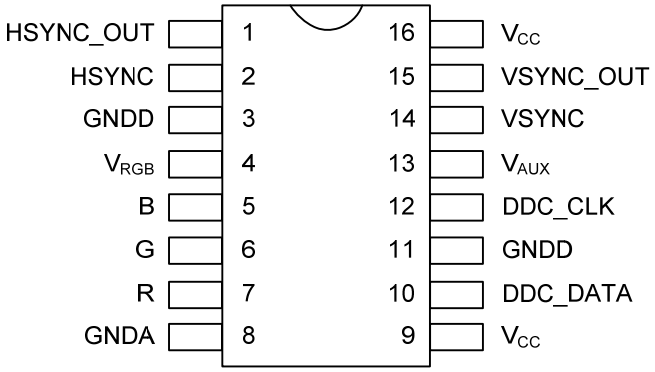
CCVGA7C5L-R16-T

(1)Packing Type — (1) T: Tube, R: Tape Reel

(2)Package Type — (2) R16: SSOP-16

(3)Lead Free — (3) L: Lead Free, G: Halogen Free

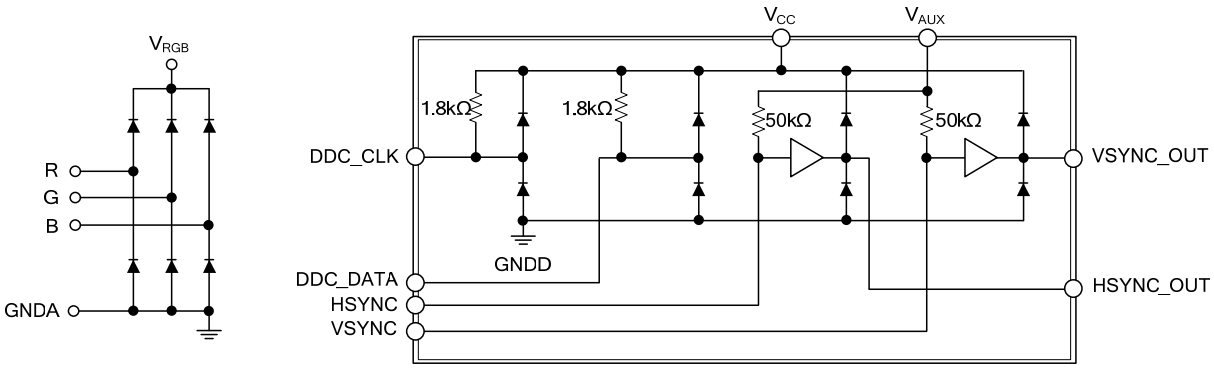
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	HSYNC_OUT	Horizontal sync signal buffer output. Connects to the video connector side of the horizontal sync line.
2	HSYNC	Horizontal sync signal buffer input. Connects to the VGA Controller side of the horizontal sync line.
3, 11	GNDD	Digital ground reference supply pin.
4	V_{RGB}	V_{RGB} supply pin. This is an isolated supply pin for the R, G and B ESD protection circuits.
5	B	Blue signal video protection channel. This pin is typically tied to the B video line between the VGA controller device and the video connector.
6	G	Green signal video protection channel. This pin is typically tied to the G video line between the VGA controller device and the video connector.
7	R	Red signal video protection channel. This pin is typically tied to the R video line between the VGA controller device and the video connector.
8	GNDA	Analog ground reference supply pin.
9, 16	V_{CC}	V_{CC} supply pin. This is the main supply input for the DDC_CLK and DDC_DATA pullup resistors and ESD protection circuits. It is also connected to the sync buffers and to the ESD protection diodes present on the HSYNC_OUT and VSYNC_OUT lines.
10	DDC_DATA	DDC data pin.
12	DDC_CLK	DDC clock pin.
13	V_{AUX}	V_{AUX} supply pin. This is the supply input for the 50kΩ pullups connected to the HSYNC and VSYNC buffer inputs.
14	VSYNC	Vertical sync signal buffer input. Connects to the VGA Controller side of the vertical sync line.
15	VSYNC_OUT	Vertical sync signal buffer output. Connects to the video connector side of the vertical sync line.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage Inputs		V_{CC}, V_{RGB}, V_{AUX}	GND-0.5 ~ +6.0	V
Diode Forward Current (One Diode Conducting at a Time)			20	mA
DC Voltage at Inputs	R, G, B		GND-0.5 ~ V_{RGB} +0.5	V
	HSYNC, VSYNC		GND-0.5 ~ V_{AUX} +0.5	V
	DDC_CLK, DDC_DATA		GND-0.5 ~ V_{CC} +0.5	V
Package Power Rating			750	mW
Operating Temperature Range		T_{OPR}	0 ~ +70	°C
Storage Temperature Range		T_{STG}	−40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ STANDARD OPERATING CONDITIONS

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Main Supply Voltage		V_{CC}		4.5		5.5	V
RGB Supply Voltage		V_{RGB}		1.7		3.7	V
Auxiliary Supply Voltage		V_{AUX}		2.9		3.7	V
Logic High Input Voltage (Note)		V_{IH}		2.0			V
Logic Low Input Voltage (Note)		V_{IL}				0.8	V
Input Voltage	RGB	V_I		0		V_{RGB}	V
	HSYNC, VSYNC			0		V_{AUX}	V
	DDC_CLK, DDC_DATA			0		V_{CC}	V
High Level Output Current (Note 1)		I_{OH}				-8	mA
Low Level Output Current (Note 1)		I_{OL}				8	mA
Free−Air Operating Temperature		T_A		0		+70	°C

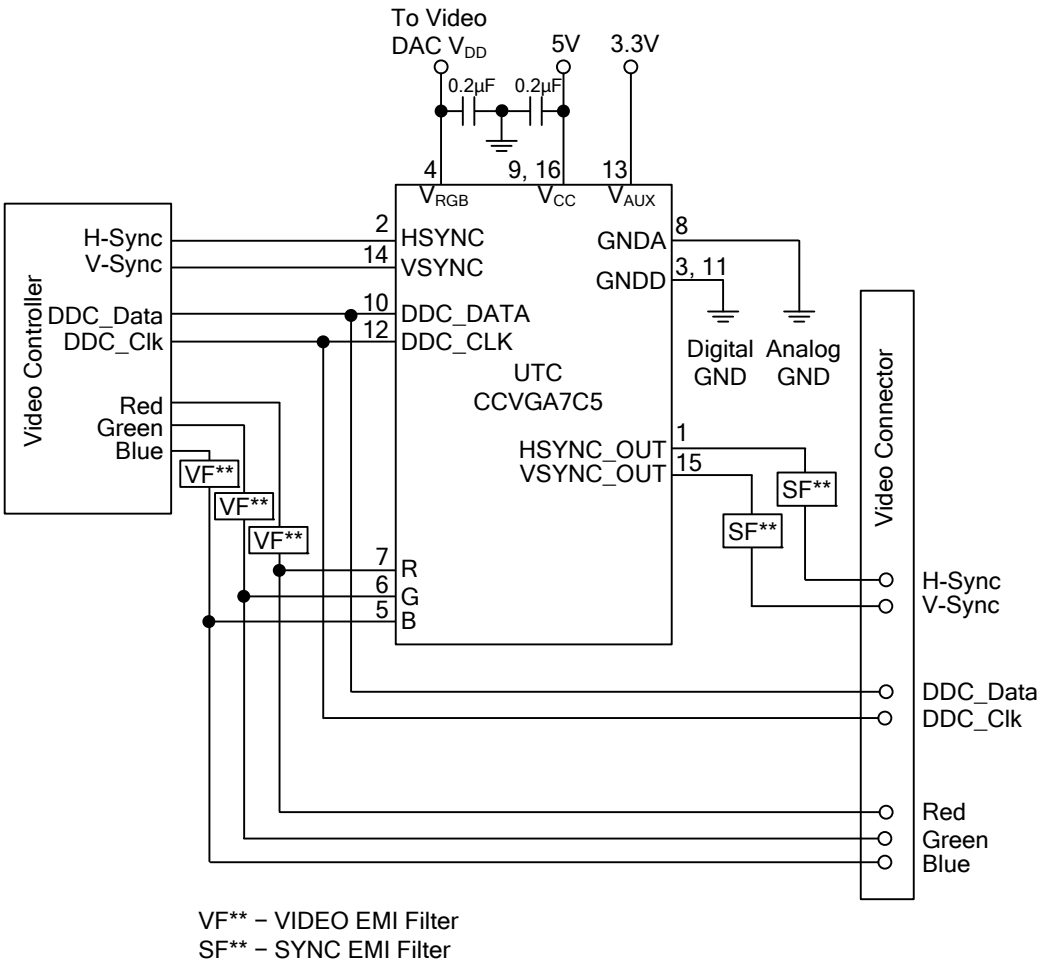
Note: These parameters apply only to the HSYNC and VSYNC signals.

■ ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Diode Forward Voltage		V_F	I_F=10mA			1.0	V
Logic High Output Voltage		V_{OH}	I_{OH}=-4mA, V_{CC}=4.5V	4.0			V
Logic Low Output Voltage		V_{OL}	I_{OL}=4mA, V_{CC}=4.5V			0.4	V
Input Current	R, G and B Pins	I_{IN}	V_{RGB}=3.63V, V_{IN}=V_{RGB} or GND			±1	μA
	HSYNC, VSYNC Pins		V_{AUX}=3.63V, V_{IN}=V_{AUX}			±1	μA
	HSYNC, VSYNC Pins		V_{AUX}=3.63V, V_{IN}=GND	-30.0	-72.5	-95.0	μA
V_{CC} upply Current		I_{CC}	V_{CC}=5.5V, V_{AUX}=V_{RGB}=2.97V, All Inputs and Outputs Floating		35	100	μA
V_{RGB} supply Current		I_{RGB}	R, G and B Pins at V_{CC} r GND, All Inputs and Outputs Floating			10	μA
Input Capacitance	R, G and B pins	C_{IN}	Note 2 Applies for All Cases		5		pF
	HSYNC, VSYNC pins				10		pF
	DDC_DATA, DDC_CLK pins				5		pF
Pull−up Resistance DDC_DATA, DDC_CLK pins		R_{PU}		1.52	1.80	1.98	kΩ
ESD Withstand Voltage		V_{ESD}	V_{CC}=5 V, V_{RGB}=3.3V, V_{AUX}=3.3 V	±8			kV
SYNC Buffer L≥H Propagation Delay		t_{PLH}	C_L=50pF, V_{CC}=5.0V, R_L=500Ω (Note 3)		7.0	15.0	ns
SYNC Buffer H≥L Propagation Delay		t_{PHL}	C_L=50pF, V_{CC}=5.0V, R_L=500Ω (Note 3)		7.0	15.0	ns
SYNC Buffer Output Rise & Fall Times		t_R, t_F	C_L=50pF, V_{CC}=5.0V, R_L=500Ω (Note 3)		7.0		ns

Notes: 1. All parameters specified over standard operating conditions unless otherwise noted.
2. Measured at 1MHz. R/G/B inputs biased at 1.65V with V_{RGB}=3.3V. DDC_CLK and DDC_DATA biased at 2.5V with V_{CC}=5V. HSYNC and VSYNC inputs biased at V_{AUX} or GND with V_{AUX}=3.3V and V_{CC}=5V.
3. Applicable to the SYNC buffers only. Input signals swing between 0V and 3.0V, with rise and fall times ≤5 ns. Guaranteed by correlation to buffer output drive currents.

■ TYPICAL APPLICATION CIRCUIT



Typical Connection Diagram

GNDA, the negative voltage rail for the R, G and B diodes is not connected internally to GNDD. GNDA should ideally be connected to the ground of the video DAC IC. This will prevent any ground bounce caused by digital signals from injecting noise onto the R, G and B signals. Analog GND and digital GND are typically connected on the printed circuit board.