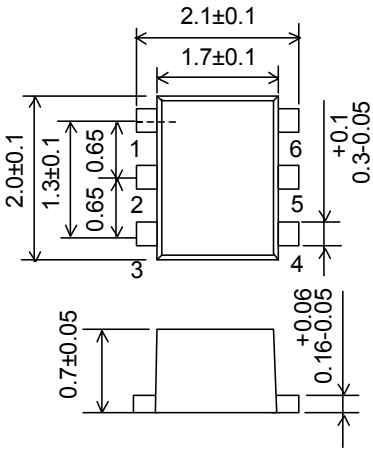
TOSHIBA Multi-Chip Device
Silicon P-Channel MOS Type + N-Channel MOS Type

SSM6E02TU

○Power Management Switch Applications

- 1.5 V drive
- P-channel MOSFET and N-channel MOSFET incorporated into one package.
- Low power dissipation due to P-channel MOSFET that features low $R_{DS\ (ON)}$ and low-voltage operation

Unit: mm



1.Nch source	4.Pch source
2.Pch drain	5.Nch gate
3.Pch drain	6.Pch gate
	Nch drain
UF6	
JEDEC	—
JEITA	—
TOSHIBA	2-2T1D

Weight: 7.0 mg (typ.)

Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	−20	V
Gate-Source voltage		V_{GSS}	± 8	V
Drain current	DC	I_D	-1.8	A
	Pulse	I_{DP} (Note 1)	-3.6	

Q2 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	20	V
Gate-Source voltage		V_{GSS}	± 10	V
Drain current	DC	I_D	0.1	A
	Pulse	I_{DP} (Note 1)	0.2	

Absolute Maximum Ratings (Q1, Q2 common) (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Drain power dissipation	P_D (Note 2)	0.5	W
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width limited by maximum channel temperature.

Note 2: Mounted on an FR4 board (25.4 mm × 25.4 mm × 1.6 t, Cu pad: 645 mm^2)

Q1 Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −1 mA, V_{GS} = 0	−20	—	—	V
		$V_{(BR)\ DSX}$	I_D = −1 mA, V_{GS} = +8 V	−12	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = −20 V, V_{GS} = 0	—	—	−10	μA
Gate leakage current		I_{GSS}	V_{GS} = ± 8 V, V_{DS} = 0	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = −3 V, I_D = −1 mA	−0.3	—	−1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −3 V, I_D = −0.9 A (Note 3)	2.7	5.4	—	S
Drain-Source on-resistance		$R_{DS\ (ON)}$	I_D = −1.0 A, V_{GS} = −2.5 V (Note 3)	—	95	136	mΩ
			I_D = −1.0 A, V_{GS} = −1.8 V (Note 3)	—	122	204	
			I_D = −0.1 A, V_{GS} = −1.5 V (Note 3)	—	137	364	
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 f = 1 MHz	—	568	—	pF
Output capacitance		C_{oss}		—	75	—	
Reverse transfer capacitance		C_{rss}		—	67	—	
Switching time	Turn-on time	t_{on}	V_{DD} = −10 V, I_D = −0.9 A V_{GS} = 0 to −2.5 V, R_G = 4.7 Ω	—	29	—	ns
	Turn-off time	t_{off}		—	39	—	
Total gate charge		Q_g	V_{DS} = −16 V, I_{DS} = -1.8 A, V_{GS} = − 4 V	—	10.6	—	nC
Gate-Source charge		Q_{gs}		—	7.4	—	
Gate-Drain charge		Q_{gd}		—	3.3	—	
Drain-Source forward voltage		V_{DSF}	I_D = 1.8 A, V_{GS} = 0 (Note 3)	—	0.8	1.2	V

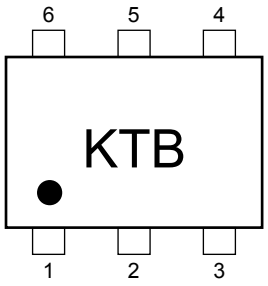
Note 3: Pulse test

Q2 Electrical Characteristics (Ta = 25°C)

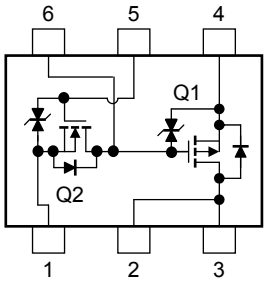
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 0.1 mA, V_{GS} = 0	20	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0	—	—	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.6	—	1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 10 m A (Note 3)	40	—	—	mS
Drain-Source on-resistance		$R_{DS\ (ON)}$	I_D = 10 mA, V_{GS} = 4 V (Note 3)	—	1.5	3.0	Ω
			I_D = 10 mA, V_{GS} = 2.5 V (Note 3)	—	2.2	4.0	
			I_D = 1 mA, V_{GS} = 1.5 V (Note 3)	—	5.2	15	
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0 f = 1 MHz	—	9.3	—	pF
Output capacitance		C_{oss}		—	9.8	—	
Reverse transfer capacitance		C_{rss}		—	4.5	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 3 V, I_D = 10 mA V_{GS} = 0 to 2.5 V, R_G = 50 Ω	—	70	—	ns
	Turn-off time	t_{off}		—	125	—	

Note 3: Pulse test

Marking



Equivalent Circuit (top view)



Precaution

V_{th} can be expressed as the voltage between the gate and source when the low operating current value is I_D = -1mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

Be sure to take this into consideration when using the device.

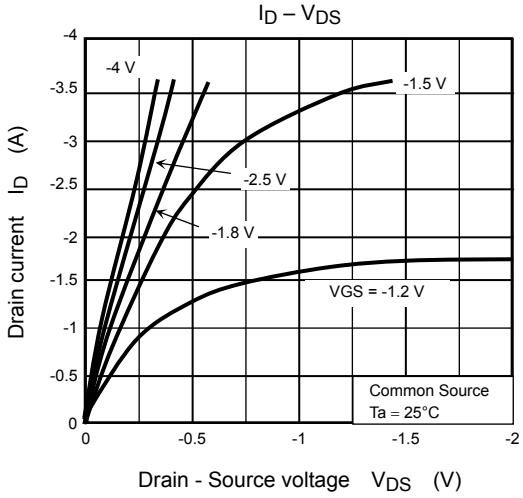
Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

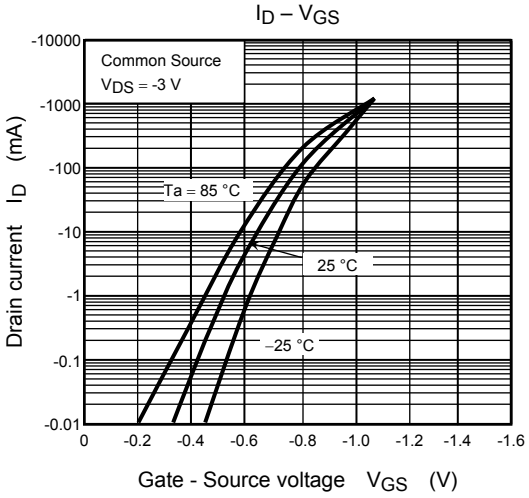
Thermal resistance $R_{th\ (j\text{-}a)}$ and drain power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

Q1 (Pch MOSFET)

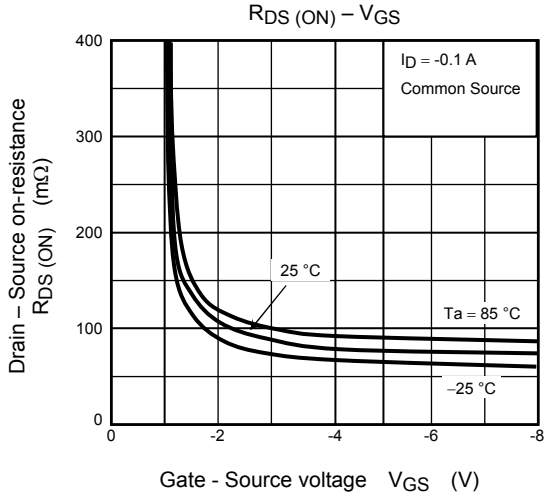
$I_D - V_{DS}$



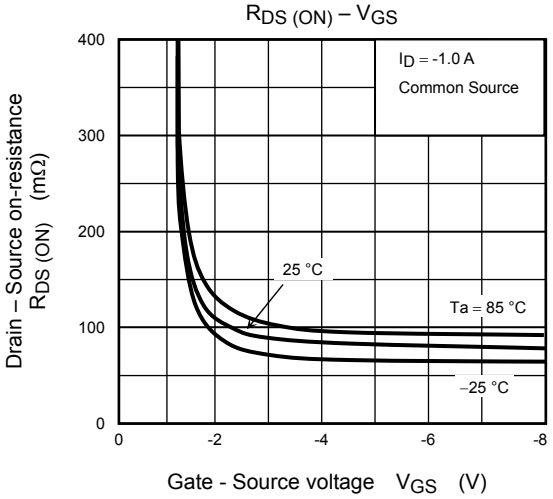
$I_D - V_{GS}$



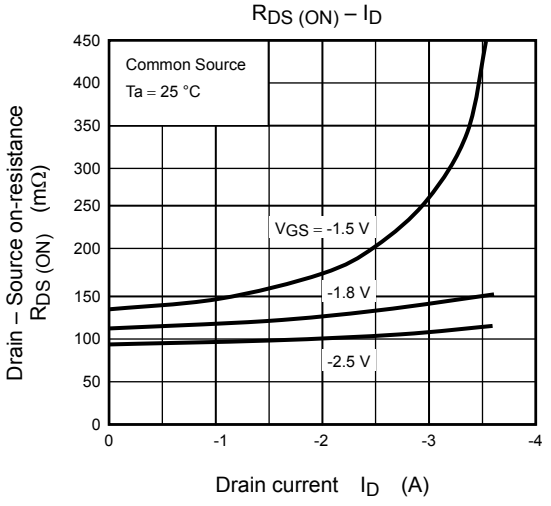
$R_{DS\ (ON)} - V_{GS}$



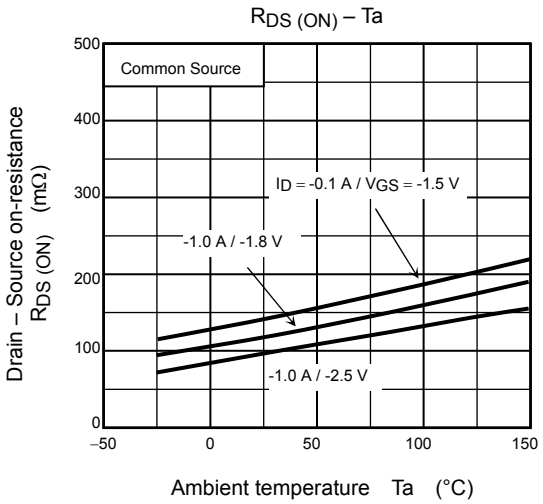
$R_{DS\ (ON)} - V_{GS}$



$R_{DS\ (ON)} - I_D$

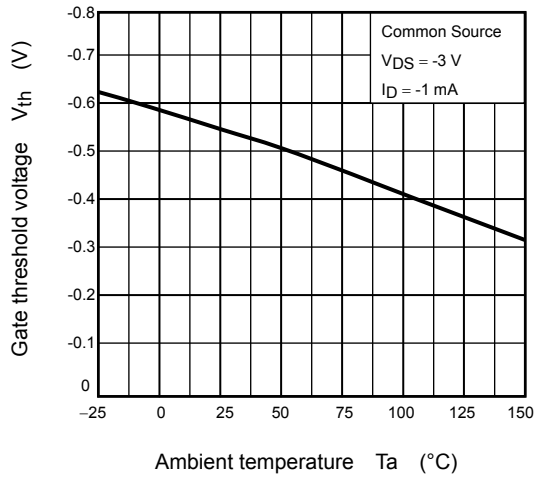


$R_{DS\ (ON)} - Ta$

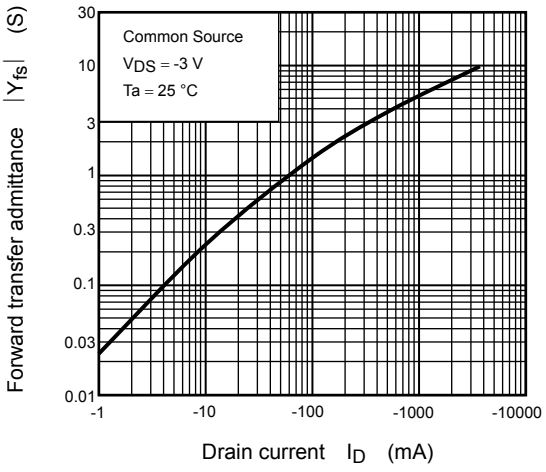


Q1 (Pch MOSFET)

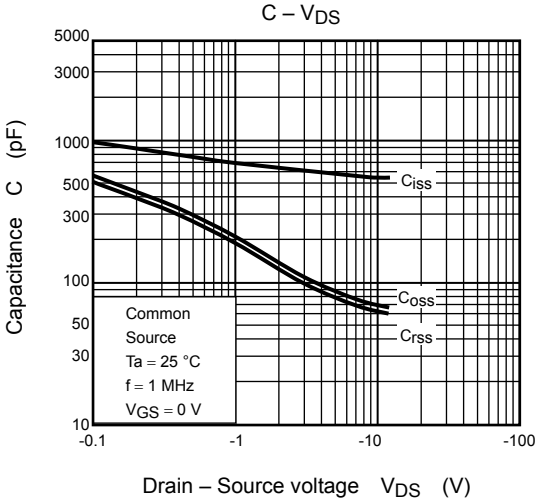
V_{th} – Ta



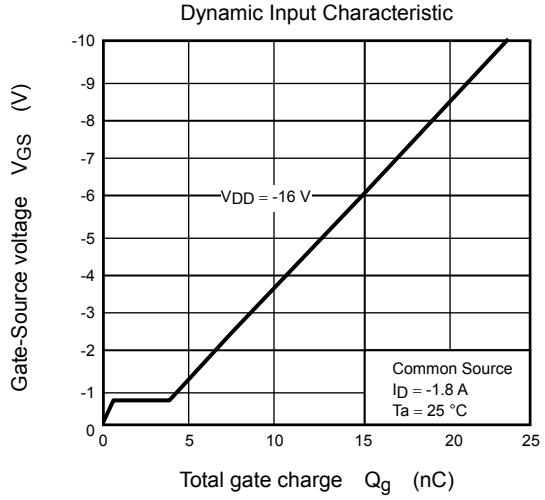
$|Y_{fs}|$ – I_D



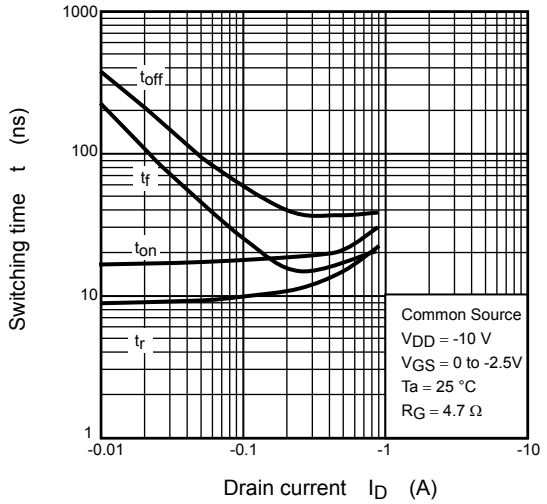
C – V_{DS}



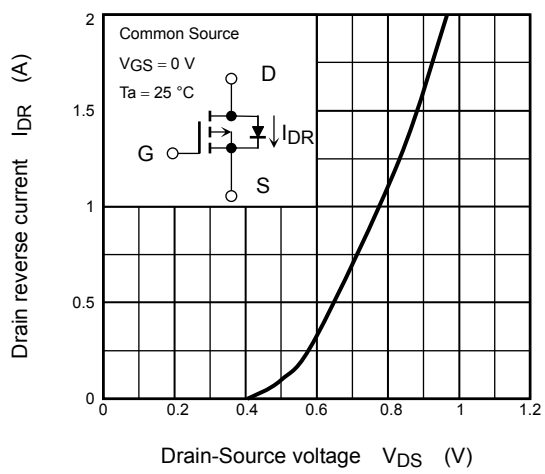
Dynamic Input Characteristic



t – I_D

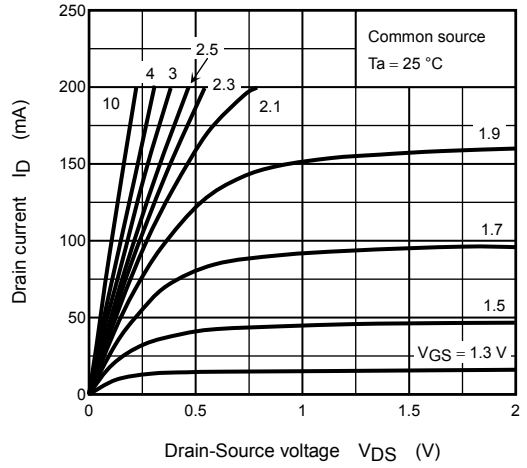


I_{DR} – V_{DS}

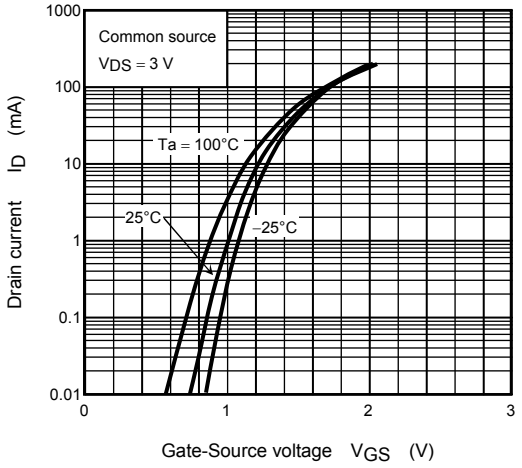


Q2 (Nch MOSFET)

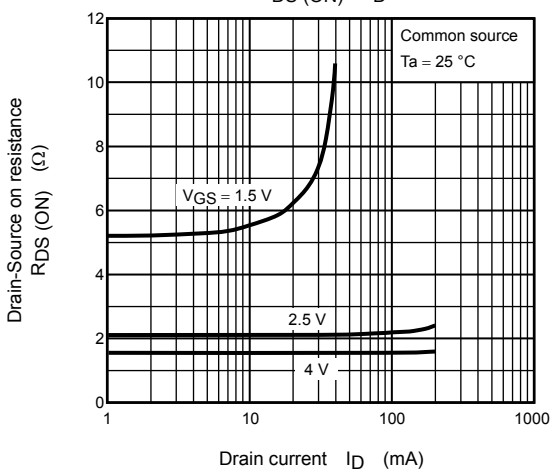
$I_D - V_{DS}$



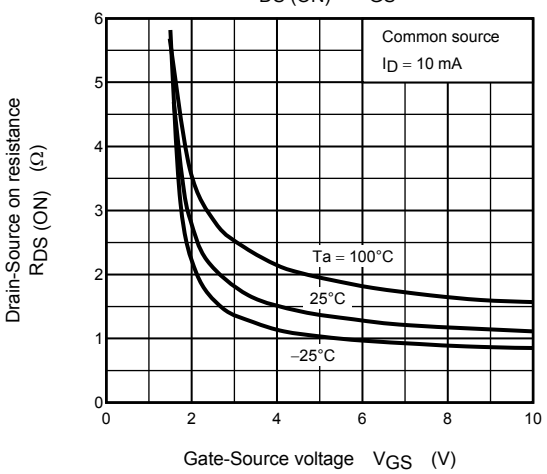
$I_D - V_{GS}$



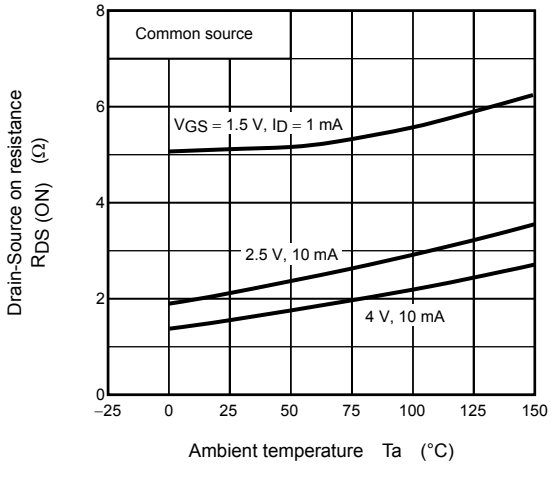
$R_{DS\ (ON)} - I_D$



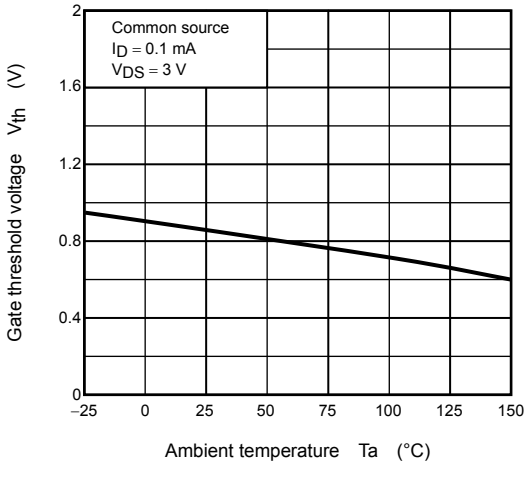
$R_{DS\ (ON)} - V_{GS}$



$R_{DS\ (ON)} - Ta$

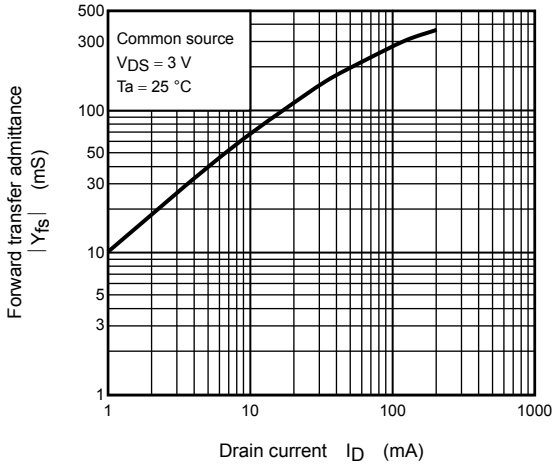


$V_{th} - Ta$

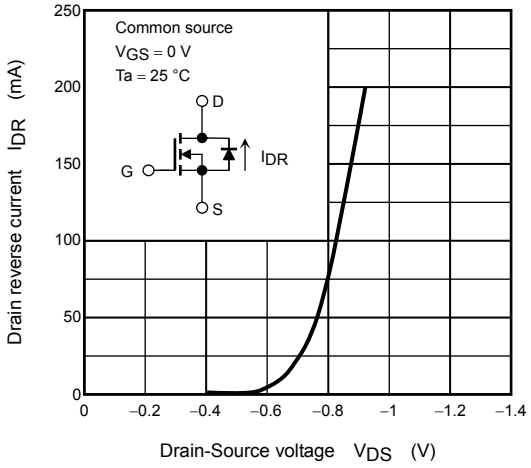


Q2 (Nch MOSFET)

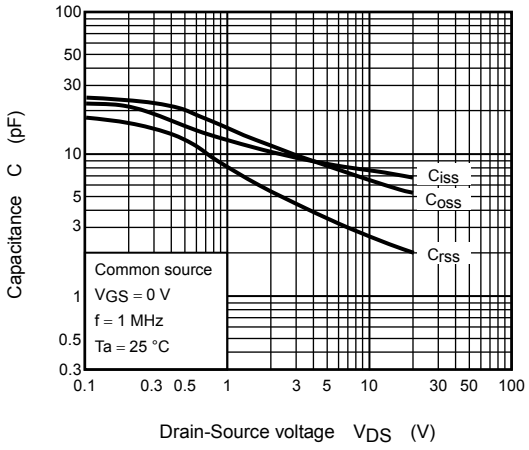
$|Y_{fs}| - I_D$



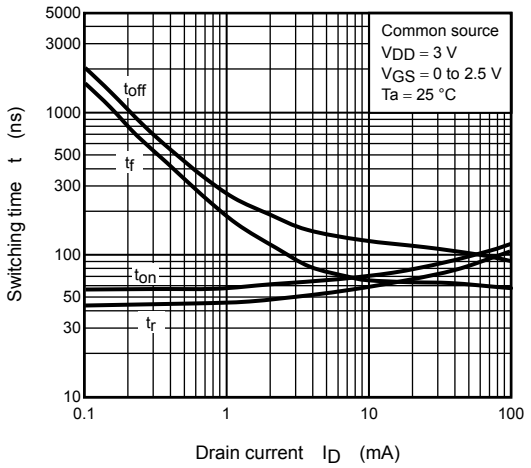
$I_{DR} - V_{DS}$



$C - V_{DS}$



$t - I_D$



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