AN4205
Application note

AC/DC converter to drive LEDs with mixed linear and switching regulation

By Vittorio Giuffrida

Introduction

The most recent developments in energy savings fit perfectly with LED lighting as LEDs have an almost unlimited operating life and a smaller size as well as better efficiency when compared to their incandescent counterparts. Nowadays these advantages make the use of LED lighting very attractive, but the higher cost is delaying widespread introduction in the lighting market.

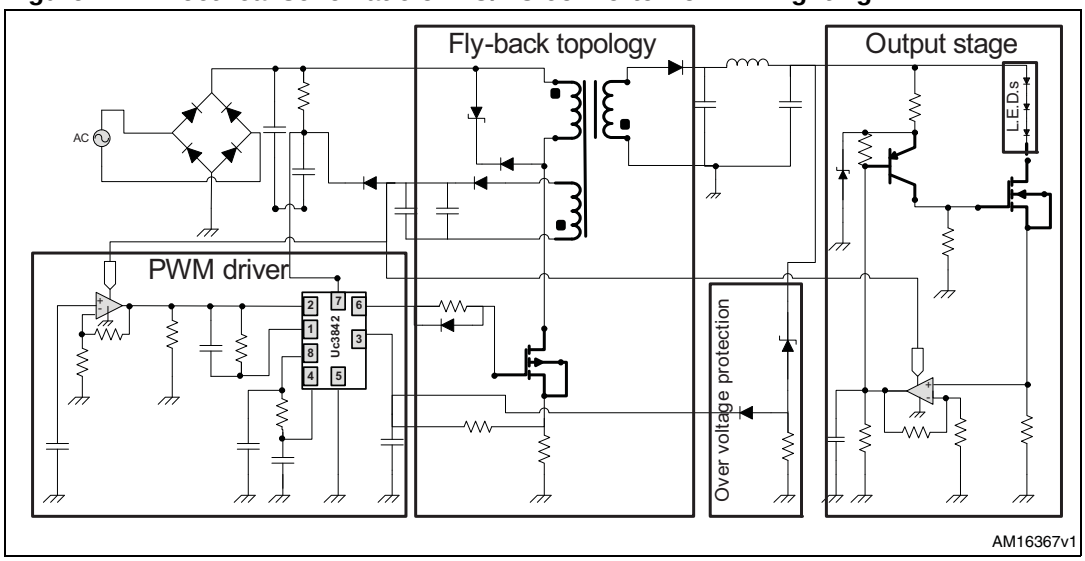
In this context an LED lighting driver has been designed in order to offer a cheap board in the consumer market. The AC/DC converter for LED lighting acts on linear regulation to control the LED current and on the switching regulation to minimize the power losses. In particular this application note presents the design guidelines of a 7 W LED driver. The solution lies in the output stage that implements a simple circuit able to keep the LED current constant and at same time to keep down the power losses in the Power MOSFET that works in the linear zone.

Contents

List of figures

1 System description

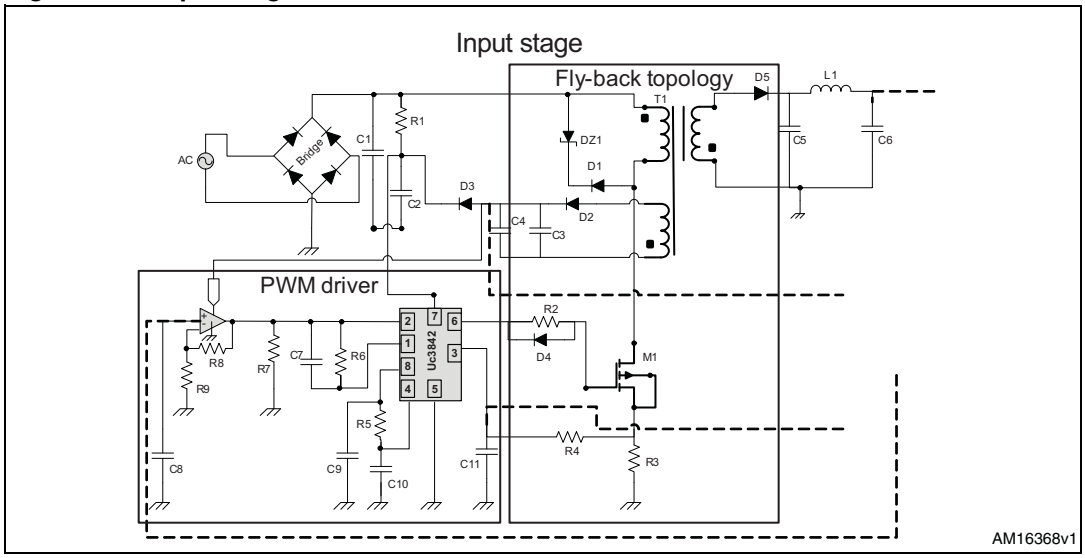
Figure 1. Electrical schematic of AC/DC converter for LED lighting



The AC/DC converter system is divided mainly into two sections, the input stage and the output stage. The input stage consists of a flyback topology able to transfer the energy to the secondary stage and to fix the output voltage. The output stage implements mixed linear regulation of the LED and switching current in order to decrease the power losses during linear current control.

2 Input stage of the AC/DC converter

Figure 2. Input stage of AC/DC converter



The input stage consists of a flyback topology where the main active elements are the standard STD3NK80Z Power MOSFET device and the reliable UC3842 PWM driver. As a power conversion topology, the flyback has been chosen because the control is easier, it's cheap and doesn't need an inductive input filter. In fact the main transformer works as an inductive filter itself. Therefore, the properties of the flyback meet the cost saving target of this project. Next, the specifications and the design of the input stage will be shown.

The first step is to define the specifications that the user must set for the AC/DC converter.

Table 1. Input stage specifications data

Name	Symbol	Value
Minimum DC input voltage	V_{DCmin}	250 V
Maximum DC input voltage	V_{DCmax}	370 V
DC output voltage	V_{Bus}	~19 V
Output power	P_{OUT}	~7 W
Electrical efficiency	η	80%
Switching frequency	f_s	100 kHz

The flyback operation, with reference to the basic circuit in *Figure 2*, is a two-step process. The first step is the on-time of the switch, where the energy is taken from the input and stored in the primary winding of the flyback transformer. At the secondary stage, the diode is reverse-biased and the load is supplied by the energy of the bulk capacitor. Then the switch turns off (off-time) and the energy stored in the primary is transferred to the transformer secondary. So through the diode, forward-biased, the stored energy is delivered to the out capacitor. The output voltage V_{out} is reflected back to the primary through the transformer

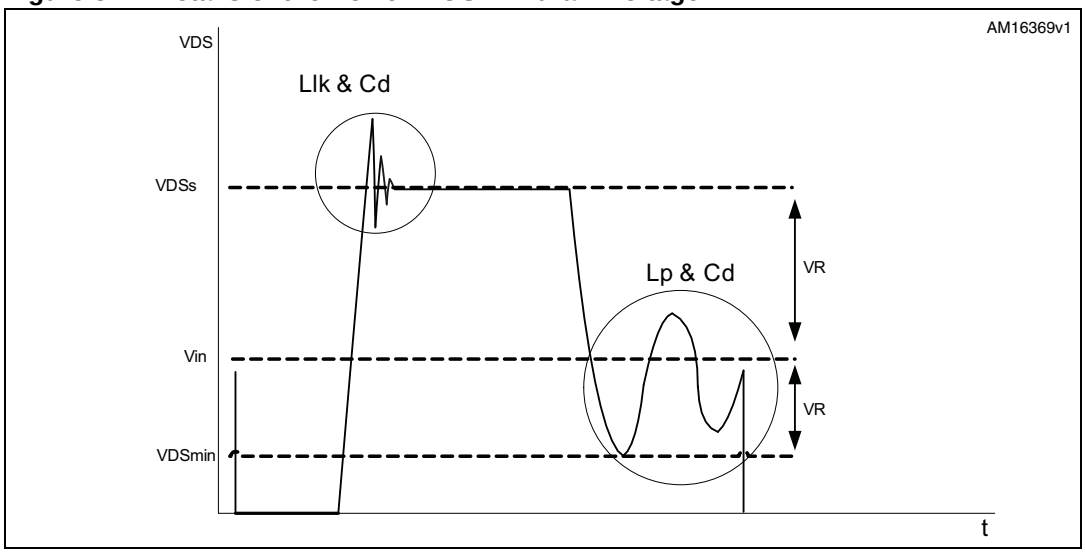
ratio and adds to the input voltage V_{IN}, giving a much higher voltage on the drain of the Power MOSFET.

Equation 1

$$V_{fl} = (V_{out} + V_{diode})\frac{N_p}{N_s}$$

Before starting the design of the converter, some parameters need to be set.

Figure 3. Details of the Power MOSFET drain voltage



The drain voltage of the Power MOSFET device is:

Equation 2

$$V_{DSS} = V_{IN} + V_{fl} + V_{spike} + V_{margin}$$

The V_{fl} reflected voltage depends on a proper N_P/N_S transformer ratio. In particular the maximum voltage rating of the Power MOSFET and the V_R reverse voltage across the output diode relates to this transformer ratio. A lower N_P/N_S requires a higher V_R on the diode, while V_{DS} of the Power MOSFET is decreased. However, a higher transformer ratio implies a higher voltage stress on the Power MOSFET, while V_R is decreased.

The V_{spike} leakage inductance overvoltage is due to energy stored in the mutual inductance of the transformer primary side which is not completely transferred to the secondary. When the leakage inductance is demagnetized, the energy can be transferred to the secondary. In order to minimize this delay, the voltage across the primary inductance should be as high as possible.

The V_{margin} should be 20% of the V_{DSS} of the Power MOSFET device.

In accordance with these explanations we have chosen:

V_{spike}=160 V

V_{margin}=160 V

Hence, a device with V_{DSS} = 800 V (STD3NK80Z) has been chosen. This selection will allow using a clamp circuit with a lower operation time and having a safety margin around the voltage rating on the drain pin.

Equation 3

$$V_{fl} = V_{DSS} - V_{DCmax} - V_{spike} - V_{margin} \cong 110V$$

Therefore, from *Equation 1* we can easily calculate the transformer ratio.

Equation 4

$$\frac{N_P}{N_S} = \frac{V_{DSS} - V_{DCmax} - V_{spike} - V_{margin}}{V_{out} - V_{F,diode}} = \frac{800 - 370 - 160 - 160}{19 + 1} = 5.5$$

The other step is to ensure that the energy on the primary coil will be completely transferred to the secondary before the next cycle occurs.

$$T_{on} + T_{reset} < T_s$$

T_{ON} is the time during which the Power MOSFET operates, T_{reset} is the time to demagnetize the transformer inductance (Power MOSFET is off) and T_s is the switching time. The next formula gives a safe margin in order to demagnetize the primary side.

Equation 5

$$T_{on} + T_{reset} = 0.8T_s$$

Combining *Equation 2* and *Equation 3* results in:

Equation 6

$$T_{ONmax} = \frac{V_{fl} 0.8T_s}{V_{DCmin} + V_{fl}} = 2.4\mu s$$

The next step is to calculate the current peak. The output power is set to 7 W and the efficiency to 80% and using an approximate formula, we have:

Equation 7

$$P_{IN} = \frac{P_{OUT}}{0.8} = \frac{L_P I_P^2}{2T_s} = \frac{V_{DCmin}^2 T_{ONmax}^2}{2L_P T_s}$$

therefore:

Equation 8

$$L_P = \frac{V_{DCmin}^2 T_{ONmax}^2}{2.5T_s P_{out}} \cong 2mH$$

Now we can calculate the peak current on the primary and on the secondary:

Equation 9

$$I_{P,peak} = \frac{V_{DCmin} T_{ONmax}}{L_P} = 300mA$$

Equation 10

$$I_{S,peak} = I_P \frac{N_P}{N_S} = 1.65A$$

Then the value of the I_{RMS} current must be determined:

Equation 11

$$I_{Prms} = \frac{I_P}{\sqrt{3}}\sqrt{\frac{T_{ONmax}}{T_s}} \cong 85mA$$

Equation 12

$$I_{Srms} = \frac{I_{S,peak}}{\sqrt{3}}\sqrt{\frac{T_{reset}}{T_s}} \cong 713mA$$

2.1 Flyback transformer design

The transformer design mainly consists of fixing the magnetic core, its geometry and the exact number of primary turns. The standard soft ferrite with gapped core and E-type geometry is a common choice for flyback topology because it is low cost and suitable for low/medium power applications. For this project E16/8/5 N87 material has been chosen.

First the power losses of the ferrite with regard to the maximum magnetic flux ΔBmax must be determined. From the datasheet of the N87 material, the dynamic magnetization curve shows that ΔBmax = 380 mT (@ T=100 °C) but we impose a ΔBmax = 200 mT to have a safety margin. So, knowing the switching frequency (f_S=100 kHz) and the magnetic flux, we can determine the relative core losses (referring to the datasheet of N87, see the figure "relative core losses versus frequency"):

$$P_v = 400mW/cm^3$$

Therefore the power losses of the ferrite are:

Equation 13

$$P_{fe} = P_v V_e$$

where V_e=0.75 cm^3 is the total volume of the core.

$$P_{fe} = P_v V_e = 0.75 \bullet 400 = 300mW$$

Knowing that the thermal resistance R_{th} of the selected core is 65 °C/W, we have:

Equation 14

$$P_{fe} = \frac{\Delta T}{R_{th}} \rightarrow \Delta T = 19.5°C$$

This result provides the thermal condition regarding the hypothesis of ΔBmax. Next we have to add the power losses due to the winding.

Now the number of primary turns must be calculated.

Equation 15

where A_{min} = 19.4 mm² is the minimum area of ferrite.

$$N_P = \frac{V_{DCmin} T_{ONmax}}{\Delta B_{max} A_{min}}$$

From *Equation 4*, we can determine the number of secondary turns:

$$N_P \approx 155$$

$$N_{PS} \approx 28(155)$$

We can also calculate the auxiliary needed to supply the driver. The driver used is the UC3842 which is driven by 15 V.

Equation 16

$$\frac{N_P}{N_{Aux}} = \frac{V_{fl}}{V_{Aux} + V_{F,diode}} = \frac{100}{15+1} = 6.25 \rightarrow N_{Aux} = 25$$

The next step is to determine the air gap length (l_g) of the core and the inductance of a single turn (A_L).

Knowing the primary inductance, the inductance of a single turn can be calculated:

Equation 17

$$L_P = N_P^2 A_L \rightarrow A_L = \frac{L_P}{N_P^2} = 85nH$$

In this case we chose the standard value A_L=100 nH.

Now the air gap length is known:

Equation 18

$$l_g = \left(\frac{A_L}{K_1}\right)^{1/K_2}$$

From the datasheet of the core K1 = 42.2 and K2 = -0.701

$$l_g = 0.3mm$$

Before proceeding to calculate the wire dimension, we can verify if the selected core is acceptable (safety condition) with regard to thermal operation.

Using Ampere's law we can calculate the B field:

Equation 19

$$N_P I_P = \oint H dl = \Sigma H_i l_i = H_g l_g + H_{fe} l_{fe} = \frac{B}{\mu_0} l_g + \frac{B}{\mu_{fe}} l_{fe}$$

The magnetic permeability μ_{fe} is much higher than μ_0 (the magnetic permeability in the air), so we can neglect the last term in *Equation 19*.

Equation 20

$$N_P I_P = \frac{B}{\mu_0} l_g \rightarrow B = 194mT$$

This result confirms the accuracy of the hypothesis about ΔBmax.

In order to calculate the wire dimension, we have to impose the maximum losses on the copper. In this case we choose a dissipation level similar to the one of the core (P_{fe}) plus a safety margin, for practical purposes we have chosen 0.5 W. Now we assume that the primary and secondary winding losses are half of the selected total power:

$P_{CUprimary}$ = 0.25 W, $P_{CUsecondary}$ = 0.25 W

From Joule's law, we have:

Equation 21

$$P_{CUprimary} = R_P I_{P,rms}^2 \rightarrow R_P \cong 35\Omega$$

Equation 22

$$P_{CUsecondary} = R_S I_{P,rms}^2 \rightarrow R_S \cong 0.5\Omega$$

Knowing the copper resistivity at 100 °C (ρ100=2.303*10-6 Ωcm) and the average winding length (L_t=3.4 cm, from the datasheet of the core), we have:

Equation 23

$$A_{PCU} = \frac{\rho_{100} N_P L_t}{R_P} = 3.46 \bullet 10^{-05} cm^2$$

Equation 24

$$A_{SCU} = \frac{\rho_{100} N_S L_t}{R_S} = 4.5 \bullet 10^{-04} cm^2$$

Therefore, the diameter of the wire is:

Equation 25

$$d_P = 6.6 \bullet 10^{-03} cm$$

Equation 26

$$d_S = 23.4 \bullet 10^{-03} cm$$

In accordance with the above specifications, the final transformer has been provided by MAGNETICA. The following table summarizes the most important parameters of this transformer.

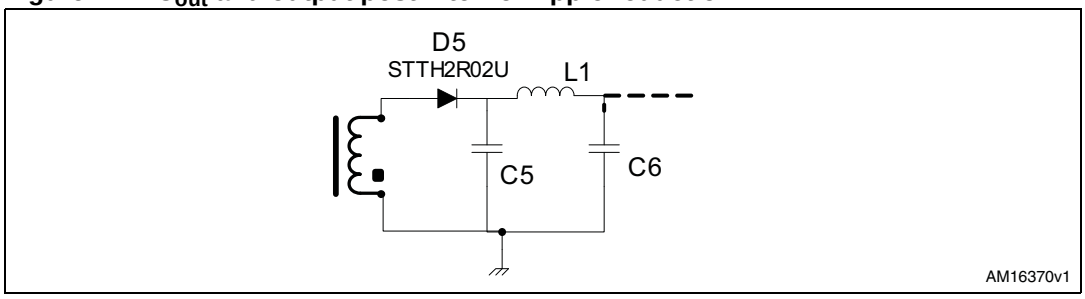
Table 2. Key transformer characteristics

Name	Symbol	Value
Inductance	$L_{primary}$	2.18 mH ± 15%
	$L_{secondary}$	93 µH ± 15%
	$L_{auxiliary}$	35 µH ± 15%
Transformer ratio	N_P/N_S	4.85
Leakage inductance	$L_{leakage}$	3.5% nom
Parasitic capacitance	$C_{parasitic}$	38 pF
Saturation current	I_{sat}	0.45 A max
Switching frequency	f_s	100 kHz

2.2 Output capacitor selection and post filter

The AC current in the output capacitor causes power dissipation on its series resistance (ESR), resulting in a rise in temperature. Thus, it is important to not operate the output capacitor beyond its AC current ripple rating, otherwise its lifetime will be very short. In general, a low ESR capacitor is a good choice as it provides excellent energy storage and improves the transient performance. For this project the requirement on ESR is very tight, so we have used a C_{out} output capacitor and an L_C post filter, like the one shown in *Figure 4* that attenuates the ripple to the desired level.

Figure 4. C_{out} and output post filter for ripple reduction



In this case we have chosen a capacitor supplier with:

Equation 27

$$ESR \bullet C = 32 \bullet 10^{-06} s$$

Since we want V_{ripple}~0.4 V (2% of V_{out}=20 V), hence:

Equation 28

$$ESR_{ripple} = \frac{V_{ripple}}{I_{S,peak}} = 0.24\Omega$$

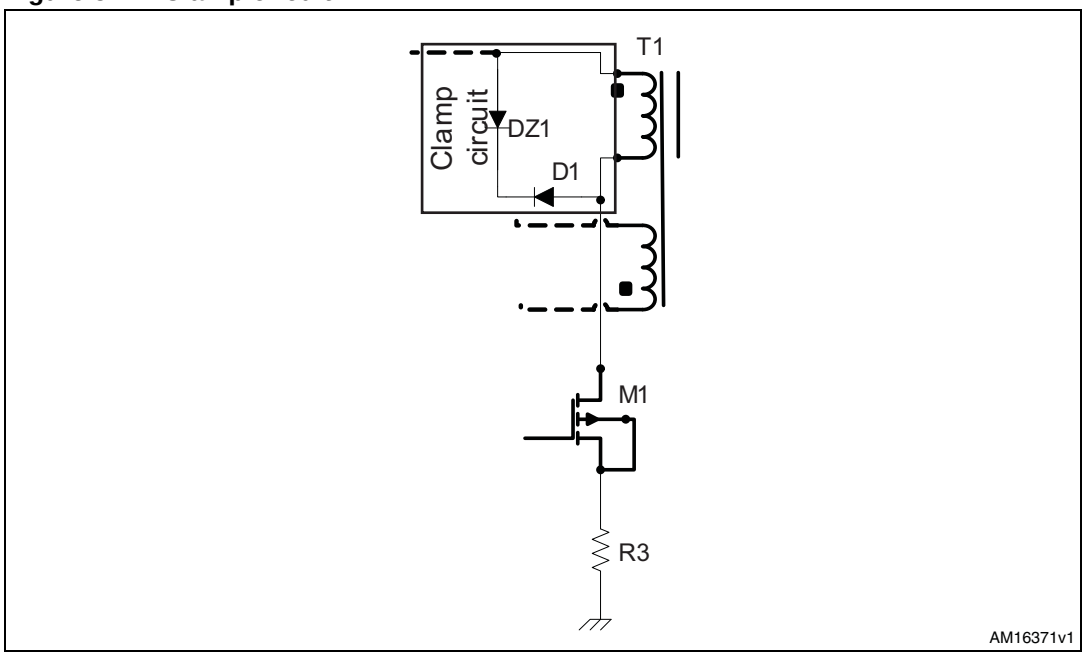
Therefore,

$$C_{out} \geq \frac{32 \bullet 10^{-06}}{ESR} = 135\mu F$$

The choice of the correct size of the post filter has been an iterative process that has required some trials before finding the optimal level of the desired ripple.

2.3 Clamp circuit

Figure 5. Clamp circuit



The drain pin of the Power MOSFET device (STD3NK80Z) has to be properly clamped to prevent a spike due to the transformer leakage inductance from exceeding the breakdown voltage. An RCD clamp is a cheap solution but it dissipates power. Therefore we have preferred to use a Zener or Transil™ clamp which is recommended to minimize the power losses during the Power MOSFET commutation.

Imposing a safety margin of 15%, we have:

Equation 29

$$V_{ZENER} + V_{DCmax} = V_{DSS} - 15\% V_{DSS}$$

Hence:

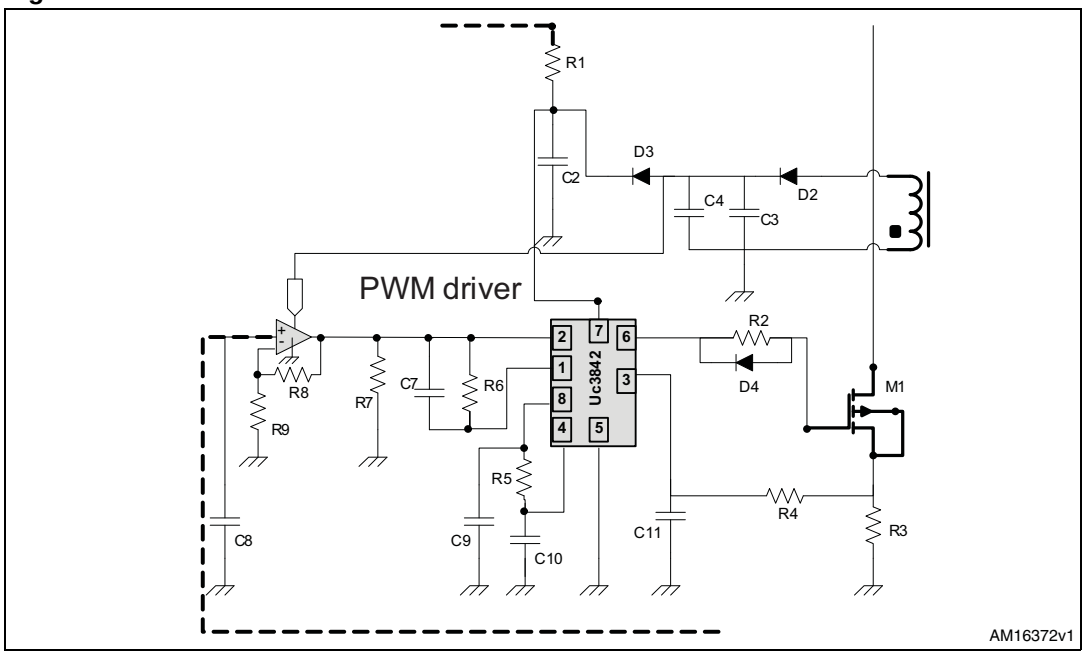
$$V_{ZENER} \cong 300V$$

In accordance with this specification the Transil™ is STP6KE300A.

2.4 UC3842 driver

A simple PWM driver has been chosen to drive the gate of the STD3NK80Z device and direct the flyback topology requested by the converter. The driver is the common UC3842 and it provides all the essential features necessary to the operation of the basic current mode controller. The UC3842 needs 15 V for its correct biasing and this voltage reference is supplied by the auxiliary output of the transformer.

Figure 6. UC3842 PWM driver and network



The next step is to design the network for the PWM driver pins.

The first step is to determine the required circuit dead time in order to select the oscillator components. Once obtained, *Figure 7* is used to pinpoint the nearest standard value of C9. Next, the appropriate R5 value is interpolated using the parameters for C9 and oscillator frequency. *Figure 8* illustrates the R5/C9 combinations versus oscillator frequency.

Figure 7. Dead time vs. C9 (R5>5k)

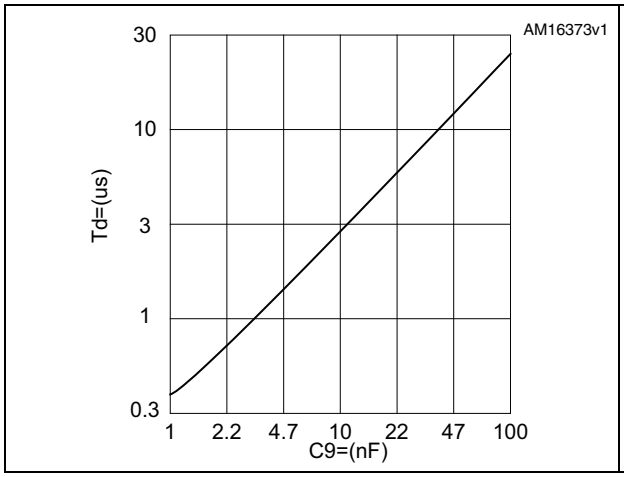
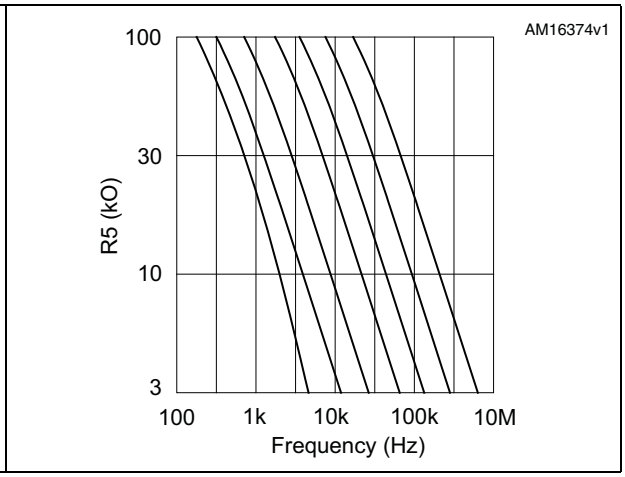


Figure 8. Time resistance vs. frequency



The timing resistor can be calculated from the following formula:

Equation 30

$$f_{osc}(kHz) = \frac{1.72}{R5(k) \bullet C9(\mu F)}$$

The UC3842 current sensing input is done externally with ground-referenced resistor R3. Under normal operation the peak voltage across R3 is controlled by the error amplifier according to the following formula:

Equation 31

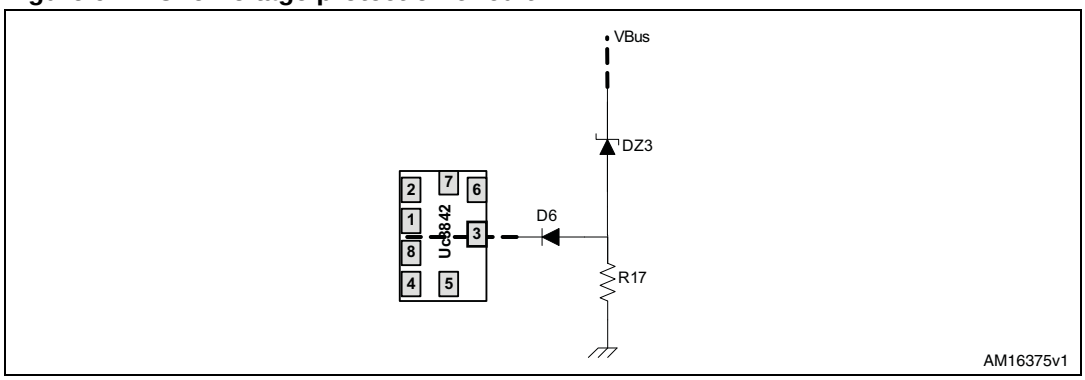
$$I_{P,peak} = \frac{V_C - 1.4V}{3R_S}$$

where V_C = E/A output voltage.

The next step is the error amplifier (E/A) configuration. The R6, R7 and C7 error amplifier compensation circuit is chosen in order to ensure converter stability while providing good dynamic response.

2.5 Overvoltage protection circuit

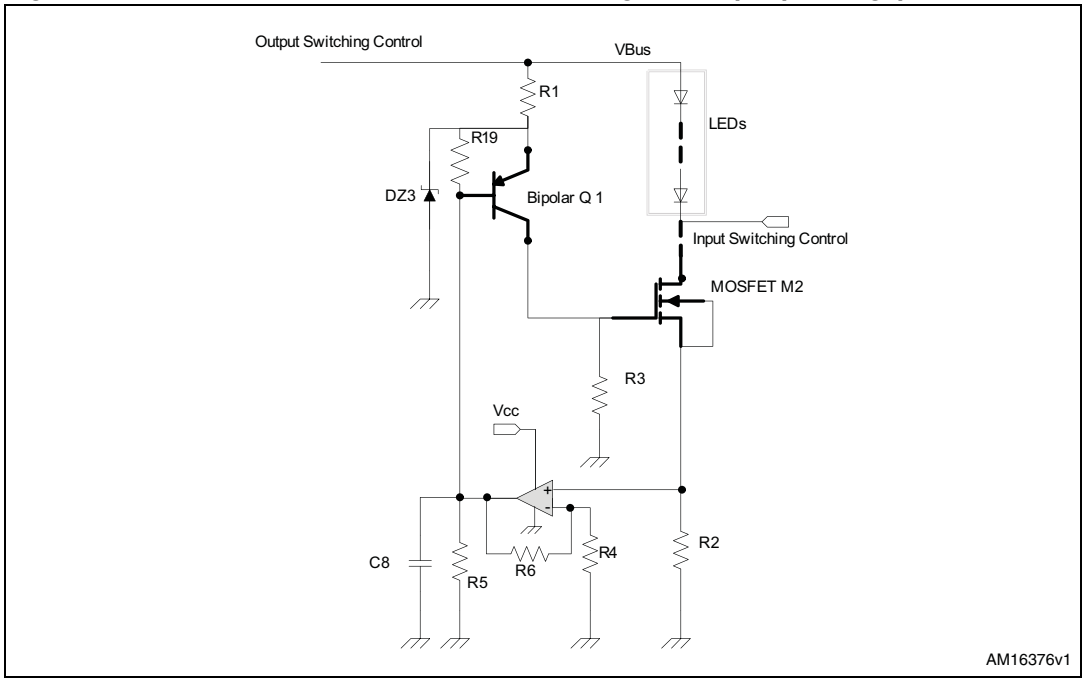
Figure 9. Overvoltage protection circuit



The overvoltage protection circuit is required in order to not damage the LED lamps. It is connected between the output and ground. The Zener diode voltage has been chosen to be slightly above that of the output voltage. When the Zener diode voltage is reached, current flows into the resistor and as soon as the voltage, through the diode, exceeds one of the internal silicon diodes (1 V) of the UC3842 driver, the PWM is stopped. In this way the voltage across the output capacitor decreases. When the input of the error amplifier of UC3842 is lower than 2.5 V (internal reference voltage), the PWM restarts. So this overvoltage protection circuit temporarily stops the PWM driver, but it ensures system operation as soon as the condition of the error amplifier is reached.

3 Output stage description

Figure 10. Electrical schematic of the double regulation (output stage)



The solution, shown in *Figure 10*, performs the linear regulation of the current of the LEDs and the switching regulation which adjusts the V_{DS} voltage of the Power MOSFET (M2) device in order to decrease the power losses during the linear regulation. This last result is the main feature of this solution because it compensates for the cost of efficiency due to standard linear regulation. The voltage control depends on the switching regulation that first reads the V_{DS} voltage of Power MOSFET in series to the LED components and then controls the out voltage (V_{Bus}) in order to minimize V_{DS}. This feature allows power losses lower than those of typical linear regulation and very low voltage ripple across LED components. The linear regulation of the current consists of a bipolar device which, connected to the Power MOSFET gate, controls the V_{GS} voltage so that this Power MOSFET operates in the linear region. So the I_{DS} current and the current of the LEDs are regulated very well.

4 Output stage setting

The goals of this output stage of the LED driver are the constant current on the LED components and low power losses during the linear regulation. Next, the setting and the project of the output stage will be shown.

The first step is to define the output stage specifications that the user must set for the innovative LED driver.

Table 3. Output stage specifications data

Name	Symbol	Value
Light emitter diode	LED	6 LEDs of ~ 3.2 V & 1.2 W
DC output current	I_{OUT} (I_{DS})	~ 350 mA
DC output voltage	V_{BUS}	~ 19 V
MOSFET drain-source voltage	V_{DS}	~ 300 mV
Output voltage	P_{OUT}	~ 7 W

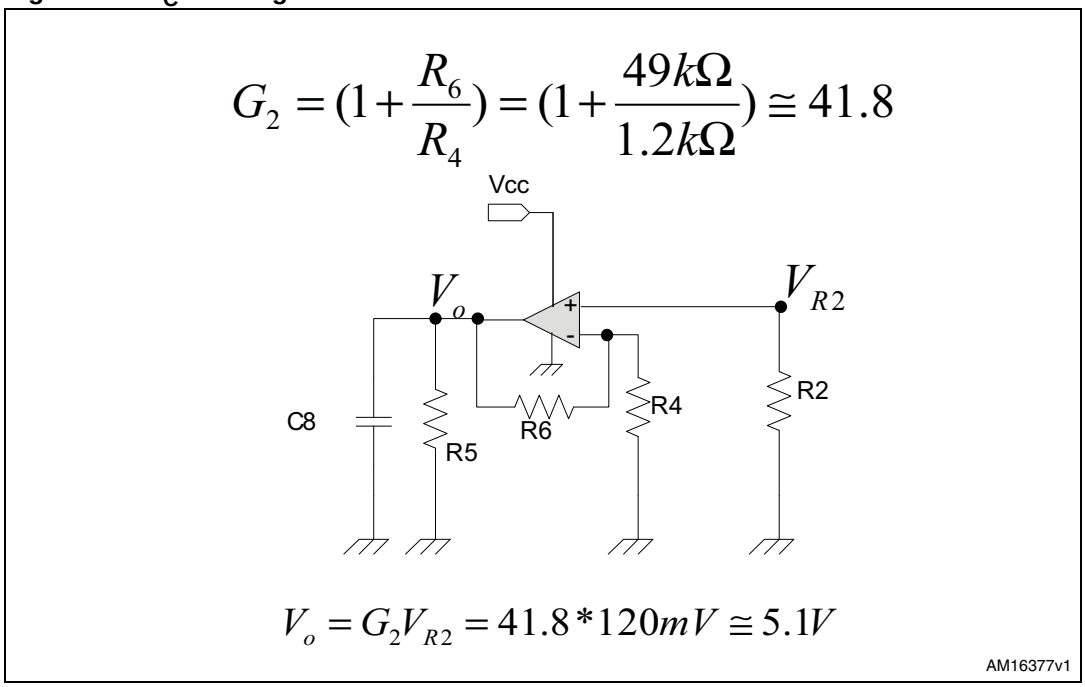
The bipolar device (Q1), connected to the Power MOSFET gate (*Figure 10*), controls the V_{GS} voltage and consequently the I_{DS} current using the following formula:

Equation 32

$$I_{DS} = K \bullet (V_{GS} - V_{th})^2 \bullet (1 + \lambda V_{DS})$$

In order to perform the linear regulation, the bipolar Q1 operates in forward active mode (common emitter), therefore for small base current variations, the emitter-collector voltage changes depending on the H_{fe} parameter of the transistor. The collector variations cause a negative feedback. If the base voltage of the bipolar implies a rise in the collector voltage, the gate of the Power MOSFET decreases because the emitter node is fixed by the Zener device, vice versa if the collector voltage decreases. The base current variations depend on the I_{OUT} (I_{DS}) current through the voltage, across the R2 sensing resistor, which is boosted by the I_C1 amplifier. The I_C1 setting guarantees the forward active mode operation of the bipolar.

Figure 11. I_C1 setting



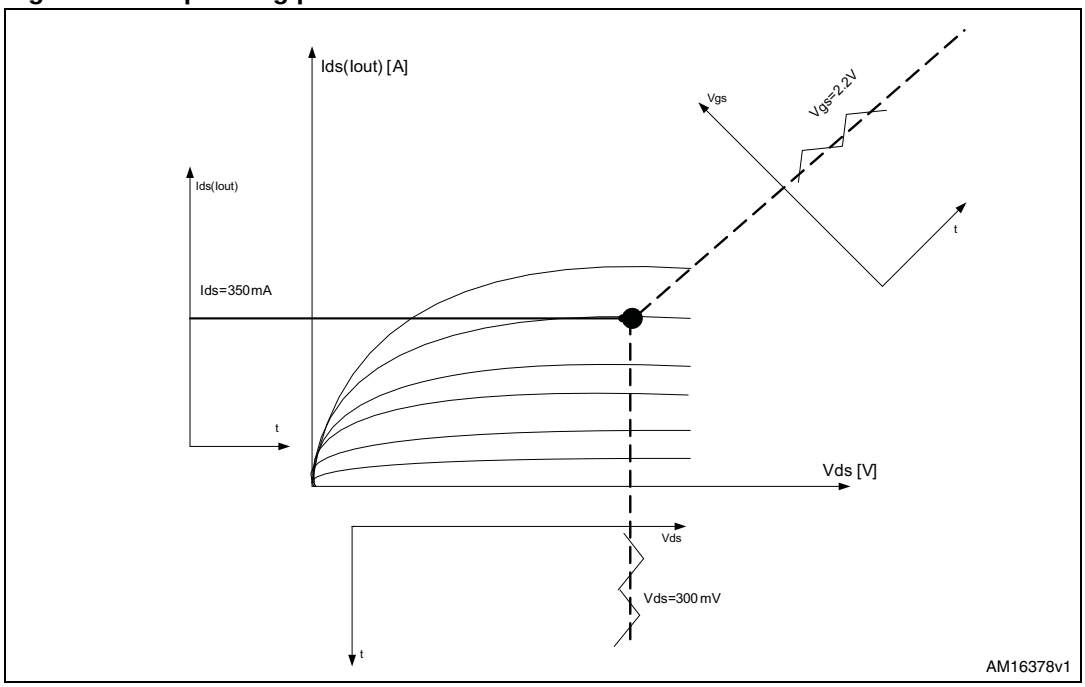
The bipolar Q1, operating in forward active mode, guarantees the linear region for the Power MOSFET device and so the linear regulation of the I_{DS} (I_{out}) current can occur thanks to *Equation 1*. The Q1 transistor is basically a common-emitter amplifier where the base terminal serves as the input and the collector terminal as the output. The voltage gain depends on the R1/R3 resistors and on the transconductance g_m.

$$\frac{V_{ec}}{V_{eb}} = |g_m| R_{eq}$$

The R1 resistor in *Figure 10* and the Vz voltage of DZ3 Zener fix the collector variations in function of the V_{eb} voltage and consequently determine the peak-to-peak amplitude of the regulation signal. On the other hand, the R3 and R19 resistors in *Figure 10* set the feedback time of the bipolar Q1 and Power MOSFET M2.

To summarize, *Figure 12* clarifies the linear current regulation of this simple and innovative solution.

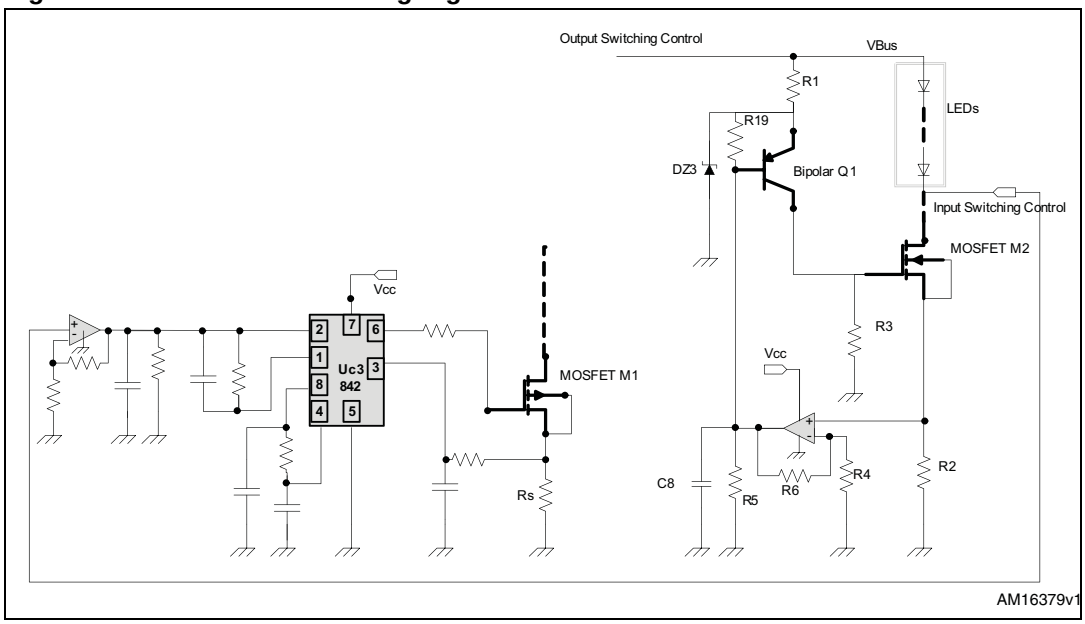
Figure 12. Operating point of the Power MOSFET



4.1 Switching regulation

The switching regulation adjusts the V_{DS} voltage of the Power MOSFET (M2) device in order to decrease the power losses during the linear regulation. In particular this type of regulation first reads the V_{DS} voltage of the Power MOSFET in series to the LED components and then controls the out voltage (V_{Bus}) in order to fix V_{DS} in order to minimize the power losses in the power transistor. When the V_{DS} voltage reaches the maximum threshold (fixed by the specification), the I_{DS} (I_{OUT}) current has already reached the 350 mA value, thus triggering the switching regulation.

Figure 13. Details of switching regulation



The V_{DS} signal is processed by an operational amplifier (A.O.) and is then sent to the “non-inverting input” of the “UC3842” driver, which decides the state of the Power MOSFET M1 put in a flyback topology *Figure 13*. If the V_{DS} value is greater than the threshold (fixed by specification), the "UC3842" driver stops the PWM regulation and the output voltage decreases, vice versa the PWM regulation starts again.

The main advantages for processing the V_{DS} signal rather than the V_{BUS} as in other standard linear regulation systems, are listed as follows:

1. To keep the ripple output voltage low
2. To fix the average value of the V_{DS} voltage in order to minimize the power losses of the power transistor
3. To guarantee the V_{DS} value lower than the threshold even if one or more LED components are short

5 Test results

To verify the validity of this innovative solution, a prototype of an AC/DC converter driver of LEDs has been built and tested. The following test results show the main advantages of the linear current regulation and the switching regulation.

Figure 14. Main waveforms of the linear current regulation

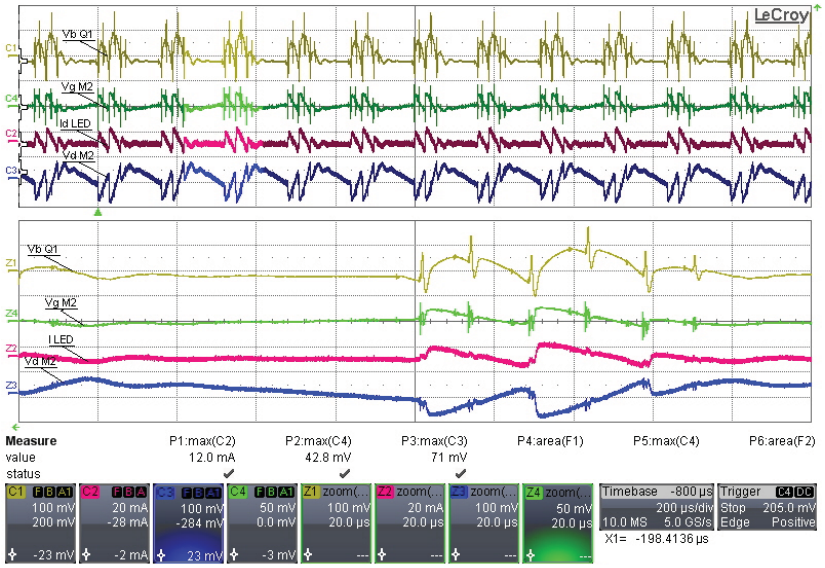
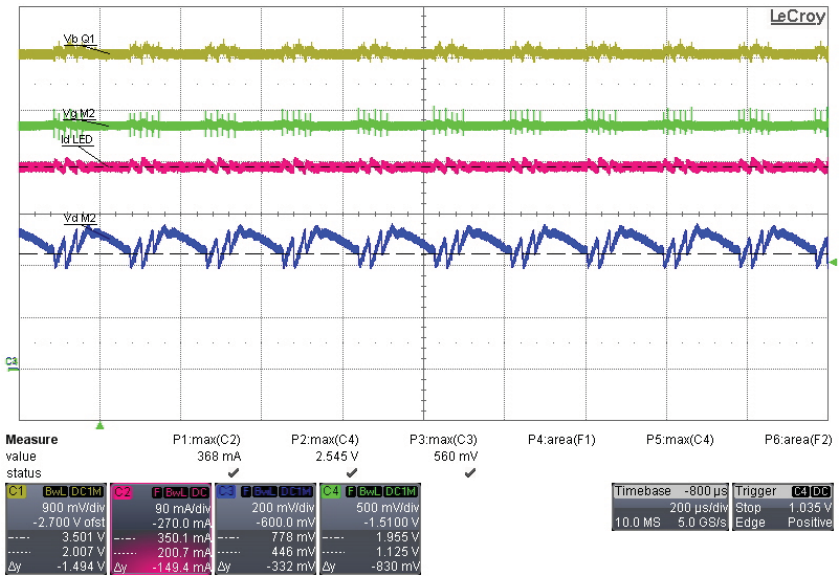


Figure 15. Main signals of the output stage



- *Figure 14* shows the details of the linear current regulation. When the value of V_B (base voltage of bipolar Q1) rises, V_{GS} of the Power MOSFET M2 decreases and the I_{DS} (I_{OUT}) current decreases. That allows fixing the current variations to approximately 350 mA.
- *Figure 15* shows the features of the output stage main signals. The I_{OUT} ripple current (red waveform) is very low and the V_{DS} average value is around the voltage threshold fixed by specification:

$$V_{DS(average)} = V_{Dground} - VR2 \sim 300mV$$

Targeting higher energy conservation, the main features of the LED driver result in an almost constant I_{DS} (I_{OUT}) current, ensuring a very long lifetime for the LED components and a regulated V_{DS} signal in order to minimize the power losses during linear regulation which is the most important feature of the LED driver because it compensates for the cost of efficiency of the standard.

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
19-Apr-2013	1	Initial release.

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