

RJE0615JSP

-60 V, -10A Silicon P Channel Thermal FET
Power Switching

R07DS0124EJ0300
Rev.3.00
Oct 27, 2014

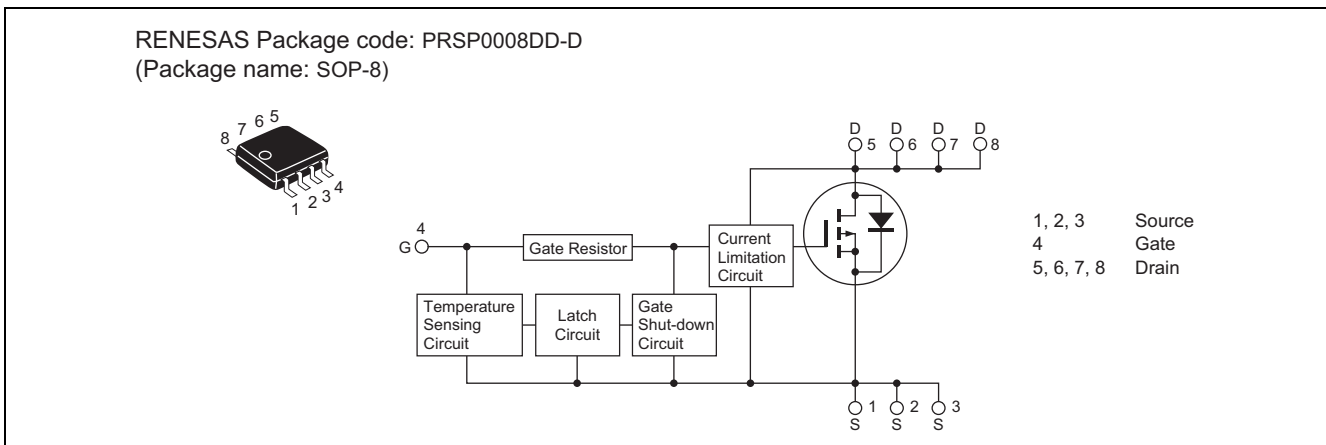
Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- Low on-resistance $R_{DS(on)}$: 53 mΩ Typ, 65 mΩ Max ($V_{GS} = -10$ V)
- High density mounting

Outline



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	-16	V
	V_{GSS}	2.5	V
Drain current	I_D ^{Note 3}	-10	A
Body-drain diode reverse drain current	I_{DR}	-10	A
Avalanche current	I_{AP} ^{Note 2}	-4.7	A
Avalanche energy	E_{AR} ^{Note 2}	94.7	mJ
Channel dissipation	P_{ch} ^{Note 1}	2.5	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1 1 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), $PW \leq 10$ s

2. $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

3. It provides by the current limitation lower bound value.

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	-3.5	—	—	V	
	V _{IL}	—	—	-1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	-100	μA	V _i = -8 V, V _{DS} = 0
	I _{IH2}	—	—	-50	μA	V _i = -3.5 V, V _{DS} = 0
	I _{IL}	—	—	-10	μA	V _i = -1.2 V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sd)1}	—	-0.8	—	mA	V _i = -8 V, V _{DS} = 0
	I _{IH(sd)2}	—	-0.35	—	mA	V _i = -3.5 V, V _{DS} = 0
Shut down temperature	T _{sd}	—	175	—	°C	Channel temperature (dv/dt V _{GS} ≥ 500 V/ms)
Gate operation voltage	V _{op}	-3.5	—	-12	V	
Drain current (Current limitation value)	I _{D limit}	-10	—	—	A	V _{GS} = -12 V, V _{DS} = -10 V ^{Note 4}

Notes; 4. Pulse test

Electrical Characteristics

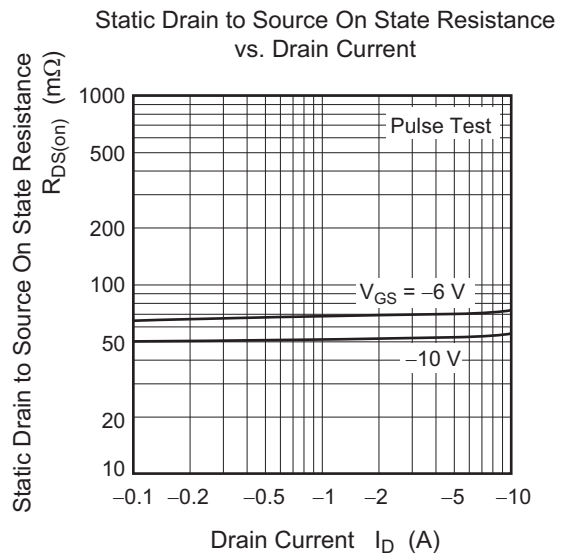
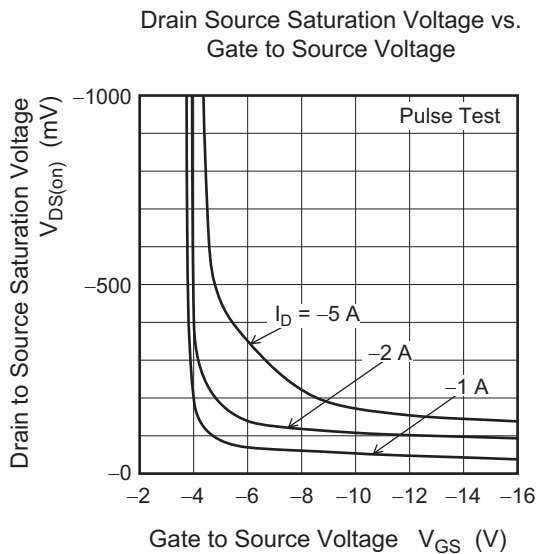
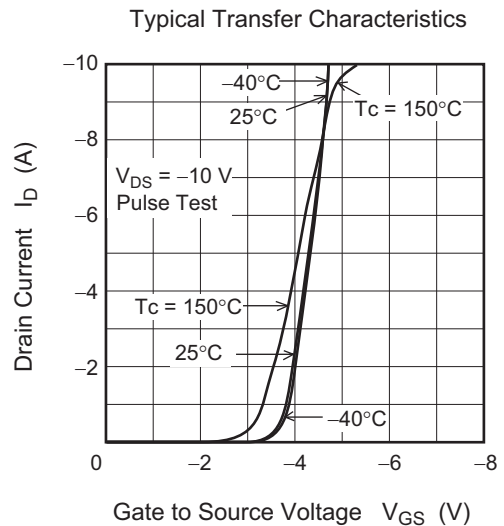
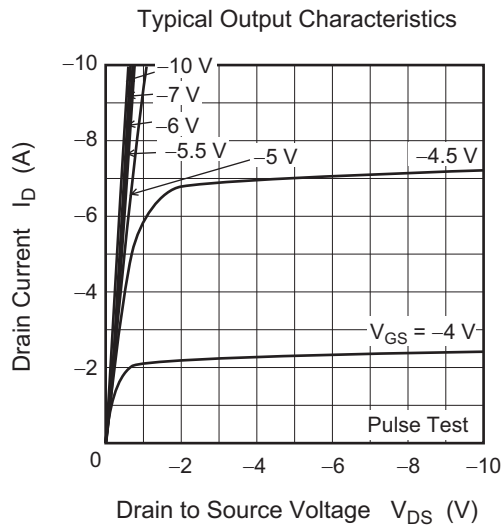
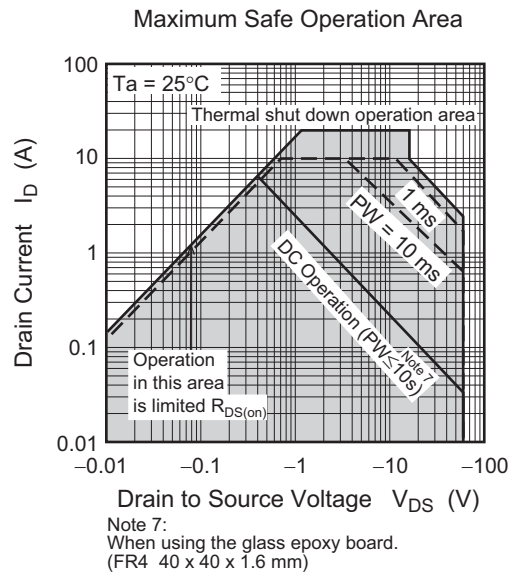
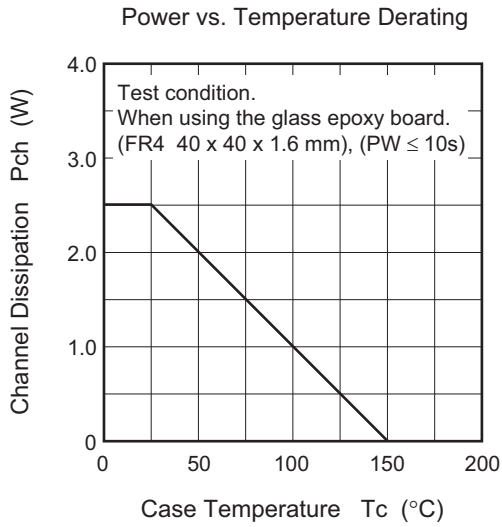
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I _{D1}	—	—	-4	A	V _{GS} = -3.5 V, V _{DS} = -10 V
	I _{D2}	—	—	-10	mA	V _{GS} = -1.2 V, V _{DS} = -10 V
	I _{D3}	-10	—	—	A	V _{GS} = -12 V, V _{DS} = -10 V ^{Note 5}
Drain to source breakdown voltage	V _{(BR)DSS}	-60	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	-16	—	—	V	I _G = -800 μA, V _{DS} = 0
	V _{(BR)GSS}	2.5	—	—	V	I _G = 100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS1}	—	—	-100	μA	V _{GS} = -8 V, V _{DS} = 0
	I _{GSS2}	—	—	-50	μA	V _{GS} = -3.5 V, V _{DS} = 0
	I _{GSS3}	—	—	-10	μA	V _{GS} = -1.2 V, V _{DS} = 0
	I _{GSS4}	—	—	100	μA	V _{GS} = 2.4 V, V _{DS} = 0
Input current (shut down)	I _{GS(OP)1}	—	-0.8	—	mA	V _{GS} = -8 V, V _{DS} = 0
	I _{GS(OP)2}	—	-0.35	—	mA	V _{GS} = -3.5 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS1}	—	—	-10	μA	V _{DS} = -60 V, V _{GS} = 0
Zero gate voltage drain current	I _{DSS2}	—	—	-10	μA	V _{DS} = -48 V, V _{GS} = 0, Ta = 125°C
Gate to source cutoff voltage	V _{GS(off)}	-2.2	—	-3.4	V	V _{DS} = -10 V, I _D = -1 mA
Static drain to source on state resistance	R _{DS(on)}	—	70	95	mΩ	I _D = -5 A, V _{GS} = -6 V ^{Note 5}
	R _{DS(on)}	—	53	65	mΩ	I _D = -5 A, V _{GS} = -10 V ^{Note 5}
Output capacitance	C _{oss}	—	356	—	pF	V _{DS} = -10 V, V _{GS} = 0, f = 1MHz
Turn-on delay time	t _{d(on)}	—	4.4	—	μs	V _{GS} = -10 V, I _D = -5 A, R _L = 6 Ω
Rise time	t _r	—	4.5	—	μs	
Turn-off delay time	t _{d(off)}	—	2.0	—	μs	
Fall time	t _f	—	1.6	—	μs	
Body-drain diode forward voltage	V _{DF}	—	-0.87	—	V	I _F = -10 A, V _{GS} = 0
Body-drain diode reverse recovery time	t _{rr}	—	90	—	ns	I _F = -10 A, V _{GS} = 0 di _F /dt = 50 A/μs
Over load shut down operation time ^{Note 6}	t _{os1}	—	2.6	—	ms	V _{GS} = -6 V, V _{DD} = -16 V

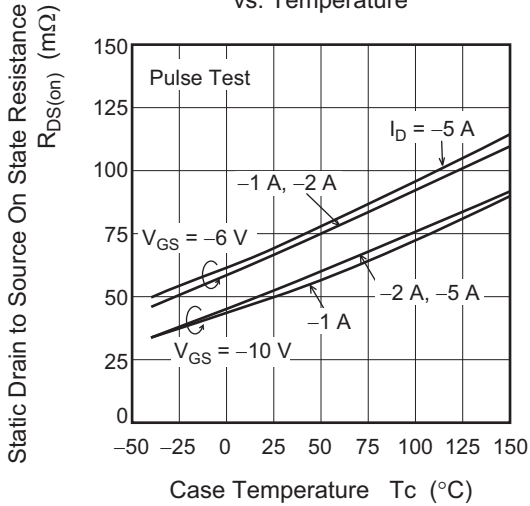
Notes: 5. Pulse test

6. Including the junction temperature rise of the over loaded condition.

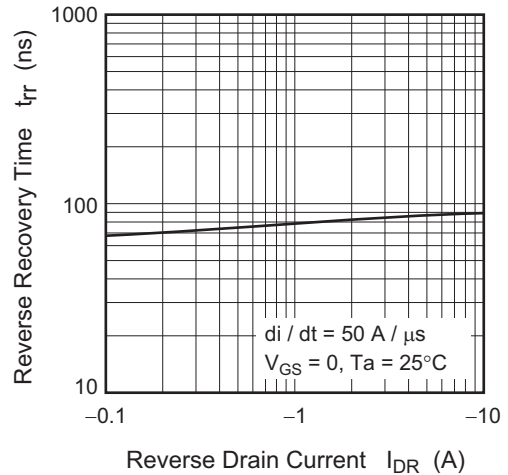
Main Characteristics



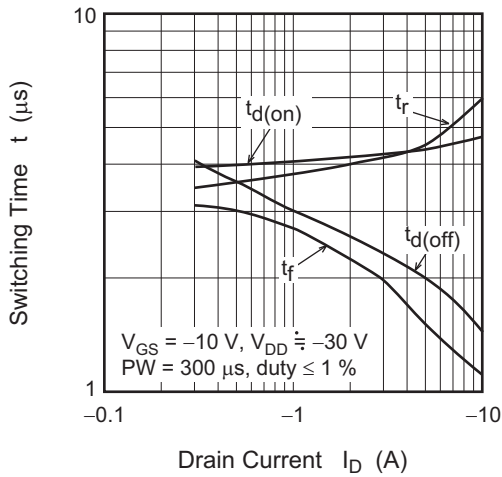
Static Drain to Source On State Resistance vs. Temperature



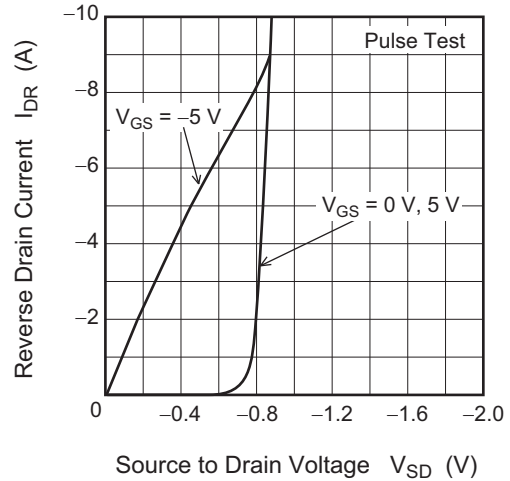
Body-Drain Diode Reverse Recovery Time



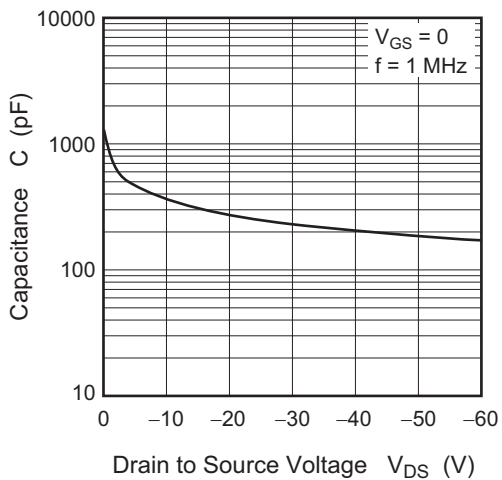
Switching Characteristics



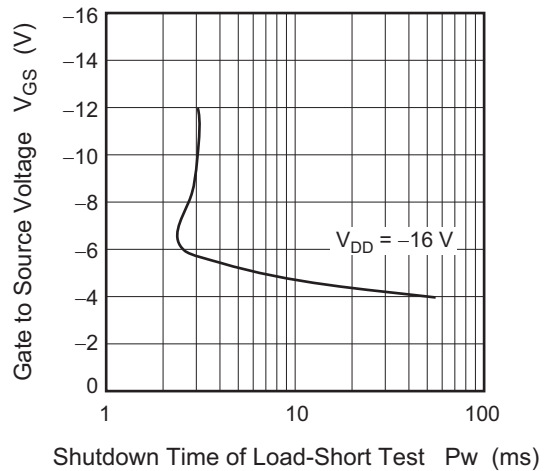
Reverse Drain Current vs. Source to Drain Voltage



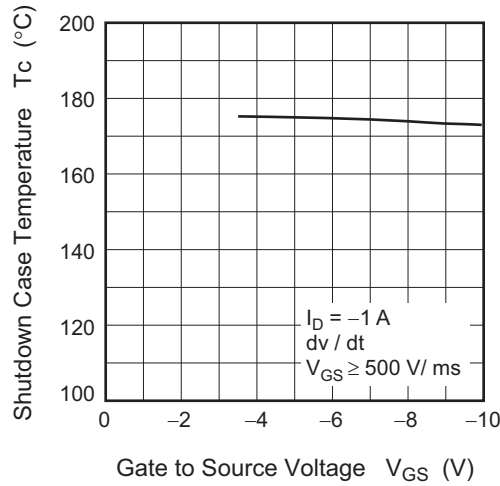
Typical Capacitance vs. Drain to Source Voltage



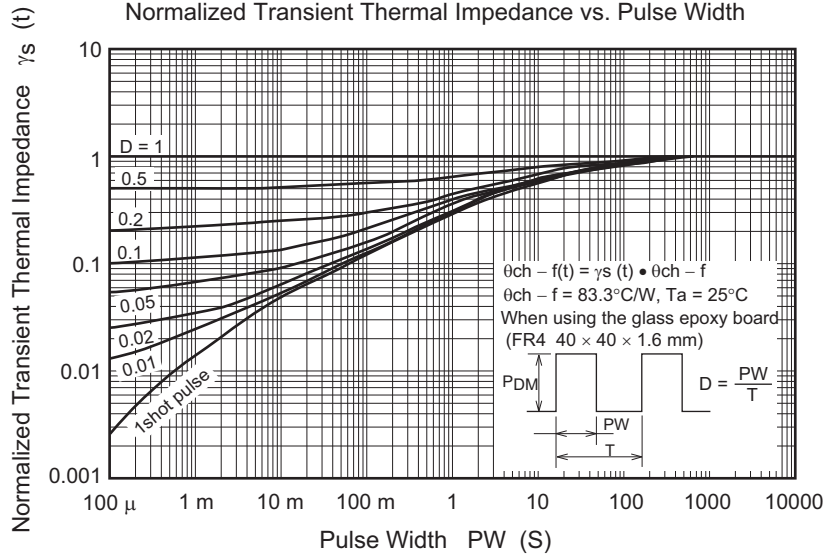
Gate to Source Voltage vs. Shutdown Time of Load-Short Test



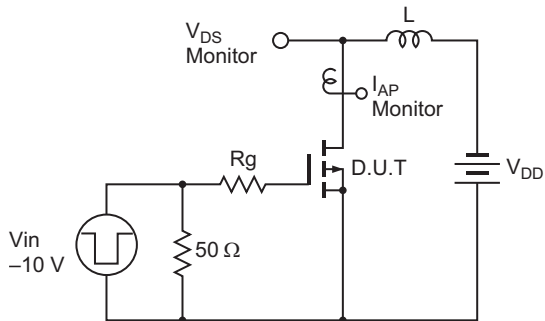
Shutdown Case Temperature vs. Gate to Source Voltage



Normalized Transient Thermal Impedance vs. Pulse Width

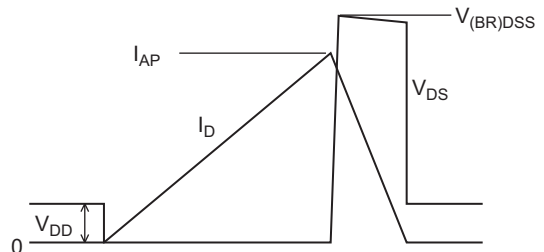


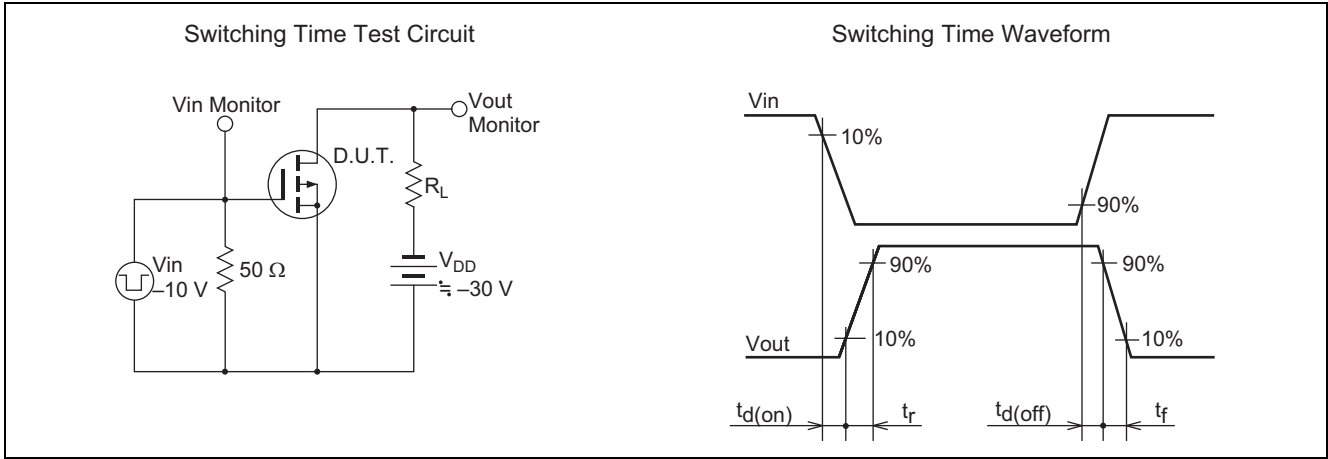
Avalanche Test Circuit



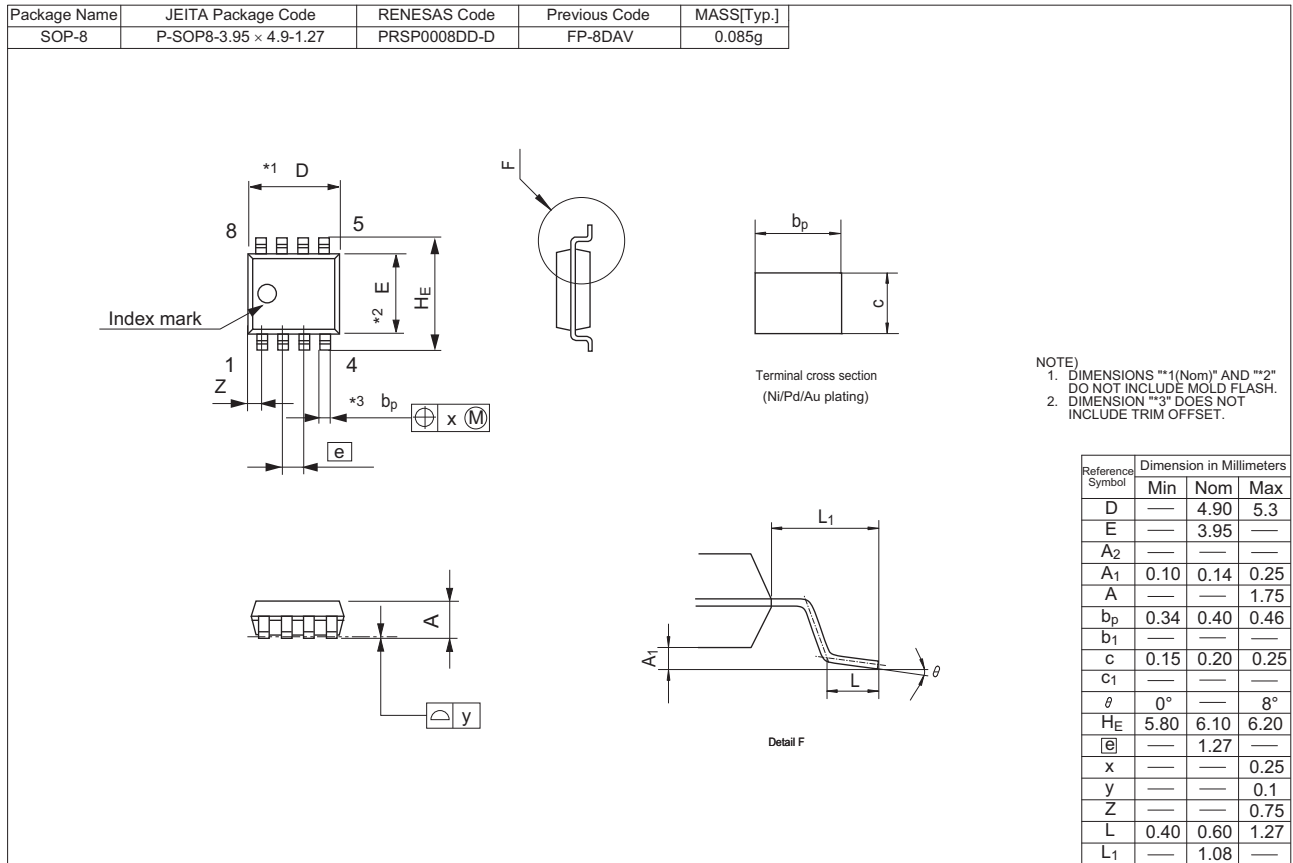
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$





Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RJE0615JSP-00-J0	2500 pcs	Taping

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