Precision Clock Generator for Laser Printers

Features

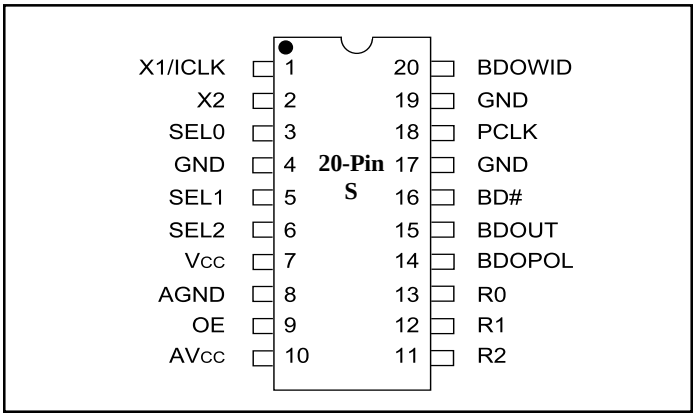
- Supports laser printer pixel rates up to 40 MHz. 70 MHz for "C" speed version.
- Jitter less than 300ps.
- Easily programmable frequency selections via parallel interface. Post divider (R) designed to load only during the Beam Detect interval.
- Source clock input can be from crystal or oscillator.
- Source clock rates from 8 MHz up to 22 MHz (from crystal or oscillator).
- Active LOW asynchronous reset input for synchronization with engine via Beam Detect input.
- Synchronized Beam Detect Output to support external state machines.
- Glitch-less clock output after Beam Detect.
- Supports dynamic frequency changes on a line-per-line basis.
- Mixed line resolution supports half-toning and gray scale operations.
- Minimizes controller memory utilization (low-resolution text mixed with high-resolution images).
- On-chip VCO loop filter (no external components).
- On-chip crystal oscillator (modified Pierce).
- Single 5V power supply.
- Low power consumption.
- 20-pin wide body (300-mil) SOIC package (S)

Description

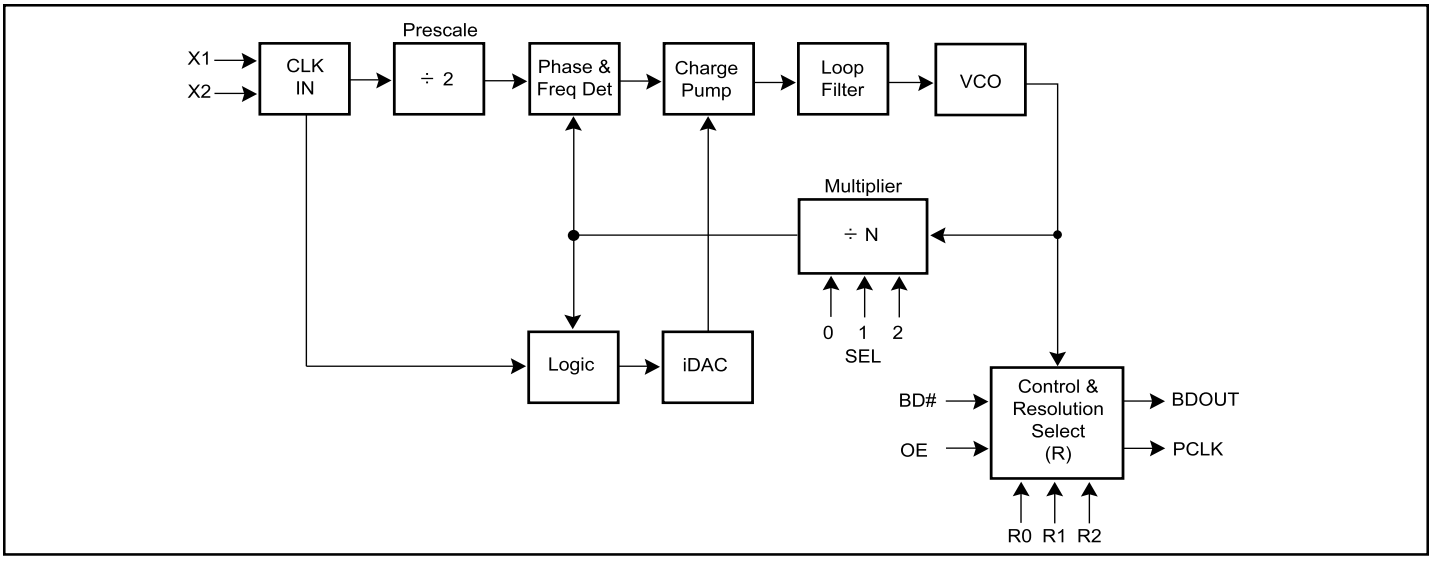
The PI6C1201 is an advanced CMOS clock generator designed specifically to support pixel clock generation in low-cost laser printers. Capable of generating highly stable clock frequencies up to 70 MHz, this device supports printer engines with dot resolutions of 1,200 dpi and above. Page speeds may range from 4 pages per minute to better than 60 pages per minute.

Mixed-line resolution supports half-toning and gray scale operations (low-resolution text mixed with high-resolution images) and minimizes controller memory utilization

Pinout Diagram



Functional Block Diagram



Pin Description

Pin	Name	Description
1	X1/ICLK	**CRYSTAL, or input from external clock source**. This pin is connected to a crystal or may be used to input an external reference frequency. When connected to a crystal, a 33 pF (typ) capacitor should be connected from this pin to ground. When driven by an external clock there is no need for a capacitor.
2	X2	**CRYSTAL. Output of Ring Oscillator.** This pin should typically have a 22 pF capacitor to ground when used with a crystal. For fine-tuning the crystal frequency, this capacitor can be trimmed from 15 pF to 33 pF. If X1 is driven by an external clock source, there is no need for a capacitor.
4	GND	**Digital Ground**
3, 5, 6	SEL(0-2)	**Selects VCO/Crystal Multiplication Ratio**. These pins can be dynamically changed anytime (not recommended during active imaging). These inputs must be tied HIGH/LOW or driven actively to guarantee that the setting stays valid. Refer to Table 2 for additional information. These pins have internal pull-up resistors.
7	V_{CC}	**Digital Vcc**
8	AGND	**Analog Ground**
9	OE	**Output Enable**. When pulled HIGH, this pin will enable the PCLK and the BDOUT outputs. When pulled LOW, these pins are tri-stated. This pin has an internal pull-up resistor.
10	AV_{CC}	**Analog Vcc**
11, 12, 13	R(0-2)	**Output Resolution Selection**. Used to set the final dot resolution. The divide ratios set by these pins are all tightly aligned synchronous outputs designed to eliminate glitches and allow dynamic changes to the output clock dot resolution frequency on a per-line basis. These pins can only be changed during the BD# (Beam Detect) active interval. The signals should be externally latched at least one or two PCLK cycles prior to BD# going active to guarantee internal latches setup and hold times. R0 allows single-pin control for 1/4 or 1/8 mode (assuming R1 and R2 = 1). Please refer to Table 1 for further information. These pins have internal pull-up resistors.
14	BDOPOL	**Beam Detect Output Polarity:** This pin is used to set the polarity of the BDOUT output (pin 15). When this pin is LOW, the BDOUT polarity is active HIGH. When this pin is HIGH, the BDOUT polarity is active LOW. This pin is pulled up internally.
15	BDOUT	**Beam Detect Output**. This pin signals the start of a new line after synchronization has occurred. The BDOUT signal will go active when the incoming BD# signal is detected and synchronized. The width of this pulse is dependent upon the VCO frequency and the current PCLK setting. Please refer to the timing diagram for additional information. The polarity of BDOUT can be controlled by BDOPOL (pin 14) and the width can be set to 1 or 2 PCLKs by BDOWID (pin20). BDOUT can be tri-stated by the OE pin. BDOUT has a 12mA balanced drive CMOS output.
16	BD#	**Beam Detect Input from Engine**. The engine signal that drives this pin indicates that the end (or beginning) of a line has been detected. Since this signal is typically an asynchronous strobe, this active-low **edge-sensitive** input is extremely metastable-resistant. This input has a TTL-compatible input threshold with hysteresis. This pin has an internal pull-up resistor.
17	GND	**Digital Ground**
18	PCLK	**Pixel Clock Output**. The output frequency of this pin is a function of the crystal (or input clock) frequency (pre-scaled to ÷2), the multiply ratio as set by SEL(0-2) and the final divide ratio as set by R(0-2): PCLK = Crystal x (1/2) x [32, 16, or 8 as defined by SEL(0-1)] x (1/8 or 1/4 as controlled by R0 - assumes R1=R2=1). This output can be glitchlessly synchronized to an external asynchronous event by asserting the BD# input. The minimum indeterminacy of the alignment to the external event is controlled by the width of the VCO clock. Please refer to timing diagrams for additional information. The PCLK output can be tri-stated by the OE pin. This pin has a 12mA balanced-drive CMOS output.
19	GND	**Digital Ground**
20	BDOWID	**Beam Detect Output Width:** This pin is used to set the width of the BDOUT output (pin 15). When this pin is LOW, the BDOUT width is two PCLK periods. When this pin is HIGH, the BDOUT width is one PCLK period. This pin has an internal pull-up resistor.

Basic PLL Flow Diagram

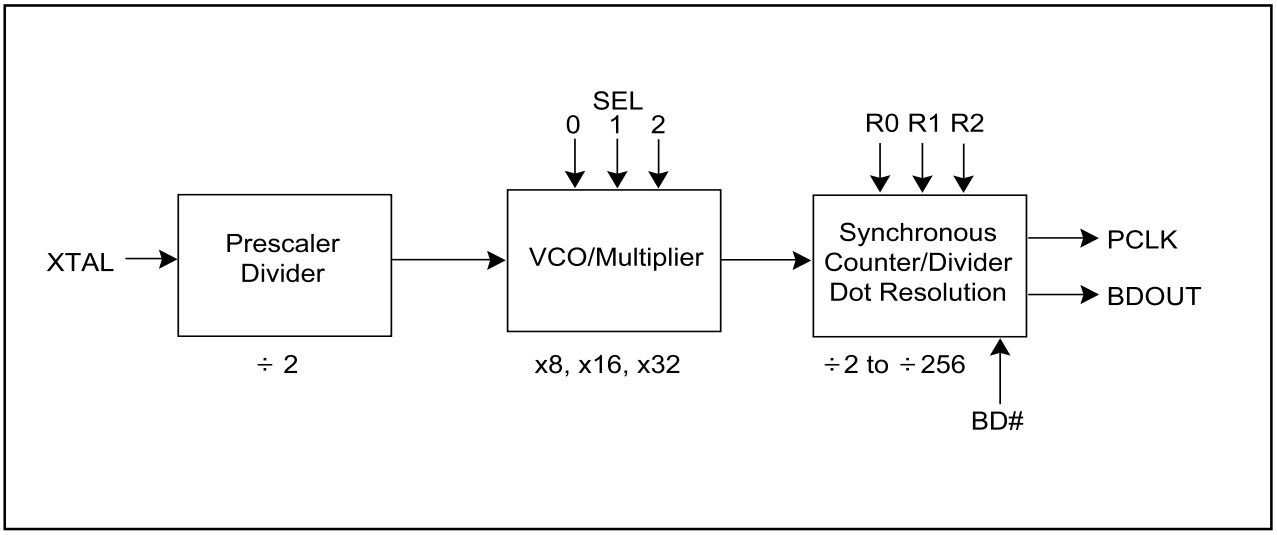


Table 1. Dot Resolution Divider Pin Setting

R2	R1	R0	Function	R
0	0	0	÷ 16	16
0	0	1	÷ 32	32
0	1	0	÷ 64	64
0	1	1	÷ 128	128
1	0	0	÷ 256	256
1	0	1	÷ 2	2
1	1	0	÷ 4	4
1	1	1	÷ 8	8

Note:

1. The relationship of the VCO to PCLK is controlled by the R synchronous divider.
   For example:
   (a) 1 PCLK = 4 VCO clocks if R0 = 0 & R1 = R2 = 1
   (b) 1 PCLK = 8 VCO clocks if R0 = 1 & R1 = R2 = 1

Table 2. VCO Multiplier Pin Setting

SEL2	SEL1	SEL0	Function
1	0	0	Reserved
1	0	1	x8
1	1	0	x32
1	1	1	x16

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc only)	–0.3V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0 W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (V_{CC} = 5V±10% for "blank" and "A" speed, Vcc = 5V ±5% for "C" speed. T_A = 0°C to 70°C)

Symbol	Description	Test Conditions[2]	Min.	Typ.[3]	Max.	Units
V_{IH}[1]	Input HIGH Voltage	All Inputs except X1 & BD#	2.0	—	—	V
$V_{IH}X1$[1]	Input HIGH Voltage X1	X1 Input	Vcc-1.0	—	—	
V_{BDTH}[1]	Input Threshold Voltage BD#	V_{CC} = 4.5V to 5.5V	1.2	—	1.4	
V_{IL}[1]	Input LOW Voltage	All Inputs	—	—	0.8	
I_{IH}	Input HIGH Current with Pull-up	All Inputs except X1 V_{CC} = Max., V_{IN} = V_{CC}	—	—	5	µA
I_{IL}	Input LOW Current with Pull-up	All Inputs except X1, V_{CC} = Max., V_{IN} = 0V	–50	—	—	
$I_{IH}X1$	Input HIGH Current X1	X1 Input, V_{CC} = Max. V_{IN} = V_{CC}	—	—	150	
$I_{IL}X1$	Input LOW Current X1	X1 Input, V_{CC} = Max. V_{IN} = 0V	–150	—	—	
V_{OH}	Output HIGH Voltage	All Outputs except X2 V_{CC} = Min., I_{OH} = –12mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	All Outputs except X2, V_{CC} = Min., I_{OL} = +12mA	—	—	0.4	
I_{OS}[1,4]	Short Circuit Current	V_{CC} = 5.25V V_{OUT} = GND	25	—	—	mA
I_{C160}	Dynamic Supply Current	V_{CC} = 5.0V, X1 = 20 MHz SEL = x16	—	—	35	
I_{C240}	Dynamic Supply Current (for 6C1201A only)	V_{CC} = 5.0V, X1 = 15 MHz SEL = x32	—	—	50	
I_{C280}[5]	Dynamic Supply Current (for 6C1201C only)	V_{CC} = 5.0V, X1 = 17.5 MHz, SEL = x32	—	—	60	

Notes:
1. These parameters are guaranteed by design and measured at characterization only.
2. For Max. or Min. conditions, use appropriate values specified under Electrical Characteristics for the appropriate device type.
3. Typical values are shown at Vcc = 5.0V, +25°C ambient and maximum loading.
4. Not more than one output should be shorted at one time. Duration of test should not exceed one second.
5. "C" speed operation is limited to a ±5% Vcc tolerance

Switching Characteristics

Vcc = 5V ±10% for "blank" and "A" Speed, Vcc = 5V ±5% for "C" Speed. T_A = 0º C to 70º C

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
tR(1)	PCLK Output Rise Time (0.8V to 2.0V)	CL = 30 pF	—	—	2	ns
tF(1)	PCLK Output Fall Time (2.0V to 0.8V)		—	—	2	
tPZH(1) tPZL(1)	OE to PCLK Output Enable Time (Please refer to the Test Circuit & Waveform)	CL = 30 pF, RL = 500Ω Rpu = 500Ω to 7V (for tPZL and tPLZ only)	1.5	—	7.5	
tPHZ(1) tPLZ(1)	OE to PCLK Output Disable Time (Please refer to the Test Circuit & Waveform)		1.5	—	6.0	
dT(1)	PCLK Duty Cycle		—	50/50	45/55	%
FXTALin	Crystal Input Frequency (Production tested at 15.0 MHz)	Within the following VCO frequency range:	8	—	22	MHz
Fin	Driven Input Frequency (Production tested at 4,20,22, and 30 MHz)		8	—	22	
Fvco(2)	VCO Frequency (Max. PCLK = 40 MHz)	"blank" Speed Grade	120	—	176	
Fvco(2)		"A" Speed Grade	120	—	240	
Fvco(2)	VCO Frequency (Max. PCLK = 70 MHz)	"C" Speed Grade (±5% Vcc)	120	—	280	
Tjis(1)	PCLK one sigma jitter	X1 = 15 MHz, SEL = x32, R = 8	—	50	—	ps
Tjab(1)	PCLK short term peak-to-peak jitter		—	—	300	
Tvco(3)	VCO clock period		3.571	—	8.333	ns
TPCLK(4)	PCLK clock period		—	—	—	

Notes:

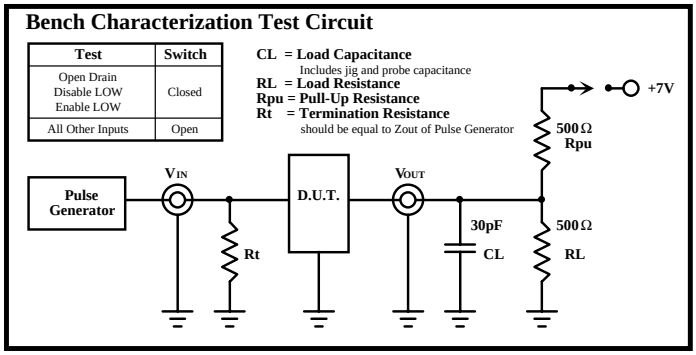
1. These parameters are guaranteed by design and measured at characterization only.
2. The VCO frequency can be determined by the following formula:

$$F_{VCO} = \frac{F_{XTALin \text{ or } Fin}}{2} \times N$$

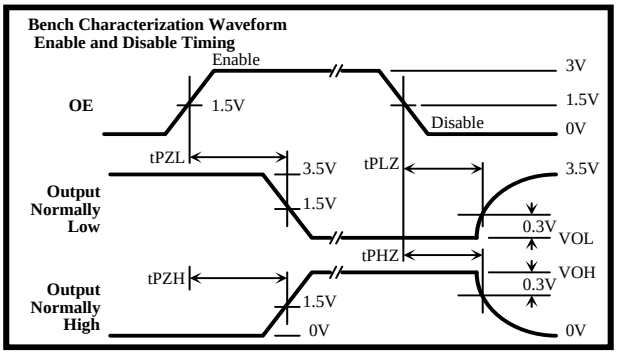
   N = VCO multiplier value. See Table 2

   For example: For X1 = 20 MHz and SEL = x16, then: Fvco = (20 MHz / 2) x 16 = 160 MHz
   For X1 = 15 MHz and SEL = x32, then: Fvco = (15 MHz / 2) x 32 = 240 MHz
3. The VCO clock period is determined by the formula: T_{VCO} = 1 / F_{VCO}. For design aid only.
4. T_{PCLK} = T_{VCO} x R, R = output dot resolution divider function (see Table 1).
   For design aid only. Not subject to production testing.

Bench Characterization Test Circuit



Bench Characterization Waveform
Enable and Disable Timing



Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Zout ≤ 50Ω, tF, tR ≤ 2.5ns

Timing Table[4]

Vcc = 5V ±10% for "blank" and "A" Speed, Vcc = 5V ±5% for "C" Speed. T_A = 0º C to 70º C

Sym.	Description	Min.	Typ.	Max.
T1	Minimum BD# Pulse Width[2]	22 TVCO	—	—
T2[1]	Time from BD# Active to BDsync	18 TVCO	—	19 TVCO
T3	Synchronous Time from BD# to BDOUT	19 TVCO + 0.5 TPCLK + t_D - 0.5 tJT3	—	20 TVCO + 0.5 TPCLK + t_D + 0.5 tJT3
T4[1]	Width of BDOUT Pulse BDOWID = 0 BDOWID = 1	2 TPCLK -0.5 tJT4 1 TPCLK -0.5 tJT4	2 TPCLK 1 TPCLK	2 TPCLK + 0.5 tJT4 1 TPCLK + 0.5 tJT4
T5	Time from BDOUT active to the first valid rising edge of PCLK	0.47 TPCLK - 0.5 tJT5	0.5 TPCLK	0.5 TPCLK + 0.5 tJT5
T6	Total time from BD# active to the first valid rising edge of PCLK	T3 + T5 = 19 TVCO + 0.97 TPCLK + t_D – 0.5 tJT6	—	T3 + T5 = 20 TVCO + 1.0 TPCLK + t_D + 0.5 tJT6
t_D	On-chip total buffer delays	See Note 3	—	See Note 3
tJT3[5]	T3 peak-to-peak jitter	0ps	—	300 ps
tJT4[5]	T4 peak-to-peak jitter	0ps	—	300 ps
tJT5[5]	T5 peak-to-peak jitter	0ps	—	300 ps
tJT6[5]	T6 peak-to-peak jitter	0ps	—	300 ps

Notes:

1. These parameters are guaranteed by design and functional test only.
2. The width of the BD# pulse (T1) MUST meet the minimum width requirements of 22 TVCO. BD# pulses less than 22 TVCO will not achieve synchronization and will not generate BDOUT.
   For measurement purposes, the falling edge of BD# should be 6 ns or less.
3. $\mathbf{t_D}$ is extracted from initial product characterization. It varies with both Vcc and temperature. The following linear regression formulas may be used to calculate $\mathbf{t_D}$ for 4.5V ≤ Vcc ≤ 5.5V and $0^oC \le T_A \le 70^oC$. This is provided for design purposes only. A ±10% guardband of the calculated value will be used for production testing.

a. Linear regression of t_D vs. Vcc at a fixed temperature: t_D = Slope x Vcc + Intercept

Temperature (ºC)	0	20	40	60	80
Intercept (ns)	14.032	14.756	15.585	16.771	17.107
Slope (ns/V)	-1.224	-1.296	-1.396	-1.568	-1.564

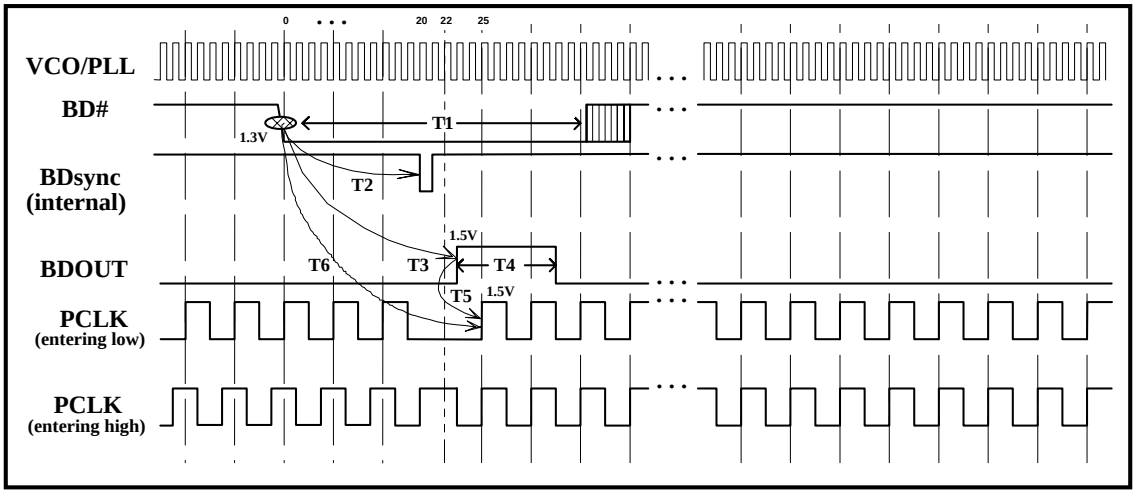
b. Linear regression of t_D vs. Temperature at a fixed Vcc: t_D = Slope x Temperature + Intercept

Vcc (V)	4.50	4.75	5.00	5.25	5.50
Intercept (ns)	8.578	8.206	7.872	7.586	7.364
Slope (ns/ºC)	0.019	0.018	0.017	0.017	0.014

4. T_{VCO} = VCO clock period. T_{PCLK} = PCLK clock period.
5. Parameters obtained from initial characterization, not subject to production testing.

Timing Diagram

PLL to Output Clock and Beam Detect Reset Sequence



Note:

1. The PCLK frequency in this example is 1/4 the VCO frequency (R0=0 & R1=R2=1 → see Table 1)
   For measurement purposes the BD# falling edge should be less than 6ns for 90% to 10%.

Vcc Power-Up and VCO Ramp to Lock Timing (Provided for Implementation Reference Purposes only).