

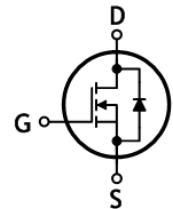
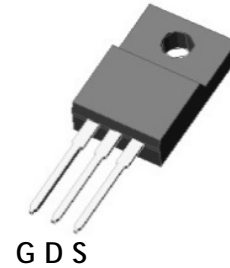
## SWITCHING REGULATOR APPLICATION

### Features

- $BV_{DSS}=800V$  (Min.)
- Low gate charge:  $Q_g=19nC$  (Typ.)
- Low drain-source On resistance:  $R_{DS(on)}=4.2\Omega$  (Max.)
- RoHS compliant device
- 100% avalanche tested

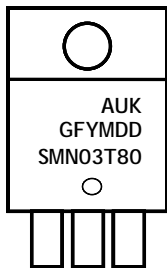
### Ordering Information

Part Number	Marking	Package
SMN03T80F	SMN03T80	TO-220F-3L



TO-220F-3L

### Marking Information



Column 1 : Manufacturer  
 Column 2 : Production Information  
 e.g.) GFYMDD  
 -. G : Option Code (H : Halogen Free)  
 -. F : Factory Management Code  
 -. YMDD : Date Code (Year, Month, Date)  
 Column 3 : Device Code

### Absolute maximum ratings ( $T_C=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	800	V	
Gate-source voltage	$V_{GSS}$	$\pm 30$	V	
Drain current (DC) *	$I_D$	$T_C=25^\circ C$	3	A
		$T_C=100^\circ C$	1.83	A
Drain current (Pulsed) *	$I_{DM}$	12	A	
Single pulsed avalanche energy <sup>(Note 2)</sup>	$E_{AS}$	200	mJ	
Repetitive avalanche current <sup>(Note 1)</sup>	$I_{AR}$	3	A	
Repetitive avalanche energy <sup>(Note 1)</sup>	$E_{AR}$	2.8	mJ	
Power dissipation	$P_D$	28	W	
Junction temperature	$T_J$	150	$^\circ C$	
Storage temperature range	$T_{stg}$	-55~150	$^\circ C$	

\* Limited only maximum junction temperature

## Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 4.46	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

## Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$BV_{DSS}$	$I_D=250\mu\text{A}, V_{GS}=0$	800	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}, V_{DS}=V_{GS}$	2	-	4	V
Drain-source cut-off current	$I_{DSS}$	$V_{DS}=800\text{V}, V_{GS}=0\text{V}$	-	-	10	$\mu\text{A}$
		$V_{DS}=640\text{V}, T_C=125^\circ\text{C}$	-	-	100	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$	-	-	$\pm 100$	nA
Drain-source on-resistance <sup>(Note 3)</sup>	$R_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=1.5\text{A}$	-	3.36	4.2	$\Omega$
Forward transfer conductance <sup>(Note 3)</sup>	$g_{fs}$	$V_{DS}=30\text{V}, I_D=1.5\text{A}$	-	3.7	-	S
Internal gate resistance	$R_G$	$f=1\text{MHz}, V_{DS}=0\text{V}$	-	3	10	$\Omega$
Input capacitance	$C_{iss}$	$V_{DS}=25\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$	-	696	-	pF
Output capacitance	$C_{oss}$		-	65	-	
Reverse transfer capacitance	$C_{rss}$		-	10.2	-	
Turn-on delay time <sup>(Note 3,4)</sup>	$t_{d(on)}$	$V_{DD}=400\text{V}, I_D=3\text{A}, R_G=25\Omega$	-	48	-	ns
Rise time <sup>(Note 3,4)</sup>	$t_r$		-	36	-	
Turn-off delay time <sup>(Note 3,4)</sup>	$t_{d(off)}$		-	106	-	
Fall time <sup>(Note 3,4)</sup>	$t_f$		-	41	-	
Total gate charge <sup>(Note 3,4)</sup>	$Q_g$	$V_{DS}=640\text{V}, V_{GS}=10\text{V}, I_D=3\text{A}$	-	19	-	nC
Gate-source charge <sup>(Note 3,4)</sup>	$Q_{gs}$		-	4	-	
Gate-drain charge <sup>(Note 3,4)</sup>	$Q_{gd}$		-	7.6	-	

## Source-Drain Diode Ratings and Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_S$	Integral reverse diode in the MOSFET	-	-	3	A
Source current (Pulsed)	$I_{SM}$		-	-	12	A
Forward voltage	$V_{SD}$	$V_{GS}=0\text{V}, I_S=3\text{A}$	-	-	1.5	V
Reverse recovery time <sup>(Note 3,4)</sup>	$t_{rr}$	$I_S=3\text{A}, V_{GS}=0\text{V}, di_F/dt=100\text{A}/\mu\text{s}$	-	372	-	ns
Reverse recovery charge <sup>(Note 3,4)</sup>	$Q_{rr}$		-	1.8	-	$\mu\text{C}$

Note:

1. Repeated rating: Pulse width limited by safe operating area
2.  $L=42\text{mH}, I_{AS}=3\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

## Electrical Characteristic Curves

Fig. 1  $I_D - V_{DS}$

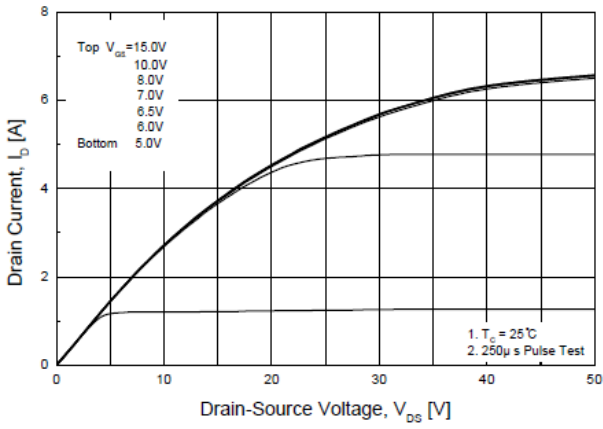


Fig. 2  $I_D - V_{GS}$

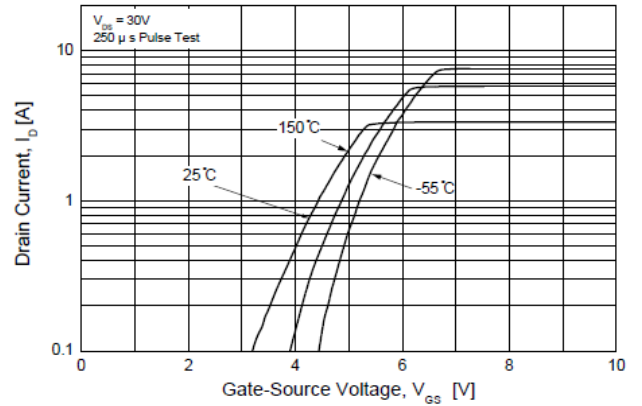


Fig. 3  $R_{DS(ON)} - I_D$

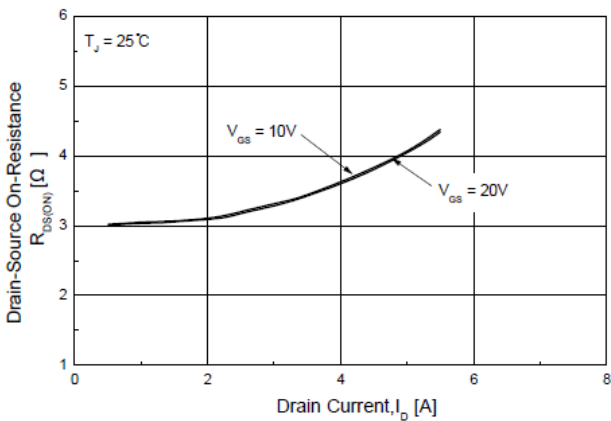


Fig. 4  $I_{DR} - V_{SD}$

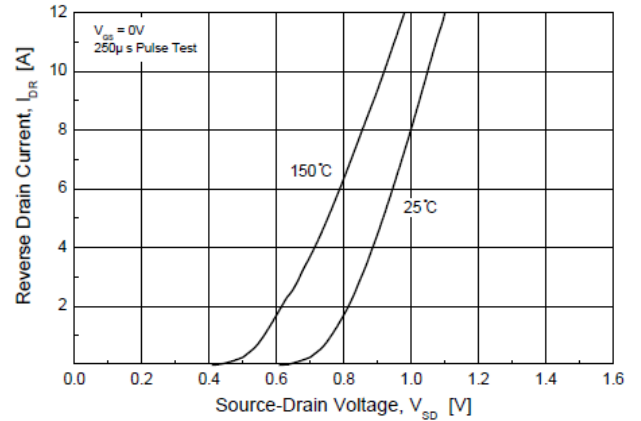


Fig. 5 Capacitance -  $V_{DS}$

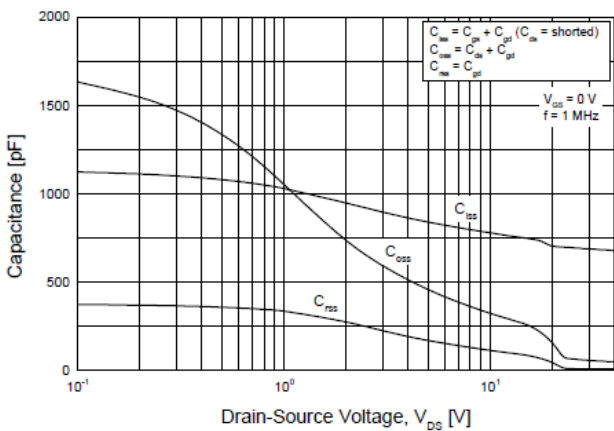
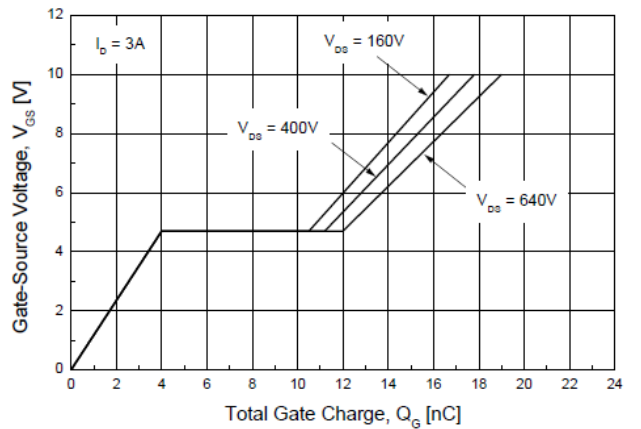


Fig. 6  $V_{GS} - Q_G$



Electrical Characteristic Curves (Continue)

Fig. 7  $BV_{DSS} - T_J$

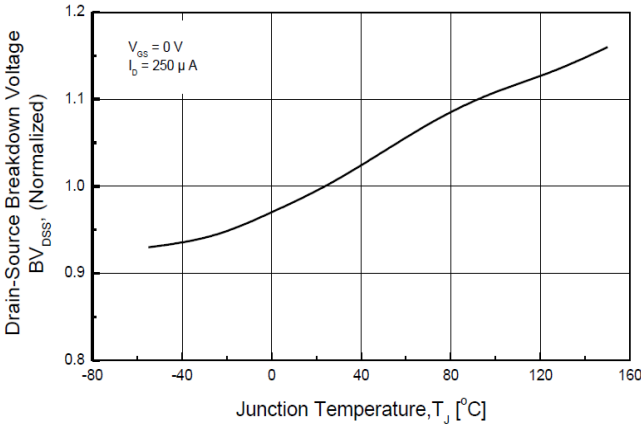


Fig. 8  $R_{DS(ON)} - T_J$

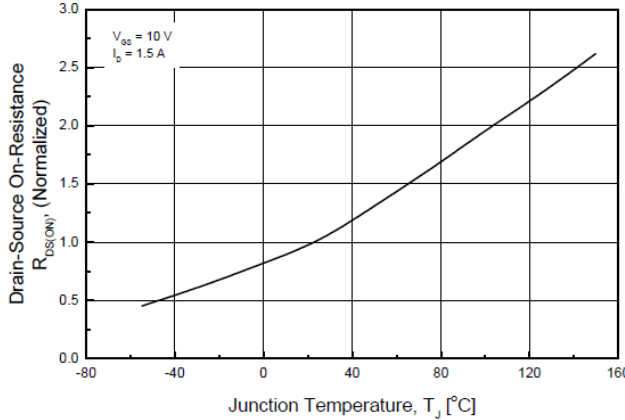


Fig. 9  $I_D - T_C$

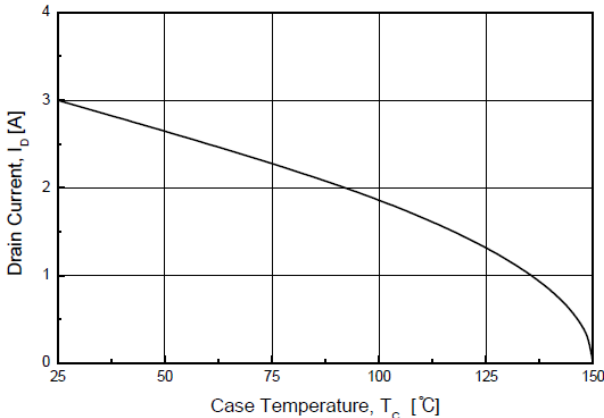


Fig. 10  $V_{GS(th)} - T_J$

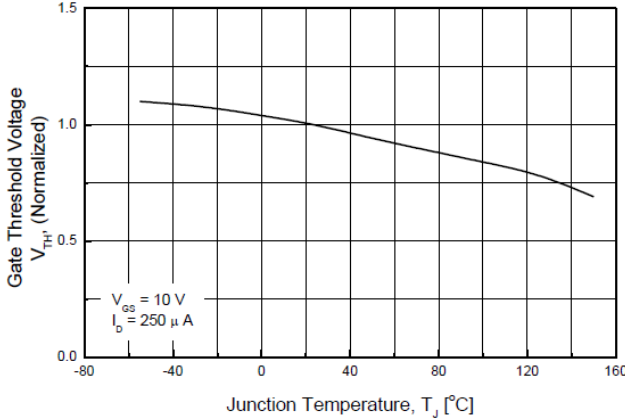


Fig. 11 Safe Operating Area

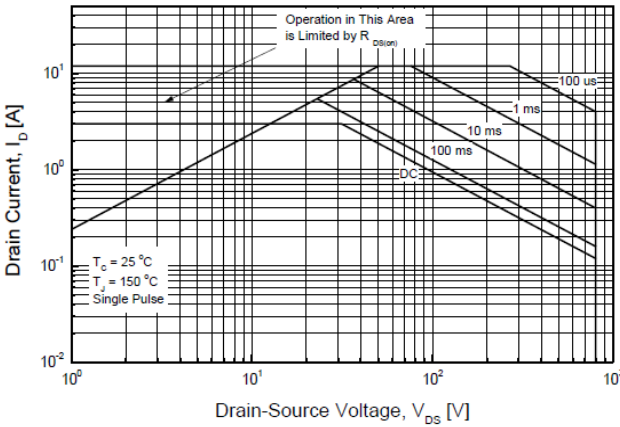


Fig. 12 Gate Charge Test Circuit & Waveform

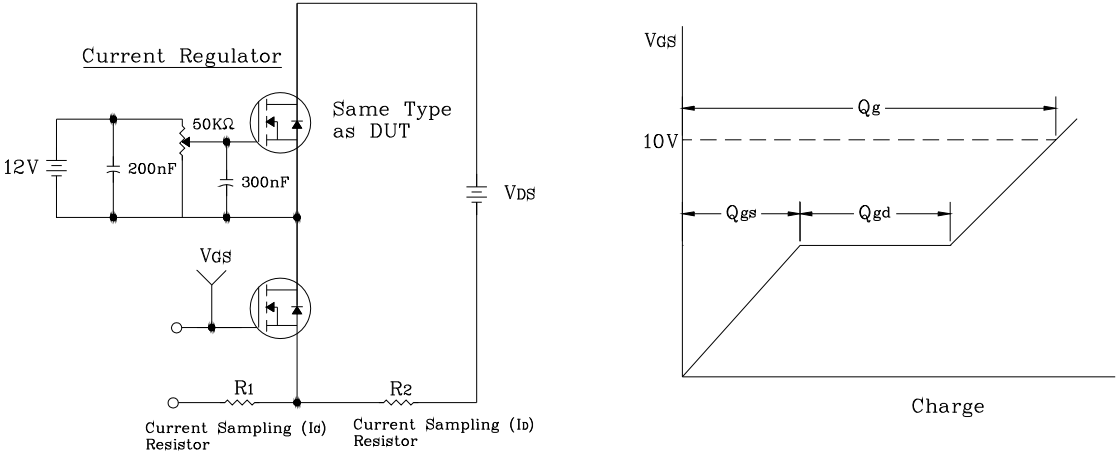


Fig. 13 Resistive Switching Test Circuit & Waveform

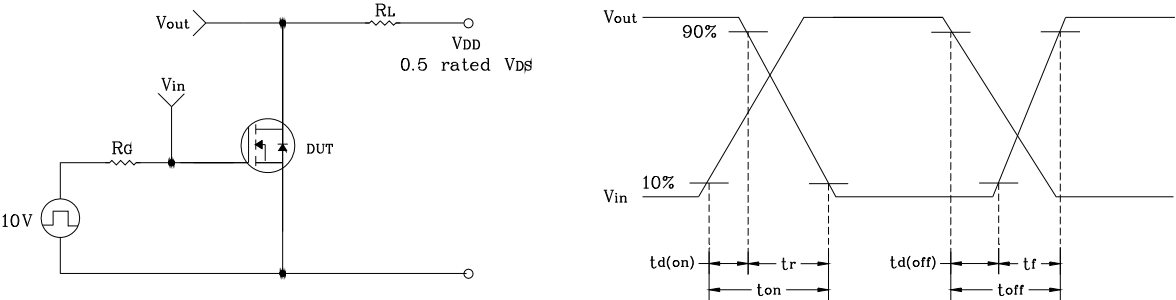


Fig. 14 E<sub>AS</sub> Test Circuit & Waveform

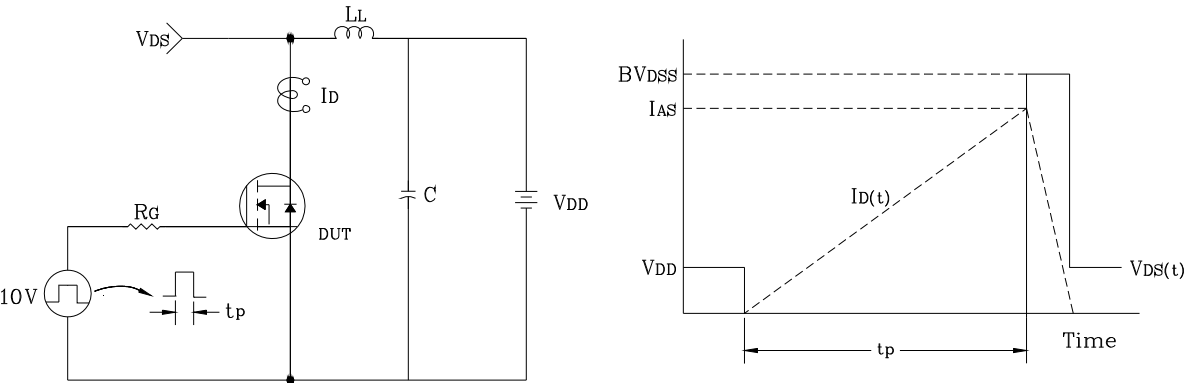
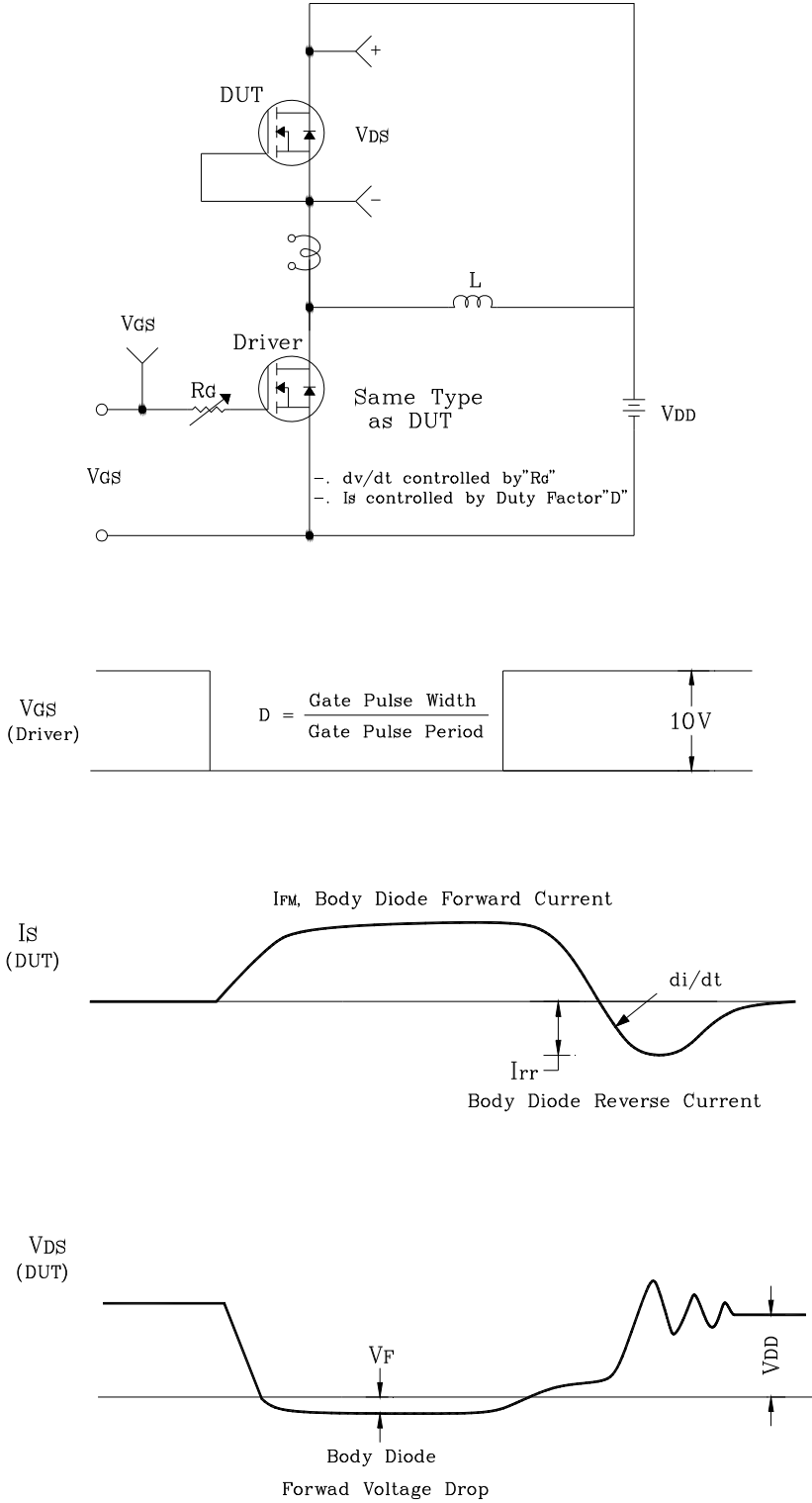
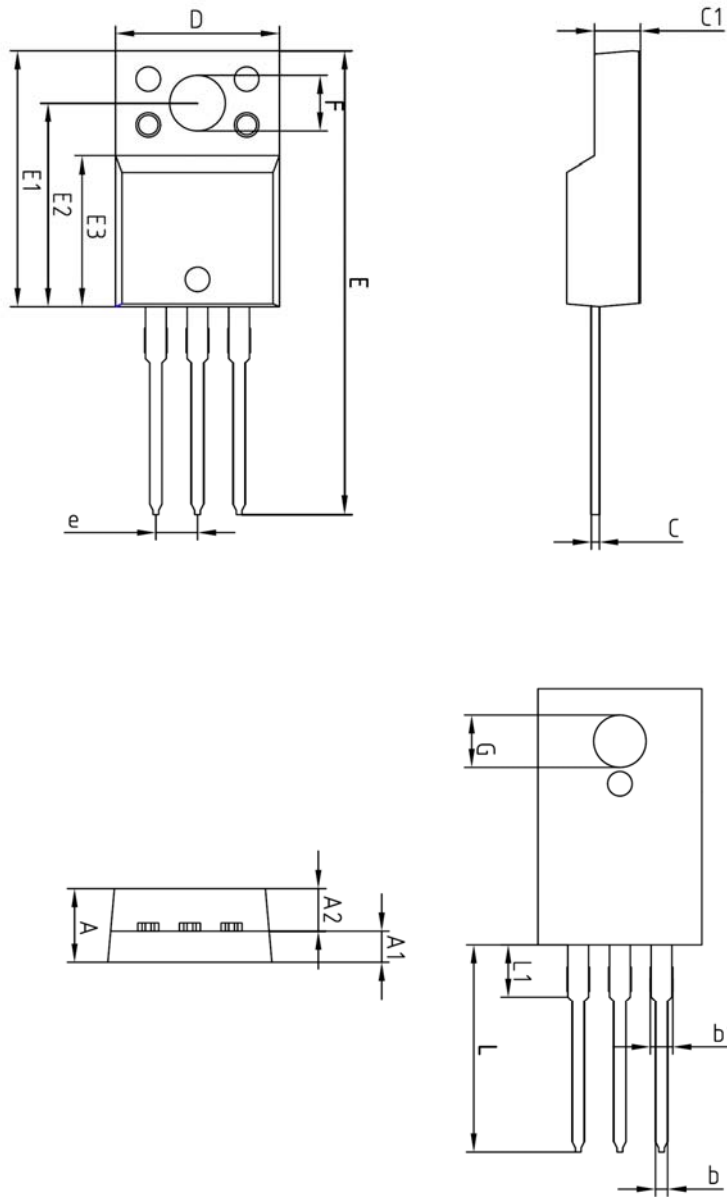


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



## Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	-	-	4.60	
A1	2.45	2.50	2.55	
A2	1.95	2.00	2.05	
b	0.65	0.75	0.85	
b1	1.07	1.27	1.47	
C	0.40	0.50	0.60	
C1	2.70	2.80	2.90	
D	9.90	10.00	10.10	
E	28.00	-	28.60	
E1	15.50	15.60	15.70	
E2	12.30	12.40	12.50	
E3	9.15	9.20	9.25	
F	3.30	3.40	3.50	
G	3.10	3.20	3.30	
e	2.54 BSC			
L	12.40	-	13.00	
L1	3.46 BSC			

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