

## Selectable Adjustable/Fixed Low dropout 300mA Linear Regulator

### Features

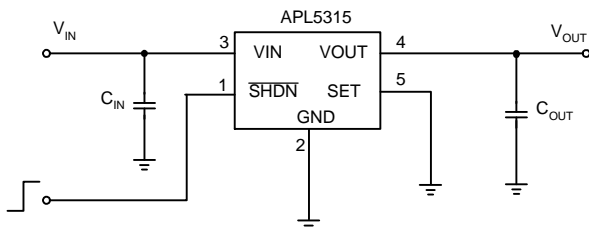
- **Wide Operating Voltage: 2.8~6V**
- **Low Dropout Voltage:**  
**230mV(typical) @ 300mA**
- **Guaranteed 300mA Output Current**
- **Two Modes for Setting Output Voltage**
  - **Fixed Output Voltage: 1~5V**
  - **Adjustable Output Voltage: 0.8~5.5V**
- **Current Limit Protection with Foldback Current**
- **Internal Soft-Start**
- **Over Temperature Protection**
- **Stable with Low ESR Ceramic Capacitor**
- **SOT-23-5 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

### General Description

The APL5315 is a P-channel low dropout linear regulator which needs only one input voltage from 2.8~6V, and delivers current up to 300mA to set output voltage. It also can work with low ESR ceramic capacitors and is ideal for using in the battery-powered applications such as notebook computers and cellular phones. Typical dropout voltage is only 230mV at 300mA loading.

The APL5315 provides two kinds of output voltage operation modes for setting the output voltage. Fixed output voltage mode senses the output voltage on VOUT, adjustable output voltage mode needs two resistors as a voltage divider. Current limit with current foldback and thermal shutdown functions protect the device against current over-loads and over temperature. The APL5315 is available in a SOT-23-5 package.

### Simplified Application Circuit



### Applications

- **Cellular Phones**
- **Portable and Battery-powered Equipment**
- **Notebook and Personal Computers**

### Ordering and Marking Information

<p>APL5315 <span style="font-family: monospace;">□□□□ - □□ □</span></p> <div style="margin-left: 40px;"> <p>□□□□ — Assembly Material</p> <p>□□ — Handling Code</p> <p>□ — Temperature Range</p> <p>□□ — Package Code</p> <p>□□ — Voltage Code</p> </div>	<p>Package Code B : SOT-23-5</p> <p>Operating Junction Temperature Range I : -40 to 85°C</p> <p>Handling Code TR : Tape &amp; Reel</p> <p>Voltage Code 12 : 1.2V                      Blank : Adjustable</p> <p>Assembly Material L : Lead Free Device G : Halogen and Lead Free Device</p>
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Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

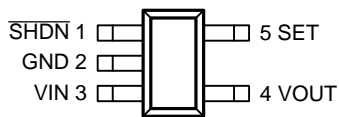
## Marking Information

Product Name	Marking	Product Name	Marking	Product Name	Marking
APL5315	35RX	APL5315-12	355X	APL5315-15	359X
APL5315-18	35CX	APL5315-25	35JX	APL5315-33	35RX <sup>(Note2)</sup>

Note1 : Other voltage version please contact ANPEC for detail.

Note2 : Because APL5315 and APL5315-33 are identical, the marking of APL5315 is same as APL5315-33.

## Pin Configuration



SOT-23-5

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
$V_{IN}$	VIN Supply Voltage (VIN to GND)	-0.3 ~ 6.5	V
$V_{\overline{SHDN}}$	SHDN Input Voltage ( $\overline{SHDN}$ to GND)	-0.3 ~ 6.5	V
$P_D$	Power Dissipation	Internally Limited	W
$T_J$	Junction Temperature	-40 ~ 150	°C
$T_{STG}$	Storage Temperature	-65 ~ 150	°C
$T_{SDR}$	Lead Soldering Temperature, 10 Seconds	260	°C

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
$\theta_{JA}$	Thermal Resistance-Junction to Ambient <sup>(Note 3)</sup>	240	°C/W
$\theta_{JC}$	Thermal Resistance-Junction to Case	130	°C/W

Note3 :  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air.

## Recommended Operating Conditions

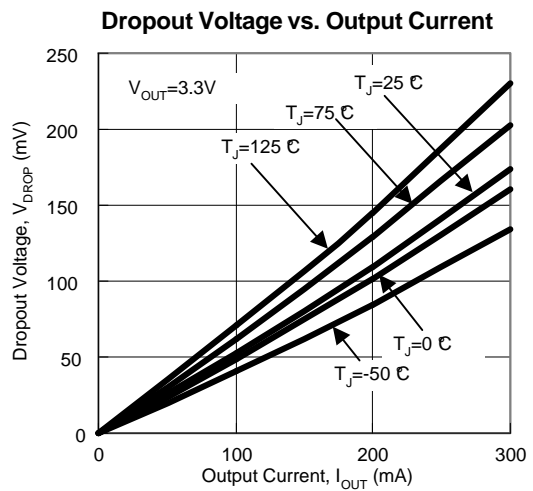
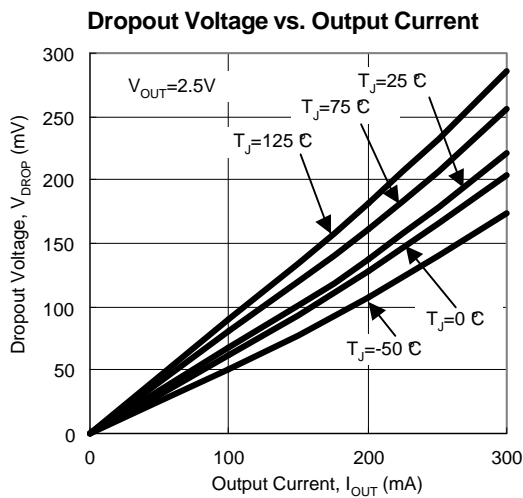
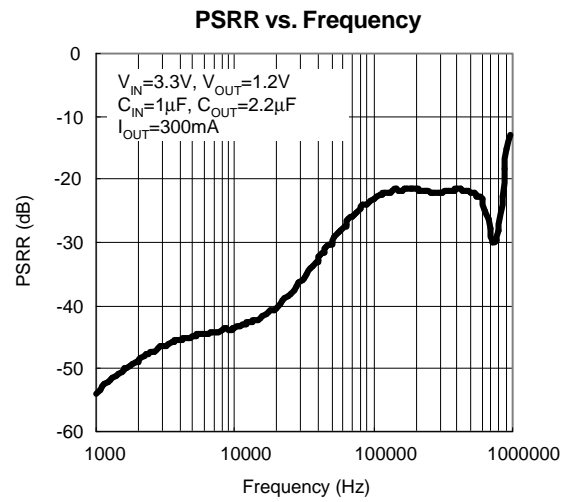
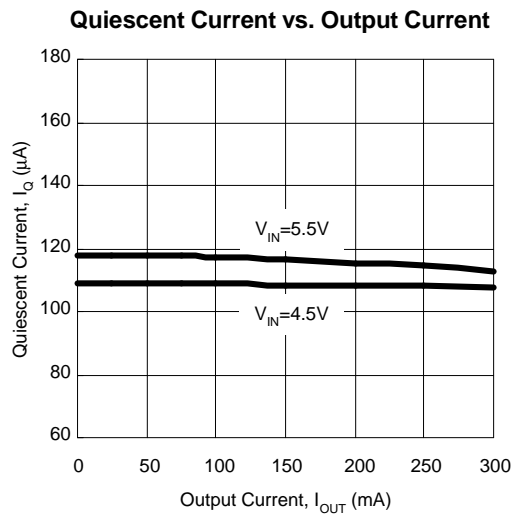
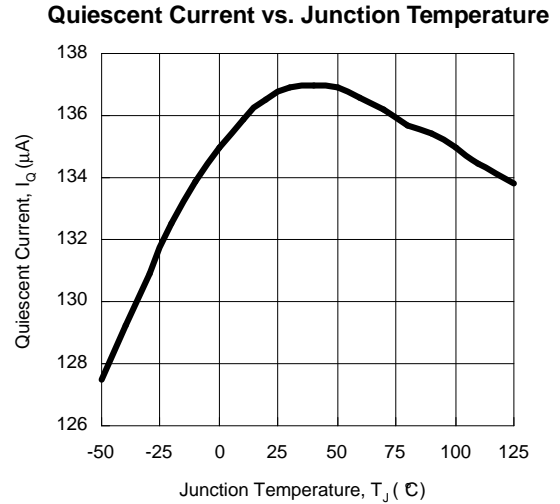
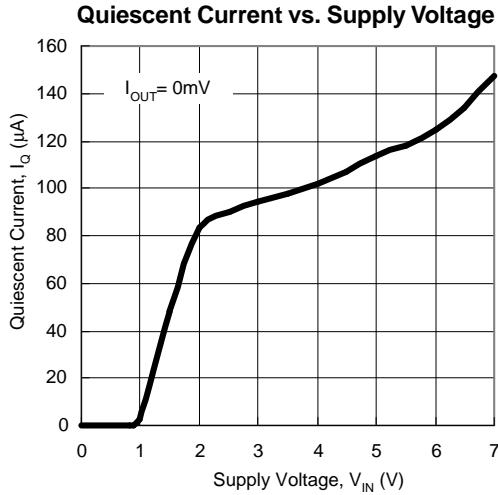
Symbol	Parameter	Range	Unit
$V_{IN}$	VIN Supply Voltage	2.8 ~ 6	V
$V_{OUT}$	Output Voltage	0.8 ~ 5.5	V
$I_{OUT}$	VOUT Output Current	0 ~ 300	mA
$C_{IN}$	Input Capacitor	0.22 ~ 100	μF
$C_{OUT}$	Output Capacitor	1.5 ~ 33	μF
$T_J$	Junction Temperature	-40 ~ 125	°C

## Electrical Characteristics

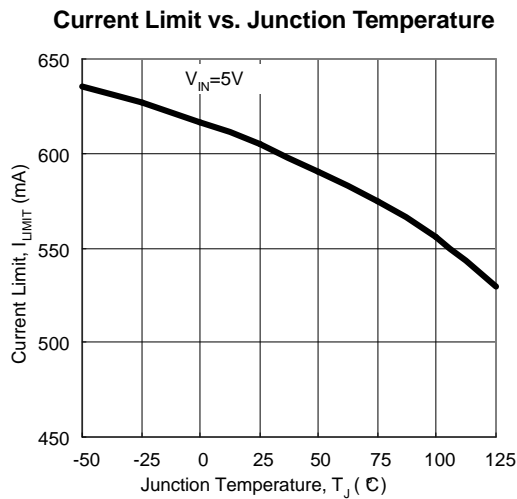
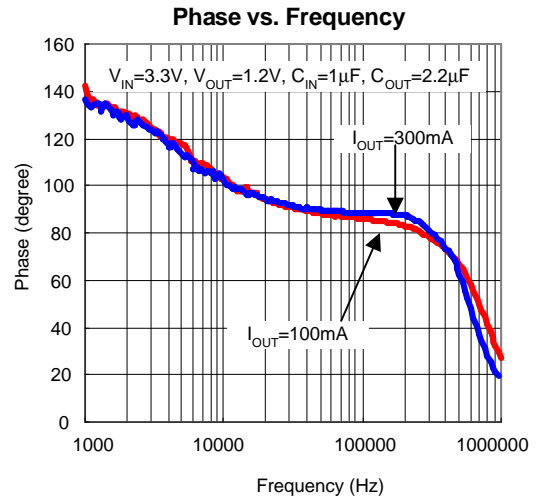
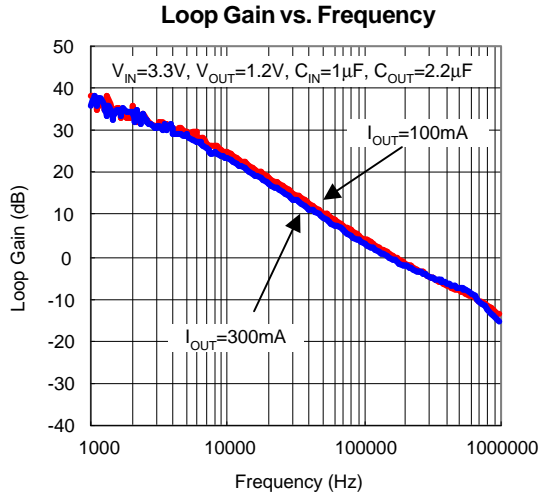
Unless otherwise specified, these specifications apply over  $V_{IN} = V_{OUT} + 1V$  (min  $V_{IN} = 2.8V$ ),  $I_{OUT} = 0 \sim 300mA$ ,  $C_{IN} = 1\mu F$ ,  $C_{OUT} = 2.2\mu F$ ,  $T_A = -40$  to  $85^\circ C$ . Typical values are at  $T_A = 25^\circ C$ .

Symbol	Parameter	Test Conditions	APL5315			Unit
			Min.	Typ.	Max.	
$V_{IN}$	Input Voltage		2.8	-	6	V
$V_{OUT}$	Output Voltage Range		0.8	-	5.5	V
$I_Q$	Quiescent Current	$I_{OUT} = 10mA \sim 300mA$	-	135	160	$\mu A$
$V_{REF}$	Reference Voltage	Measured on SET, $V_{IN} = 2.8V$ , $I_{OUT} = 10mA$	-	0.8	-	V
	Output Voltage Accuracy	$T_A = 25^\circ C$ , $I_{OUT} = 10mA$	-1	-	+1	%
	Output Voltage Accuracy	$T_A = -40^\circ C \sim 85^\circ C$ , $I_{OUT} = 10mA$	-2	-	+2	%
REG <sub>LINE</sub>	Line Regulation	$\Delta V_{OUT} \% / \Delta V_{IN}$ , $I_{OUT} = 10mA$	-0.06	-	+0.06	%/V
REG <sub>LOAD</sub>	Load Regulation	$\Delta V_{OUT} \% / \Delta I_{OUT}$	-0.2	-	+0.2	%/A
$V_{DROP}$	Dropout Voltage	$V_{OUT} = 2.5V$ , $I_{OUT} = 300mA$	-	230	360	mV
		$V_{OUT} = 3.3V$ , $I_{OUT} = 300mA$	-	170	300	
PSRR	Power Supply Ripple Rejection Ratio	$f = 10kHz$ , $I_{OUT} = 300mA$	-	45	-	dB
		Noise	$f = 80Hz$ to $100kHz$ , $I_{OUT} = 300mA$	-	160	
$I_{LIMIT}$	Current Limit		450	600	-	mA
$I_{SHORT}$	Foldback Current	$V_{OUT} = 0V$	-	80	-	mA
	$\overline{SHDN}$ Input Voltage High		1.6	-	-	V
	$\overline{SHDN}$ Input Voltage Low		-	-	0.4	
	Shutdown VIN Supply Current	$\overline{SHDN} = Low$ , $V_{IN} = 6V$	-	0.1	1	$\mu A$
	$\overline{SHDN}$ Pull Low Resistance		-	3	-	$m\Omega$
	$V_{OUT}$ Discharge MOSFET $R_{DS(ON)}$	$\overline{SHDN} = Low$	-	60	-	$\Omega$
	Over Temperature Threshold		-	160	-	$^\circ C$
	Over Temperature Hysteresis		-	40	-	$^\circ C$
	SET Input Threshold for Fixed/Adjustable Output Voltage Mode		-	100	-	mV
	SET Input Bias Current	$V_{SET} = 0.8V$	-100	-	100	nA
$T_{SS}$	Soft-Start Interval		-	60	-	$\mu s$

Typical Operating Characteristics

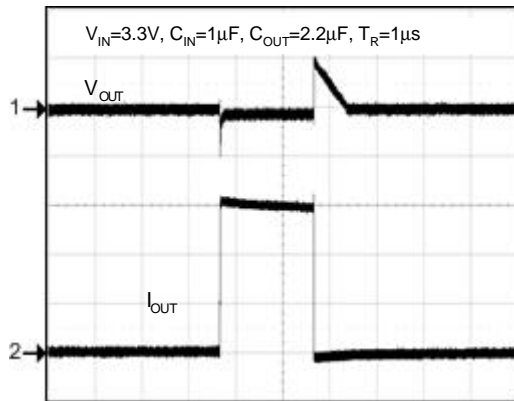


Typical Operating Characteristics (Cont.)



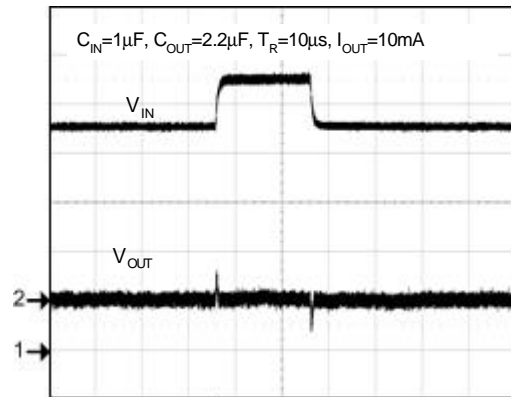
Operating Waveforms

Load Transient



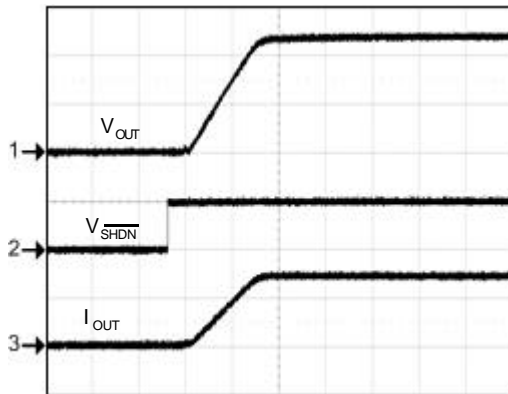
CH1 :  $V_{OUT}$ , 50mV/div, AC  
 CH2 :  $I_{OUT}$ , 100mA/div, DC  
 Time : 100μs/div

Line Transient



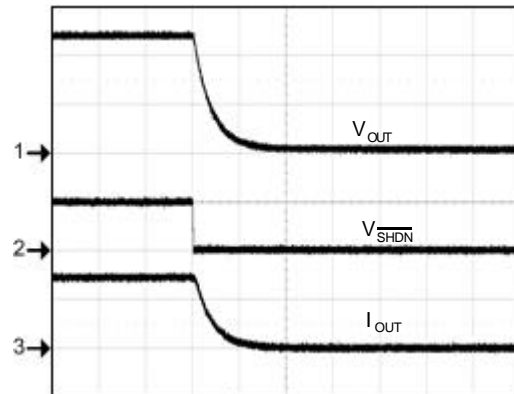
CH1 :  $V_{IN}$ , 1V/div, DC  
 CH2 :  $V_{OUT}$ , 20mV/div, AC  
 Time : 100μs/div

Enable



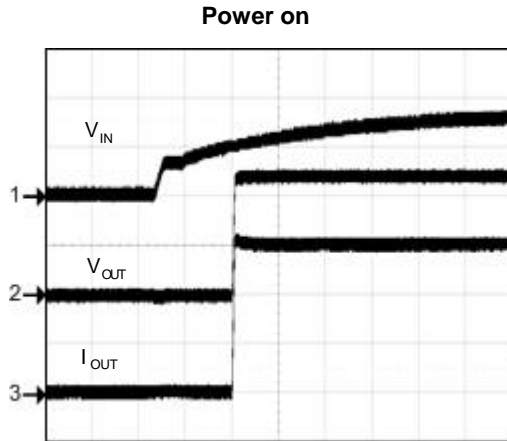
CH1 :  $V_{OUT}$ , 500mV/div  
 CH2 :  $V_{SHDN}$ , 5V/div  
 CH3 :  $I_{OUT}$ , 200mA/div  
 Time : 50μs/div

Shutdown

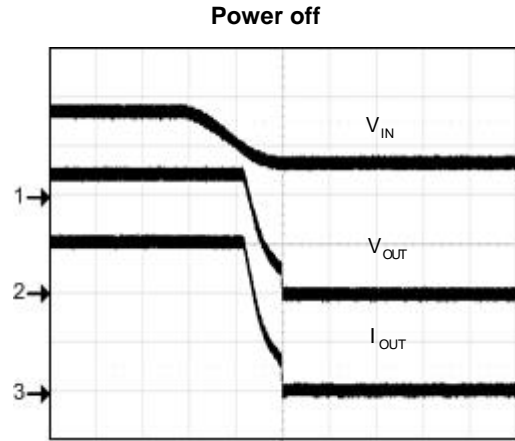


CH1 :  $V_{OUT}$ , 500mV/Div  
 CH2 :  $V_{SHDN}$ , 5V/Div  
 CH3 :  $I_{OUT}$ , 200mA/Div DC  
 Time : 10μs/Div

Operating Waveforms (Cont.)



CH1 : V<sub>IN</sub>, 2V/div  
 CH2 : V<sub>OUT</sub>, 500mV/div  
 CH3 : I<sub>OUT</sub>, 100mA/div  
 Time : 200µs/Div

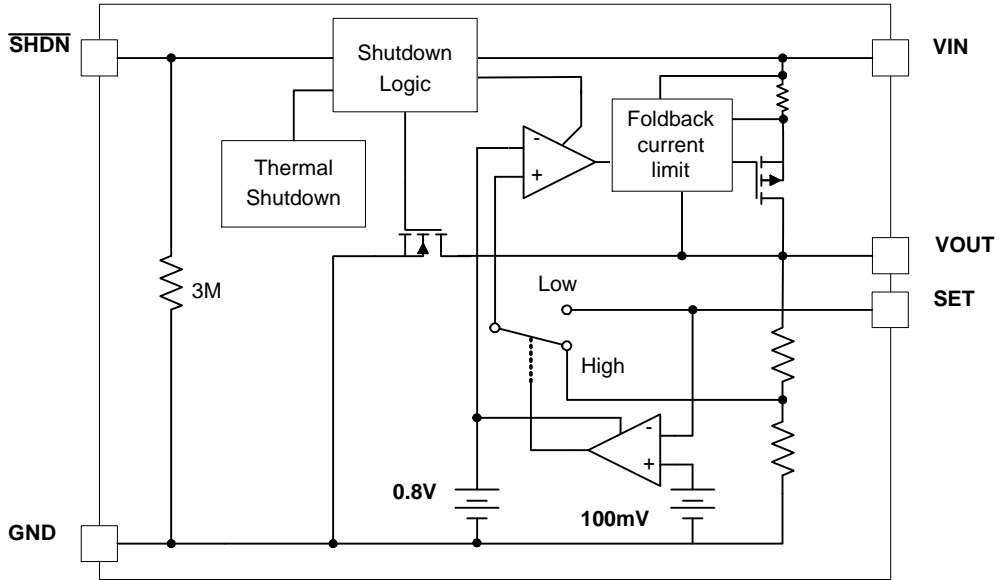


CH1 : V<sub>IN</sub>, 2V/div  
 CH2 : V<sub>OUT</sub>, 500mV/div,  
 CH3 : I<sub>OUT</sub>, 100mA/div  
 Time : 50ms/Div

Pin Description

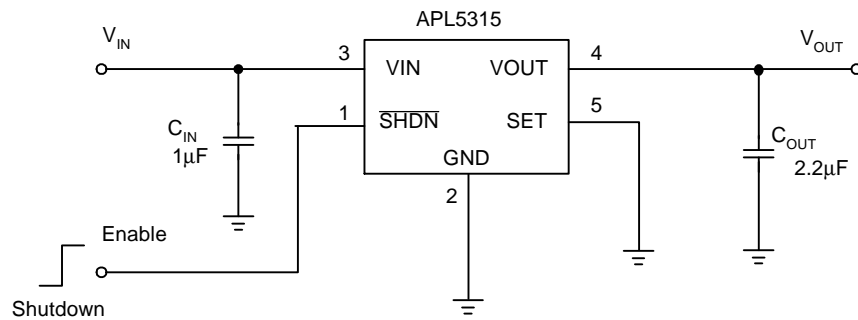
PIN		FUNCTION
No	NAME	
1	SHDN	Shutdown control pin, logic high: enable; logic low: shutdown
2	GND	Ground pin
3	VIN	Voltage supply input pin
4	VOU	Regulator output pin
5	SET	Connect this pin to ground for fixed output voltage operation. Connect this pin to an external resistor divider for adjustable output voltage mode operation.

Block Diagram



Typical Application Circuits

1. Fixed Output Voltage Mode

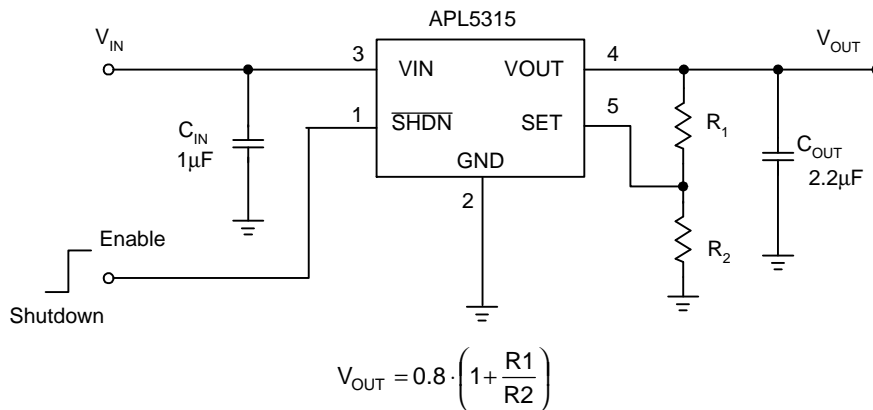


2.2µF/GRM155R60J225M Murata



## Typical Application Circuits (Cont.)

### 2. Adjustable Output Voltage Mode



## Function Description

### Internal Soft-Start

An internal soft-start function controls rising rate of the output voltage to limit the surge current at start-up. The typical soft-start interval is about 80µs.

### Output Voltage Regulation

The APL5315 can work in either fixed or adjustable mode by connecting the SET to GND or a resistor-divider which receives the feedback voltage of the regulator. The output voltage set by the resistor-divider is determined by:

$$V_{OUT} = 0.8 \cdot \left( 1 + \frac{R_1}{R_2} \right)$$

Where R1 is connected from VOUT to SET with Kelvin sensing and R2 is connected from SET to GND. The recommended value of R2 is in the range of 100~100kΩ. An error amplifier working with a temperature compensated 0.8V reference and an output PMOS regulates the output to the presetting voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output PMOS which provides load current from VIN to VOUT.

### Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APL5315. When the junction temperature exceeds +160°C, a thermal sensor turns off the output PMOS,

allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature is cooled down by 40°C. The thermal shutdown designed with a 40°C hysteresis lowers the average junction temperature during continuous thermal overload conditions, extending lifetime of the device.

For normal operation, device power dissipation should be externally limited so that junction temperature will not exceed 125°C.

### Shutdown Control

The APL5315 has an active-low shutdown function. Force  $\overline{\text{SHDN}}$  high (>1.6V) enables the  $V_{OUT}$ ; force  $\overline{\text{SHDN}}$  low (<0.4V) disables the  $V_{OUT}$ .  $\overline{\text{SHDN}}$  is internally pulled low by a resistor (3mΩ typical). If it is not used, connect to VIN for normal operation.

## Application Information

### Input Capacitor

The APL5315 requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN limit the slew rate of the surge current, place the Input capacitors near VIN as close as possible. Input capacitors should be larger than 1μF and a minimum ceramic capacitor of 1μF is necessary.

### Output Capacitor

The APL5315 needs a proper output capacitor to maintain circuit stability and to improve transient response over temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 2.2μF. With X5R and X7R dielectrics, 2.2μF is sufficient at all operating temperatures. Large output capacitor value can reduce noise and improve load-transient response and PSRR, however, it also affects power on issue. Equation (1) shows the relationship between the maximum C<sub>OUT</sub> value and V<sub>OUT</sub>.

$$C_{OUT(max)} = 31 - \frac{6}{V_{OUT}} \dots\dots\dots(1)$$

Where the unit of C<sub>OUT</sub> is μF and V<sub>OUT</sub> is V. Figure 1 shows the curve of maximum output capacitor over the output voltage. The output voltage range is from 0.8 to 5.5V and the output capacitor value should be under the line. Output capacitors must be placed at the load and ground pin as close as possible and the impedance of the layout must be minimized.

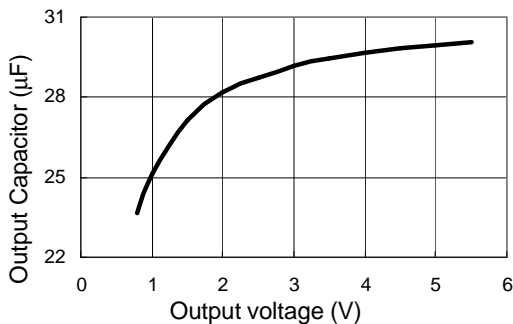


Figure 1

### Operation Region and Power dissipation

The APL5315 maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation P<sub>D</sub> across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T<sub>J</sub>-T<sub>A</sub>) is the temperature difference between the junction and ambient air. θ<sub>JA</sub> is the thermal resistance between Junction and ambient air. Assuming the T<sub>A</sub>=25°C and maximum T<sub>J</sub>=160°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)} = (160-25)/240 = 0.56(W)$$

For normal operation, do not exceed the maximum junction temperature rating of T<sub>J</sub> = 125 °C. The calculated power dissipation should less than:

$$P_D = (125-25)/240 = 0.41(W)$$

The GND provides an electrical connection to ground and channels heat away. Connect the GND to ground by using a large pad or ground plane.

### Layout Consideration

Figure 2 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN.
2. Ceramic capacitors for load must be placed near the load as close as possible.
3. To place APL5315 and output capacitors near the load is good for performance.
4. Large current paths, the bold lines in figure 2, must have wide tracks.
5. Divider resistor R1 and R2 must be placed near the SET as close as possible.

Application Information (Cont.)

Layout Consideration (Cont.)

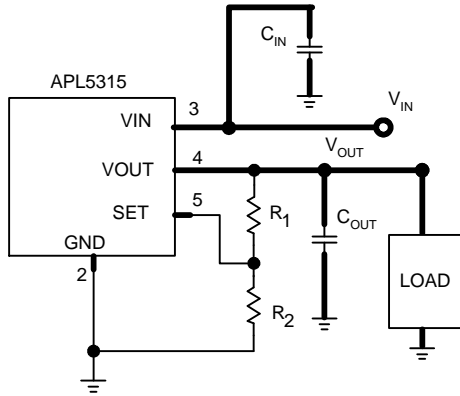
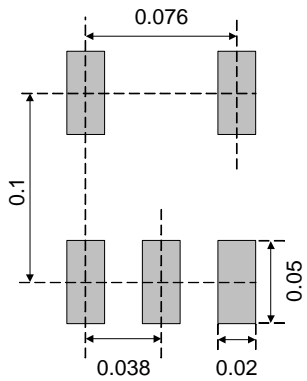


Figure 2

Recommended Minimum Footprint

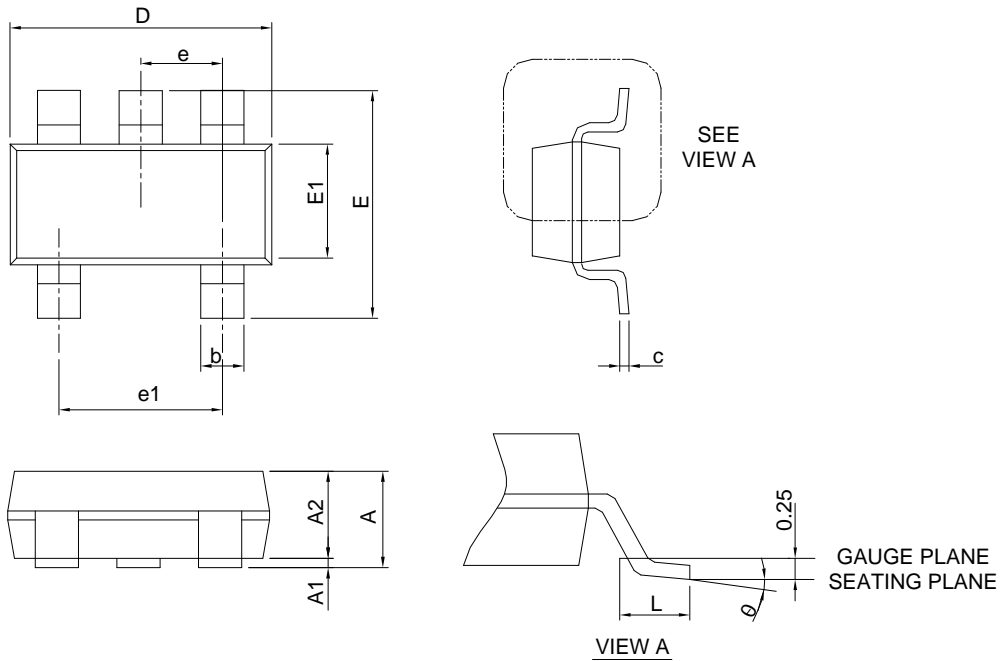
SOT-23-5



Unit : Inch

Package Information

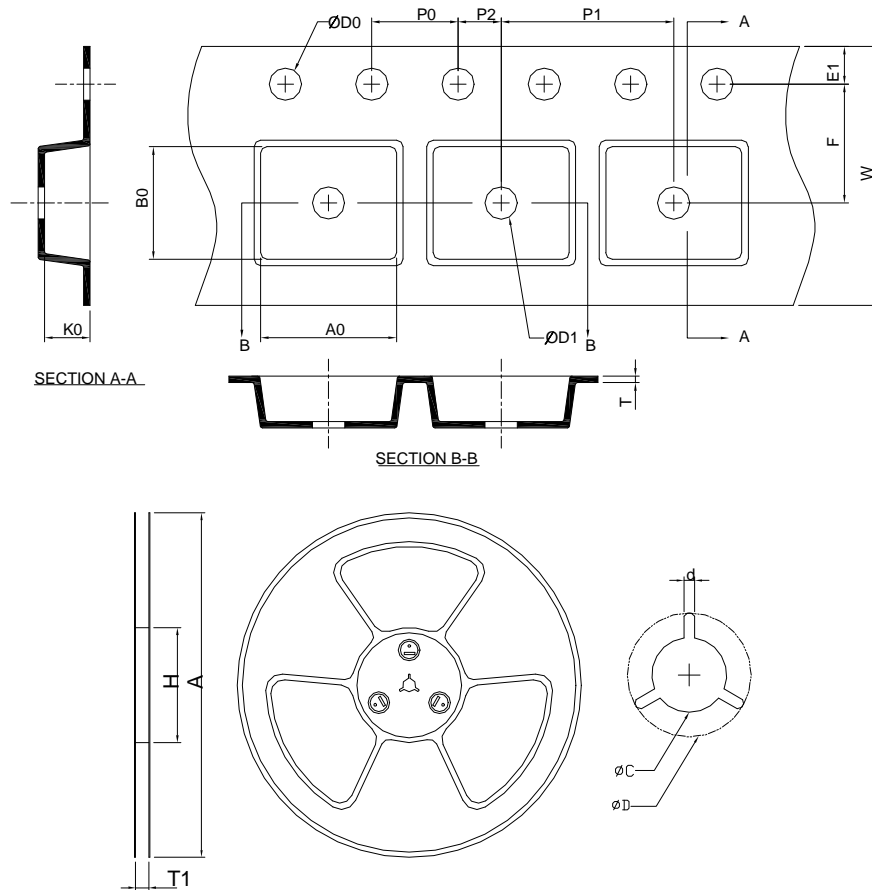
SOT-23-5



Symbol	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.016	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.  
 2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



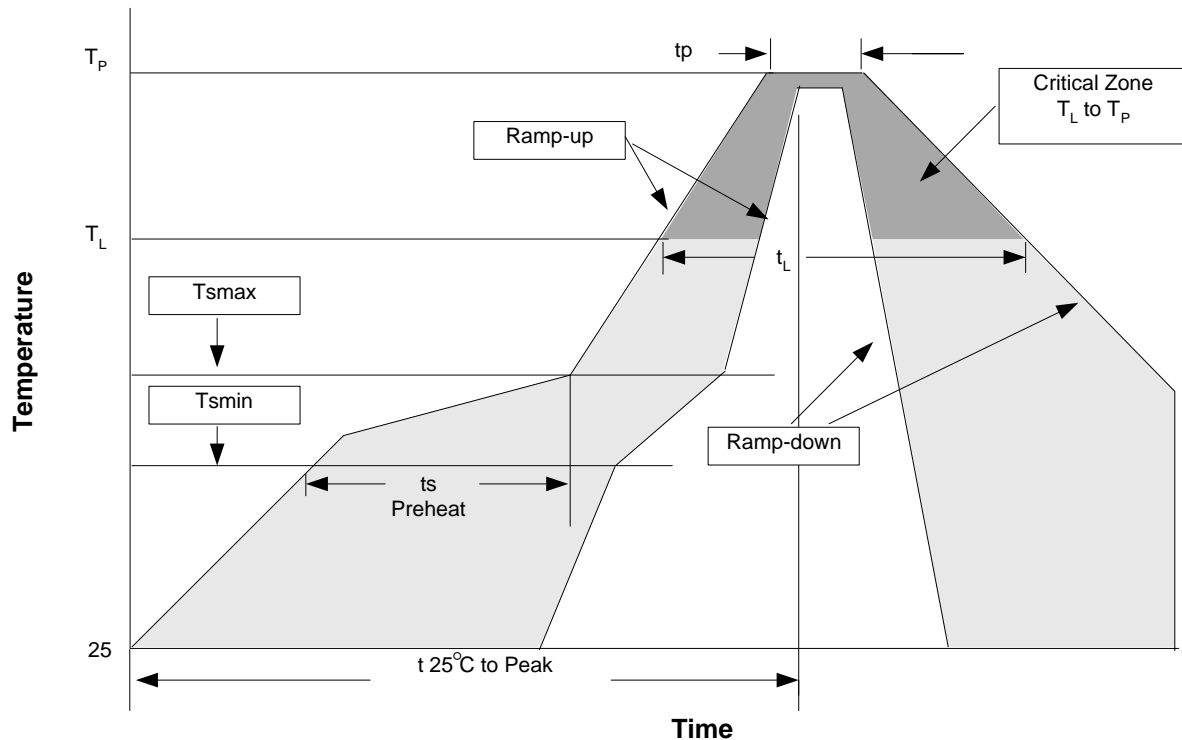
Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0 ±0.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0 ±0.30	1.75 ±0.10	3.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	4.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20 ±0.20	3.10 ±0.20	1.50 ±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOT-23-5	Tape & Reel	3000

**Reflow Condition (IR/Convection or VPR Reflow)**



**Reliability Test Program**

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1 <sub>tr</sub> > 100mA

**Classification Reflow Profiles**

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T <sub>L</sub> to T <sub>P</sub> )	3°C/second max.	3°C/second max.
Preheat		
- Temperature Min (T <sub>smmin</sub> )	100°C	150°C
- Temperature Max (T <sub>smmax</sub> )	150°C	200°C
- Time (min to max) (t <sub>s</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
- Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak/Classification Temperature (T <sub>p</sub> )	See table 1	See table 2
Time within 5°C of actual Peak Temperature (t <sub>p</sub> )	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

**Classification Reflow Profiles (Cont.)**

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

\* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

**Customer Service**

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