



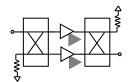
Internally Matched Balanced LNA Module Including Coupler

Features

- · S₂₁ = 13.5 dB@1760 MHz
 - = 12.5 dB@3000 MHz
- · NF of 1.6 dB over Frequency
- · Unconditionally Stable
- · Single 5 V Supply
- · High OIP3@Low Current
- · 1-stage Balanced Type







1-stage Balanced Type

Specifications (in Production)

Typ.@T = 25 °C, V_s = 5 V, Freq. = 2380 MHz, $Z_{o.sys}$ = 50 ohms

Parameter	Unit	Specifications		
	Offit	Min	Тур	Max
Frequency Range	MHz	1760		3000
Gain	dB	12.0	13.0	
Gain Flatness	dB		±0.5	±0.6
Noise Figure	dB		1.6	1.7
Output IP3 (1)	dBm	30	31	
S11/S22 (2)	dB			-11/-9
Output P1dB	dBm	18	19	
Switching Time (3)	μsec		-	
Supply Current	mA		180	200
Supply Voltage	V	5		
Impedance	Ω	50		
Max. RF Input Power	dBm	C.W 29~31(before fail)		
Package Type & Size	mm	Surface Mount Type, 16Wx13Lx5H		

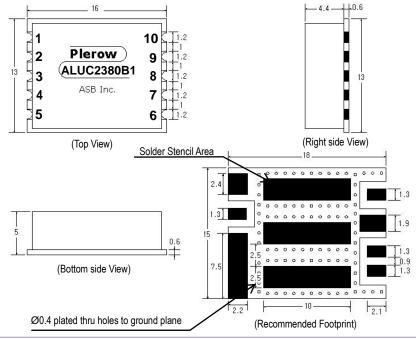
More Information

Website: www.asb.co.kr E-mail: sales@asb.co.kr Tel: (82) 42-528-7223 Fax: (82) 42-528-7222

Operating temperature is -40 °C to +85 °C.

- 1) OIP3 is measured with two tones at an output power of +4 dBm/tone separated by 1 MHz.
- Stift.252(max) is the worst value within the frequency band.
 Switching time means the time that takes for output power to get stabilized to its final level after switching DC voltage from 0 V to Vs.

Outline Drawing (Unit: mm)



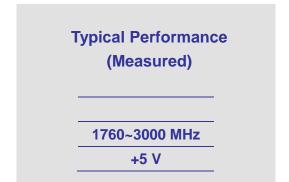
Port Number	Function		
2	RF In		
7	RF Out		
6, 10	Vs		
Others, Bottom	GND		

- Note: 1. The number and size of ground via holes in a circuit board is critical for thermal RF grounding considerations.
 - 2. We recommend that the ground via holes be placed on the bottom of all ground pins for better RF and thermal performance, as shown in the drawing at the left side.



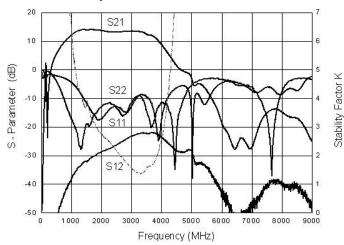


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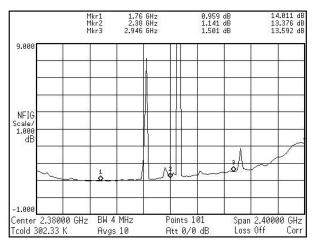


S-parameters 10 15 S21 0 13 S11, S22, S12 (dB) 12 -10 S11 S22 -20 S12 -30 -40 ┗ 1760 1915 2070 2380 2690 2845 Frequency (MHz)

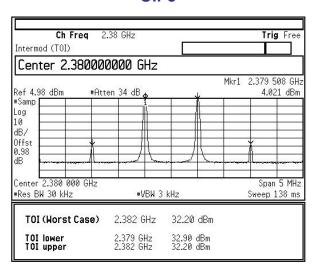
S-parameters & K Factor



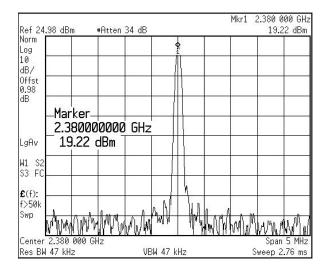
Noise Figure



OIP3



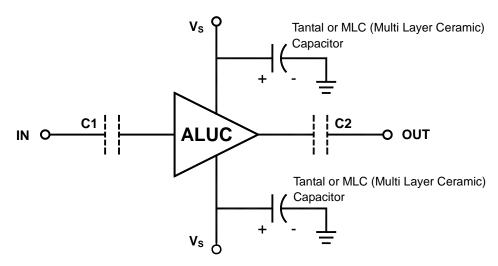
P₁dB





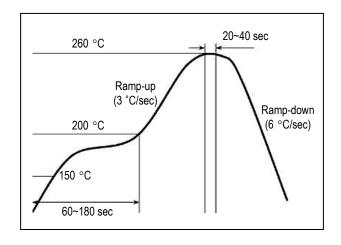
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Application Circuit

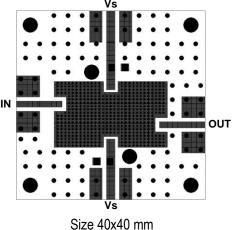


- The tantal or MLC (Multi Layer Ceramic) capacitor is optional and for bypassing the AC noise introduced from the DC supply. The capacitance value may be determined by customer's DC supply status. The capacitor should be placed as close as possible to V_s pin and be connected directly to the ground plane for the best electrical performance.
- 2) DC blocking capacitors are always necessarily placed at the input and output port for allowing only the RF signal to pass and blocking the DC component in the signal. The DC blocking capacitors are included inside the ALN module. Therefore, C1 & C2 capacitors may not be necessary, but can be added just in case that the customer wants. The value of C1 & C2 is determined by considering the application frequency.

Recommended Soldering Reflow Process



Evaluation Board Layout



(for ALUC Series – 22x12 mm)