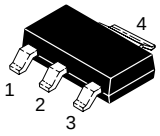
# PNP Silicon Transistor

**BF721T1**

**ON Semiconductors Preferred Device**

**PNP SILICON TRANSISTOR SURFACE MOUNT**




**CASE 318E-04, STYLE 1**
**SOT–223 (TO-261AA)**

### MAXIMUM RATINGS

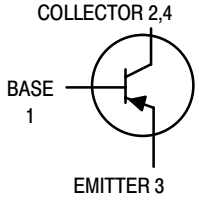
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector-Emitter Voltage | $V_{CEO}$ | –300 | Vdc |
| Collector-Base Voltage | $V_{CBO}$ | –300 | Vdc |
| Collector-Emitter Voltage | $V_{CER}$ | –300 | Vdc |
| Emitter-Base Voltage | $V_{EBO}$ | –5.0 | Vdc |
| Collector Current | $I_C$ | –100 | mAdc |
| Total Power Dissipation up to $T_A$ = 25°C(1) | $P_D$ | 1.5 | Watts |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |
| Junction Temperature | $T_J$ | 150 | °C |

### DEVICE MARKING

DF

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance from Junction to Ambient(1) | $R_{\theta JA}$ | 83.3 | °C/W |




### ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | |
| Collector-Emitter Breakdown Voltage ($I_C$ = –1.0 mAdc, $I_B$ = 0) | $V_{(BR)CEO}$ | –300 | — | Vdc |
| Collector-Base Breakdown Voltage ($I_C$ = –100 μAdc, $I_E$ = 0) | $V_{(BR)CBO}$ | –300 | — | Vdc |
| Collector-Emitter Breakdown Voltage ($I_C$ = –100 μAdc, $R_{BE}$ = 2.7 kΩ) | $V_{(BR)CER}$ | –300 | — | Vdc |
| Emitter-Base Breakdown Voltage ($I_E$ = –10 μAdc, $I_C$ = 0) | $V_{(BR)EBO}$ | –5.0 | — | Vdc |
| Collector-Base Cutoff Current ($V_{CB}$ = –200 Vdc, $I_E$ = 0) | $I_{CBO}$ | — | –10 | nAdc |
| Collector–Emitter Cutoff Current<br>($V_{CE}$ = –250 Vdc, $R_{BE}$ = 2.7 kΩ)<br>($V_{CE}$ = –200 Vdc, $R_{BE}$ = 2.7 kΩ, $T_J$ = 150°C) | $I_{CER}$ | <br>—<br>— | <br>–50<br>–10 | <br>nAdc<br>μAdc |

1. Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 $in^2$.

**Preferred** devices are ON Semiconductors recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Continued)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **ON CHARACTERISTICS** | | | | |
| DC Current Gain ($V_{CE}$ = –25 mAdc, $V_{CE}$ = –20 Vdc) | $h_{FE}$ | 50 | — | — |
| Collector-Emitter Saturation Voltage ($I_C$ = –30 mAdc, $I_B$ = –5.0 mAdc) | $V_{CE(sat)}$ | — | –0.8 | Vdc |
| **DYNAMIC CHARACTERISTICS** | | | | |
| Current-Gain — Bandwidth Product ($V_{CE}$ = –10 Vdc, $I_C$ = –10 mAdc, f = 35 MHz) | $f_T$ | 60 | — | MHz |
| Feedback Capacitance ($V_{CE}$ = –30 Vdc, $I_C$ = 0, f = 1.0 MHz) | $C_{re}$ | — | 1.6 | pF |

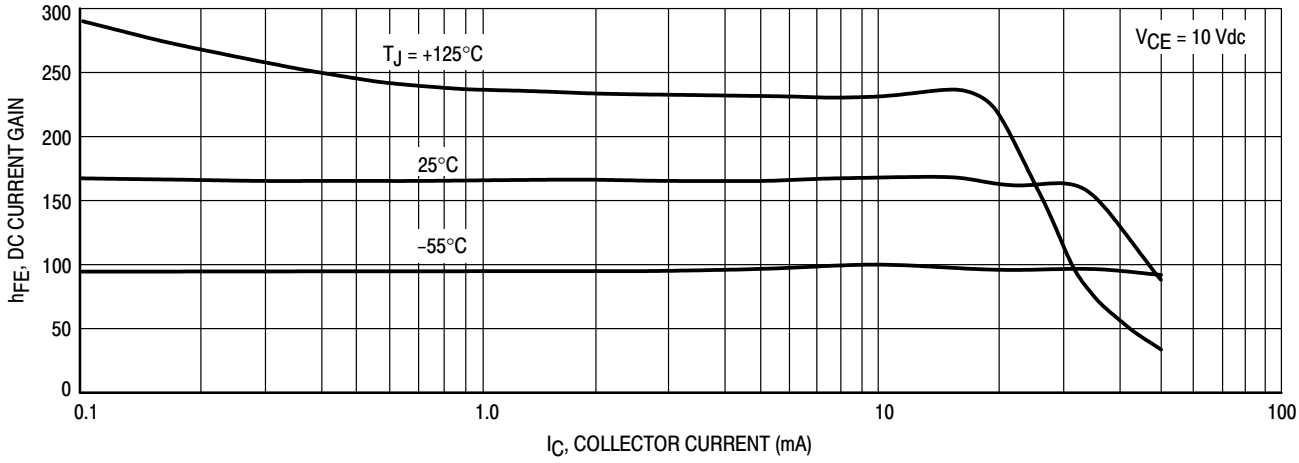



**Figure 1. DC Current Gain**

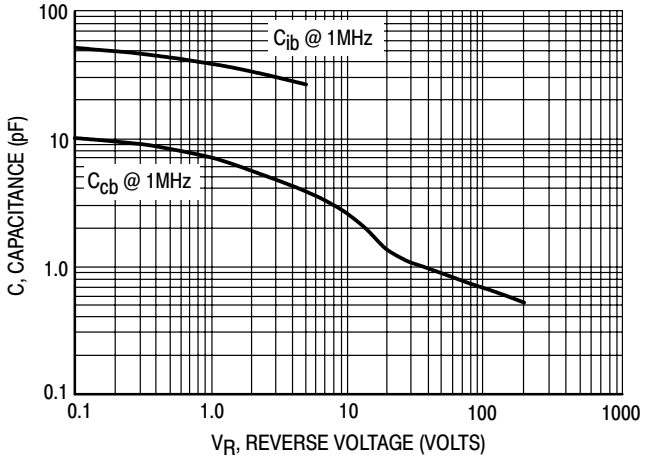



**Figure 2. Capacitance**

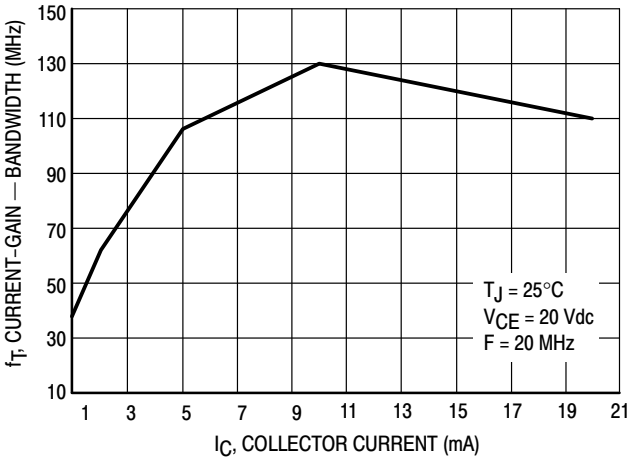
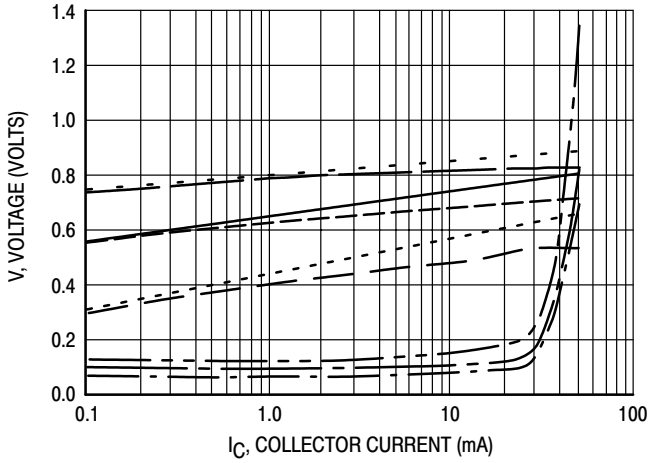



**Figure 3. Current–Gain — Bandwidth**



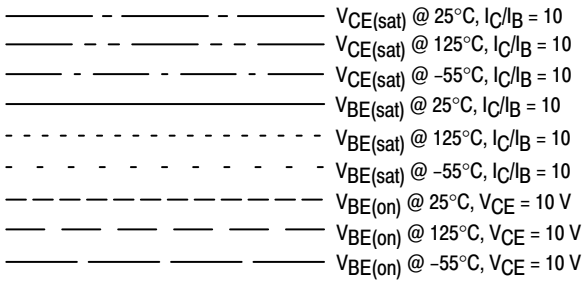
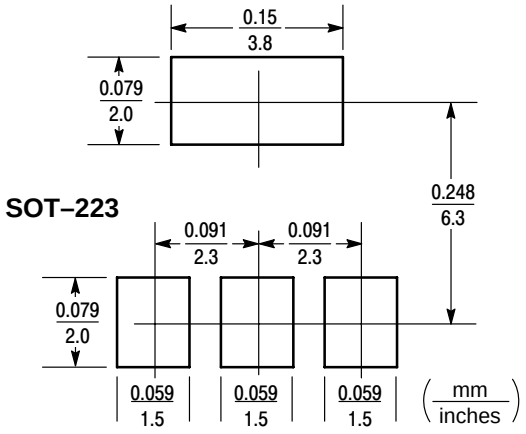




**Figure 4. “ON” Voltages**

# INFORMATION FOR USING THE SOT–223 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–223 POWER DISSIPATION

The power dissipation of the SOT–223 is a function of the pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R\theta_{JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–223 package, $P_D$ can be calculated as follows.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 1.5 watts.

$$P_D = \frac{150°C - 25°C}{83.3°C/W} = 1.50 \text{ watts}$$

The 83.3°C/W for the SOT-223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.5 watts. There are other alternatives to achieving higher power dissipation from the SOT-223 package. One is to increase the area of the collector pad. By increasing the area of the collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. A graph of $R_{\theta JA}$ versus collector pad area is shown in Figure 5.

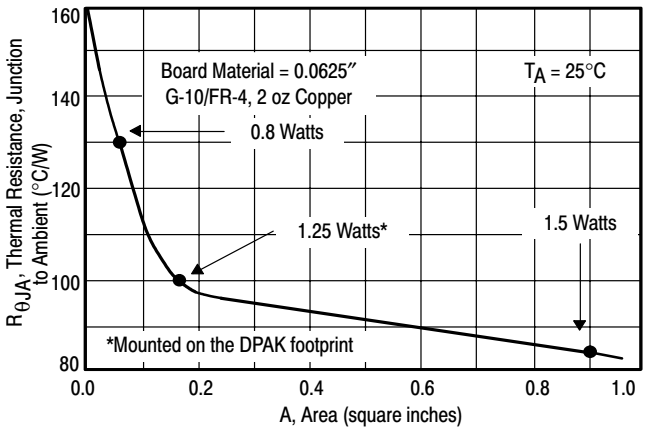



**Figure 5. Thermal Resistance versus Collector Pad Area for the SOT-223 Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches.

The stencil opening size for the surface mounted package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 7 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

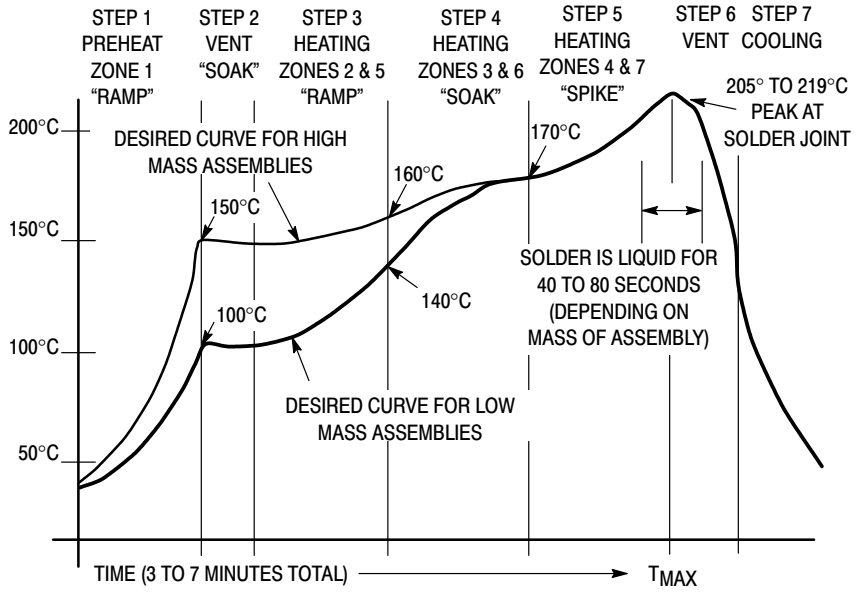
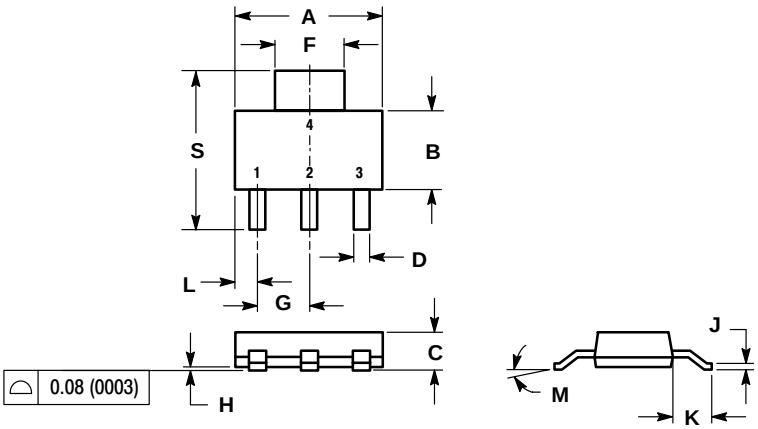



**Figure 6. Typical Solder Heating Profile**

## PACKAGE DIMENSIONS

**CASE 318E−04**
**ISSUE H**
**TO-261AA**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.249 | 0.263 | 6.30 | 6.70 |
| B | 0.130 | 0.145 | 3.30 | 3.70 |
| C | 0.060 | 0.068 | 1.50 | 1.75 |
| D | 0.024 | 0.035 | 0.60 | 0.89 |
| F | 0.115 | 0.126 | 2.90 | 3.20 |
| G | 0.087 | 0.094 | 2.20 | 2.40 |
| H | 0.0008 | 0.0040 | 0.020 | 0.100 |
| J | 0.009 | 0.014 | 0.24 | 0.35 |
| K | 0.060 | 0.078 | 1.50 | 2.00 |
| L | 0.033 | 0.041 | 0.85 | 1.05 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| S | 0.264 | 0.287 | 6.70 | 7.30 |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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