ANALOG DEVICES

CMOS 4½/5½ Digit ADC Subsystem

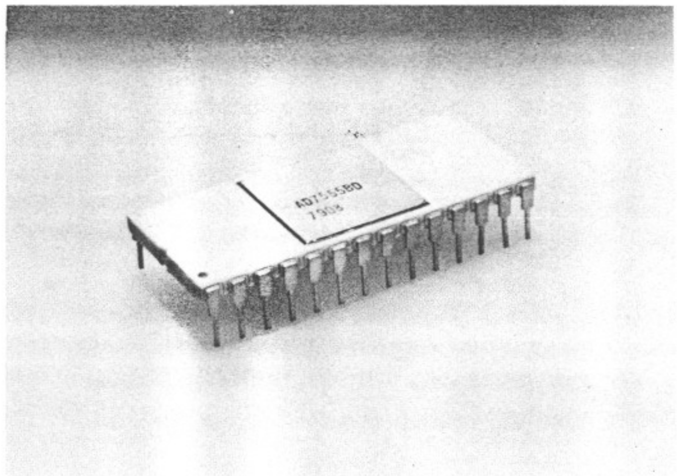
AD7555

PRELIMINARY TECHNICAL DATA

OBSOLETE

FEATURES

- Resolution: ±4 1/2 Digits BCD or ±20k Count Binary Capability for 5 1/2 Digit Resolution or Custom Data Formats
- Data Format: Multiplexed BCD (for Display) and Serial Count (for External Linearization, Data Reformatting, or Microprocessor Interface)
- Accuracy: ±1 Count in ±20k Counts
- Scale Factor Drift: 0.2ppm/°C Using Only Medium-Precision Op Amps
- Requires only a Single Positive Reference
- Overrange Display
- Auto Calibration Capability
- Interfaces to TTL or 5V CMOS
- $\overline{HOLD}$ Input and SCC (System Conversion Complete) Output for Interface Flexibility

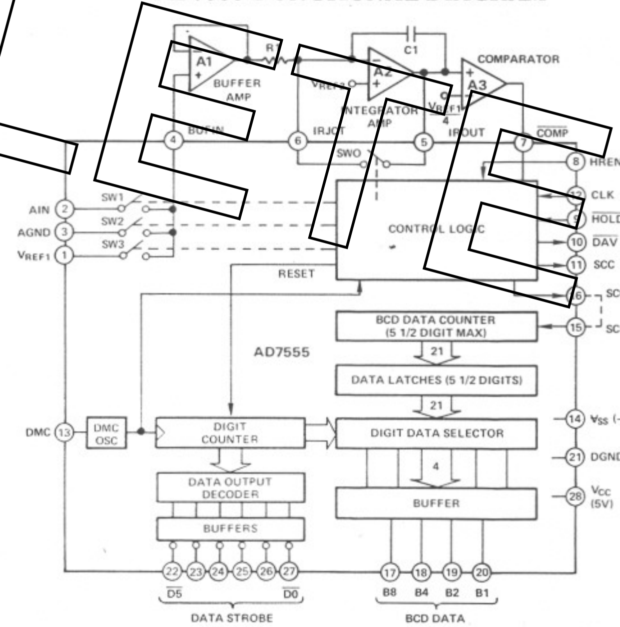


GENERAL DESCRIPTION

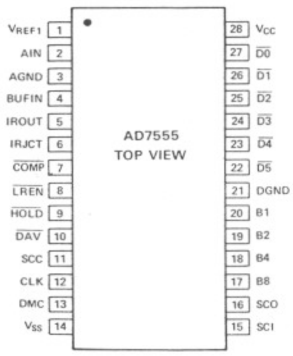
The AD7555 is a 4 1/2 digit, monolithic CMOS, quad slope integrating ADC subsystem designed for display or microprocessor interface applications. Use of the high resolution enable input expands the display format to 5 1/2 digits BCD. With SCO (Serial Count Out) connected to SCI (Serial Count In), the output data format is multiplexed BCD suitable for visual display purposes. As an added feature, SCO can also be used with rate multipliers for linearization, or with BCD or binary counters for data reformatting (up to 200k binary counts).

The quad slope conversion algorithm (Analog Devices patent No. 3872466) converts the external amplifier's input drift errors to a digital number and subsequently reduces the total system drift error to a second order effect. Using only inexpensive, medium-precision amplifiers a scale factor drift of 0.2ppm/°C is achieved.

AD7555 FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

Model	Package	Operating Temperature Range
AD7555BD	28 Pin Side Brazed Ceramic	–25°C to +85°C
AD7555KN	28 Pin Molded Plastic	0 to +70°C

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 714/842-1717
Mid-West 312/894-3300
Texas 214/231-5094

SPECIFICATIONS (V_{CC} = +5V, V_{SS} = –5V, V_{REF1} = +4.0960V, F_{CLK} = 614.4kHz, AGND = 0V)

PARAMETER	LIMIT AT T_A = +25°C	LIMIT AT T_A = T_{min}, T_{max}	UNITS	CONDITIONS/COMMENTS
ANALOG SWITCHES				
R_{ON} (Switch 1-3)	800	1200	Ω max	–2V ≤ AIN ≤ +2V Refer to Functional Diagram
ΔR_{ON} (Switch 1) versus AIN	300	500	Ω typ	–2V ≤ AIN ≤ +2V
Mismatch Between Any Two Switches (excluding SW0)	300	500	Ω typ	–2V ≤ AIN ≤ +2V
I_{LKG} (Switch OFF)				
SW0 (pin 6)	1	70	nA max	IRJCT (pin 5) = +2.048V 0V ≤ IROUT (pin 5) ≤ +10V
SW1 (pin 2)	1	70	nA typ	AIN = +2V to –2V, BUFIN = 0V and +4.096V
SW2 (pin 3)	1	70	nA typ	AGND = 0V, BUFIN = –2V to +2V, +4.096V
SW3 (pin 1)	1	70	nA typ	V_{REF1} = +4.096V, BUFIN = –2V to +2V
I_{LKG} (BUFIN, pin 4)	3	200	nA typ	Any 1 of SW1, 2, 3 on
CONTROL INPUTS (pins 7, 8, 9, 15)				
V_{INH}	3.0	3.0	V min	
V_{INL}	0.8	0.8	V max	
I_{INH} or I_{INL}	1	10	μA max	V_{IN} = 0V or V_{CC}
CLOCK INPUTS (pin 12 and 13)				
V_{INH} (CLK)	3.5	3.5	V min	
V_{INL} (CLK)	0.8	0.8	V max	
V_{INH} (DMC)	3.0	3.0	V min	
V_{INL} (DMC)	0.8	0.8	V max	
I_{INH} (CLK)	1.0	1.5	mA max	
I_{INL} (CLK)	–1.0	–1.5	mA max	
I_{INH} (DMC)	200	300	μA max	
I_{INL} (DMC)	–100	–150	μA max	
DIGITAL OUTPUTS				
$\overline{D0}$ – $\overline{D5}$ (pins 22-27)				
V_{OH}	4.5	4.5	V min	I_{SOURCE} = 40μA
V_{OL}	4.0	4.0	V max	I_{SINK} = 5mA (Display Driver Load)
V_{OL}	0.5	0.8	V max	I_{SINK} = 1.6mA (TTL Load)
B1, B2, B4, B8, $\overline{DAV}$, SCC, SCO (pins 20, 19, 18, 17, 10, 11, 16)				
V_{OH}	4.0	4.0	V min	I_{SOURCE} = 40μA
V_{OL}	0.5	0.8	V max	I_{SINK} = 1.6mA
DYNAMIC PERFORMANCE				
DMC Pulse Width	5	5	μs min	See Figure 3
DMC Frequency	100	100	kHz max	Typical f_{DMC} is 1.5kHz with C_{DMC} = 0.01μF
CLK Frequency	1.5	1.5	MHz max	
Propagation Delays				
DMC HIGH to $\overline{DAV}$ HIGH	5	7	μs max	See Figure 3
DMC HIGH to $\overline{DAV}$ LOW	5	7	μs max	
DMC HIGH to BCD Data on B8, B4, B2, B1	5	5	μs max	
DMC LOW to Digit Strobe (D0 – D5) LOW	5	5	μs max	
POWER SUPPLY				
I_{CC}	5	5	mA max	During Conversion
I_{SS}	5	5	mA max	During Conversion
V_{CC} Range	+5 to +17	+5 to +17	V	See Absolute Maximum Ratings
V_{SS} Range	–5 to –17	–5 to –17	V	

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

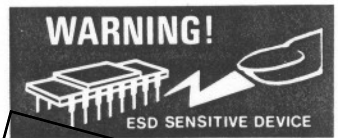
V_{CC} to DGND . . . . +17V
V_{SS} to DGND. . . . . –17V
V_{CC} to V_{SS} . . . . +22V
Digital Outputs . . . . V_{CC}, DGND
Digital Inputs
  DMC (Pin 13), CLK (Pin 12) . . . . V_{SS}, V_{CC}
  All other Logic Inputs . . . . DGND, +17V
Analog Inputs/Outputs
AGND to DGND (Positive Limitation) . . . . V_{CC} or V_{IROUT}*
AGND to DGND (Negative Limitation). V_{SS} or V_{IROUT} –20V†
  AIN (Pin 2), V_{REF1} (Pin 1),
    BUFIN (Pin 4) . . . . V_{CC}, V_{SS}
    IRJCT (Pin 6), IROUT (Pin 5). . . . . +27V, AGND
Operating Temperature Range
  AD7555KN (Plastic) . . . . 0 to +70°C
  AD7555BD (Ceramic) . . . . –25°C to +85°C
Storage Temperature . . . . –65°C to +150°C
Lead Temperature (Soldering, 10s). . . . . +300°C

Power Dissipation (package)
  Plastic (AD7555KN)
    To +50°C. 1200mW
    Derate above +50°C by. . . . . 12mW/°C
  Ceramic (AD7555BD)
    To +50°C. 1000mW
    Derate above +50°C by. . . . . 10mW/°C

*Whichever is the least positive.
†Whichever is the least negative.

NOTE:
Do not apply voltages to any AD7555 digital output, AIN or V_{REF1} before V_{CC} and V_{SS} are applied. Additionally, the voltages at AIN, V_{REF1} or any digital output must never exceed V_{CC} and V_{SS} (if an op amp output is used to drive AIN it must be powered by the AD7555 V_{CC} and V_{SS} supply voltages). Do not allow any digital input to swing below DGND.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.



SYSTEM ELECTRICAL CHARACTERISTICS (T_A = 0 to +45°C)
Characteristics refer to the system of Figures 6a and 6b. V_{CC} = +5V, V_{SS} = –5V, V_{REF1} = +4.096V, error count n calibrated to zero at T_A = +25°C as per procedure on page 9 unless otherwise noted. Switch leakages and limitations in temperature performance of auxiliary components (such as the integrating capacitor) cause performance degradations above +45°C.

CHARACTERISTIC	LIMIT	CONDITIONS/COMMENTS
Resolution	4 1/2 Digit BCD 5 1/2 Digit BCD	±20,000 Counts ±200,000 Counts (See Note 1)
Relative Accuracy	±1 Count max ±10 Count max	4 1/2 Digit BCD 5 1/2 Digit BCD (See Notes 1 and 2)
Count Uncertainty Due to Noise (Flicker)	±1/2 Count max ±2 Counts max	4 1/2 Digit BCD 5 1/2 Digit BCD (See Note 1)
Conversion Time	610ms max 1,760ms max	4 1/2 Digit BCD 5 1/2 Digit BCD (See Note 1)

NOTES:
[1] 4 1/2 digit mode; f_{CLK} = 614.4kHz, HREN = LOW, R_1 = 360kΩ
C_1 = 0.22μF
5 1/2 digit mode; f_{CLK} = 1.024MHz, HREN = HIGH, R_1 = 750kΩ
C_1 = 0.22μF
[2] Assumes voltage reference (V_{REF1}) TC of 0ppm/°C.

Applying the AD7555

AD7555 PIN DESCRIPTION

ANALOG FUNCTIONS

V_{REF1}	(Pin 1):	+4.096V Reference Input
AIN	(Pin 2):	Analog Input Voltage (±2V Full Scale)
AGND	(Pin 3):	Analog Signal Common Ground
BUFIN	(Pin 4):	To External Buffer Amplifier Input
IROUT	(Pin 5):	From Integrator Amplifier Output
IRJCT	(Pin 6):	To Integrator Amplifier Summing Junction

LOGIC INPUTS

$\overline{COMP}$	(Pin 7):	Input from the external comparator.
HREN	(Pin 8):	High Resolution Enable, determines converter resolution HREN = LOGIC LOW, Full Scale = ±1.9999V (100μV resolution) HREN = LOGIC HIGH, Full Scale = ±1.99999V (10μV resolution)
$\overline{HOLD}$	(Pin 9):	Hold Input $\overline{HOLD}$ = LOGIC HIGH, the ADC converts and updates the displays continuously as per the timing diagram of Figure 3. $\overline{HOLD}$ = LOGIC LOW, the ADC is reset and conversion is disabled. Data from the last complete conversion continues to be displayed. To ensure most recent data is displayed, $\overline{HOLD}$ should not be taken LOW when $\overline{DAV}$ is HIGH. When $\overline{HOLD}$ returns HIGH, the next leading edge of DMC initiates a new conversion.
DMC	(Pin 13):	Display Multiplexer Clock, can be driven from an external logic source, or with the addition of an external capacitor, will self oscillate. With an external capacitor of 10,000pF, DMC oscillates at approximately 1.5kHz at a 5% to 10% duty cycle, suitable for display purposes.
CLK	(Pin 12):	Clock Input for maximum line rejection in the 4 1/2 digit mode; 50Hz: f_{CLK} = 512kHz (= 4.096MHz ÷ 8) 60Hz: f_{CLK} = 614.4kHz (= 4.915MHz ÷ 8) 50/60Hz: f_{CLK} = 409.6kHz (= 3.2768MHz ÷ 8) For maximum line rejection in the 5 1/2 digit mode; 50/60Hz, f_{CLK} = 1.024MHz (= 4.096MHz ÷ 4)
SCI	(Pin 15):	Serial Count In. Input to totalizing counter in the AD7555. SCI is normally connected to SCO for direct count totalization.

SUPPLY INPUTS

V_{CC}	(Pin 28):	Positive Supply Input (+5V)
V_{SS}	(Pin 14):	Negative Supply Input (−5V)
DGND	(Pin 21):	Digital Ground

LOGIC OUTPUTS

B8 - B1	(Pins 17 - 20)	BCD8 - BCD1 output, Active HIGH (See table 1)
$\overline{D5}$	(Pin 22):	10^{-5} digit output, Active LOW in 5 1/2 digit mode, stays HIGH in 4 1/2 digit mode
$\overline{D4}$ - $\overline{D1}$	(Pins 23-27)	10^{-4} - 10^{-1} digit outputs, Active LOW
$\overline{D0}$	(Pin 27):	10^{0}/overflow/polarity output, Active LOW
SCC	(Pin 11):	System conversion complete, goes HIGH when conversion is complete, returns LOW on comparator crossing at end of phase 0 integration period.
SCO	(Pin 16):	Serial Count Out, a serial output pulse train proportional in length to the magnitude of AIN. SCO can be externally pulled HIGH while $\overline{DAV}$ = HIGH to display the error count "n" for calibration purposes (see page 9).
$\overline{DAV}$	(Pin 10):	Data Valid — When low, $\overline{DAV}$ indicates that the data being presented on the BCD output bus is valid. $\overline{DAV}$ goes high on the first positive edge of DMC after a conversion is complete and returns low two DMC pulses later. When it returns low, the digit counter is reset to D0. This is termed the MASTER RESET.

DATA		B8	B4	B2	B1	LED DISPLAY WHEN USING 7447 SEGMENT DECODER
0		0	0	0	0	0
1		0	0	0	1	1
2		0	0	1	0	2
3		0	0	1	1	3
4		0	1	0	0	4
5		0	1	0	1	5
6		0	1	1	0	6
7		0	1	1	1	7
8		1	0	0	0	8
9		1	0	0	1	9
OVERFLOW		1	1	0	0	⊔
DIGIT 0 ONLY	+1	0	0	0	0	+1
	−1	0	0	1	0	−1
	+	1	1	0	0	+
	−	0	1	1	1	−

Table 1. Output Coding

Component limitations such as switch leakage, as well as operational amplifier offset voltage and bias current (and the temperature dependency of these errors), are major obstacles when designing high resolution integrating A/D converters.

The AD7555 however, utilizes a patented *quad slope* conversion technique (Analog Devices Patent No. 3872466) to reduce the effects of such errors to second order effects.

Figure 1 shows a simplified quad slope integrator circuit. The various inputs AGND (Analog Ground), V_{REF1}, and AIN (Analog Input) are applied in sequence to the integrator via switches 1-3 (see Table 2), creating four slopes at the integrator output (phase 1-4 of Figure 2). If the equivalent summing junction voltage V_S is precisely $0.5V_{REF1}$, the phase 1 and phase 2 integration times are equal, indicating there are no input errors. If $V_S \neq 0.5V_{REF1}$ (due to amplifier offset voltage, bias current, etc.), an error count "n" is obtained. The analog input integration cycle (phase 3) is subsequently lengthened or shortened by "n" counts, depending on whether the error was positive or negative.

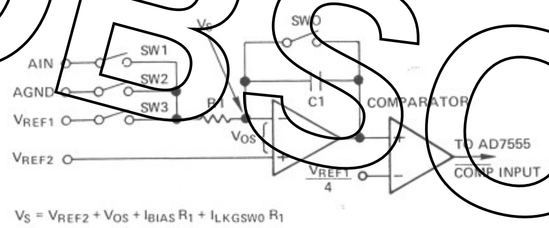
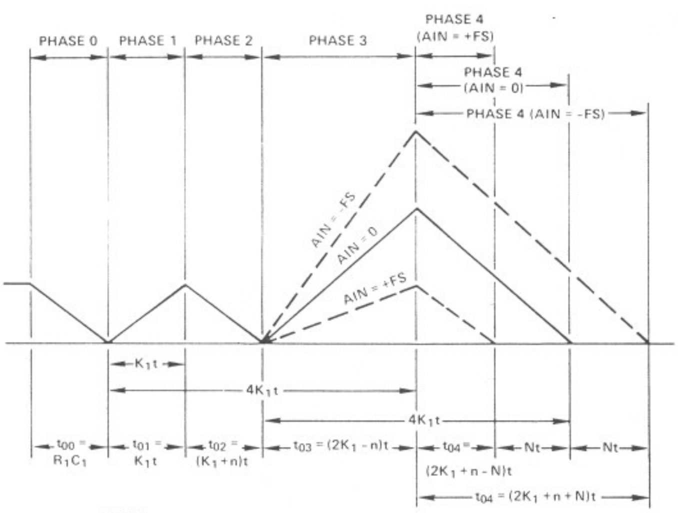


Figure 1. Simplified Quad Slope Integrator Circuit



NOTES:
1. FOR 4 1/2 DIGIT MODE, K_1 = 10,240
$t = 4 \times 1/f_{CLK}$, WHERE f_{CLK} IS CLOCK FREQUENCY AT PIN 12
2. FOR 5 1/2 DIGIT MODE, K_1 = 102,400
$t = 2/f_{CLK}$, WHERE f_{CLK} IS CLOCK FREQUENCY AT PIN 12
3. n = ERROR COUNT DUE TO AMPLIFIER OFFSETS ETC. AND CAN BE POSITIVE OR NEGATIVE.

Figure 2. Quad Slope Integrator Output

The final effect is to reduce the analog input error terms to second order effects. This can be proven by solving the differential equations obtained during the phase 1 through phase 4 integration periods. Barring third (and higher) order effects, the solutions are given in equations 1 and 2.

$$N_{(AIN \geq 0)} = \underbrace{K_T\left[\frac{AIN}{V_{REF1}}\right]}_{\text{IDEAL TERM}} + \underbrace{K_T\left[\frac{AIN}{V_{REF1}} - 1\right]\left[-a^2 + \frac{AGND}{V_{REF1}}(1+2a)\right]}_{\text{ERROR TERM}} \qquad \text{EQN1}$$

$$N_{(AIN < 0)} = \underbrace{-K_T\left[\frac{AIN}{V_{REF1}}\right]}_{\text{IDEAL TERM}} - \underbrace{K_T\left[\frac{AIN}{V_{REF1}} - 1\right]\left[-a^2 + \frac{AGND}{V_{REF1}}(1+2a)\right]}_{\text{ERROR TERM}} \qquad \text{EQN2}$$

WHERE:

N = Number of counts appearing at AD7555 Serial Count Out pin corresponding to the analog input voltage, AIN.

AIN = Analog Input Voltage to be digitized

K_T = 40960 counts (4 1/2 Digit Mode)
409600 counts (5 1/2 Digit Mode)

AGND = Voltage at AD7555 pin 3 (AGND) measured with respect to V_{REF1} and AIN signal common ground. (Ideally, AGND = 0V)

a is an error term equal to $\frac{2V_S - V_{REF1}}{V_{REF1}}$

Ideally $a = 0$ when $V_S = 0.5V_{REF1}$.

NOTE:
$V_S = V_{REF2} + V_{OS1} + V_{OS2} + I_{B2}R_1 + I_{SW0}R_1$

WHERE:

V_{REF2} = $0.5V_{REF1}$ if no error is present

V_{OS1} = Offset voltage of buffer amplifier A1 (required to buffer the effect of ΔR_{ON} of SW1 – SW2)

V_{OS2} = Offset voltage of integrator amplifier A2

$I_{B2}R_1$ = Equivalent integrator amplifier offset voltage due to bias current of A2

$I_{SW0}R_1$ = Equivalent integrator amplifier offset voltage due to SW0 leakage current.

If AGND = 0, then the error terms of EQN 1 and 2 contain only second order effects due to $a \neq 0$. Thus, the AD7555 is a powerful tool which allows high precision system performance to be obtained when using only moderate precision op amps.

Other advantages of the quad slope technique include bipolar operation using a single positive voltage reference, and the fact that since the comparator propagation delay is constant hysteresis effects are eliminated. (This is because the comparator always approaches the zero crossing from the same direction).

Phase	Switch Closed (Figure 1)	Equivalent Input Voltage	Integration Time
0	SW3	$V_{REF1} - V_S$	$t_{00} = R_1C_1$
1	SW2	$AGND - V_S$	$t_{01} = K_1t$
2	SW3	$V_{REF1} - V_S$	$t_{02} = (K_1 + n)t$
3	SW1	$AIN - V_S$	$t_{03} = (2K_1 - n)t$
4	SW3	$V_{REF1} - V_S$	$t_{04} = (2K_1 + n \pm N)t$
5	SW0	RESET INTEGRATOR	

Table 2. Integrator Equivalent Input Voltages and Integration Times

TIMING AND CONTROL

Figure 3 shows the AD7555 timing. SCC goes HIGH at the end of SCO indicating conversion is complete. DAV goes HIGH on the 1st leading edge of DMC after conversion is complete. New data is strobed into the data latches (see functional diagram) on the leading edge of the 2nd DMC. DAV returns low on the leading edge of the 3rd DMC.

BCD data is placed on B1, B2, B4, B8 on the positive edge of DMC while the digit counter is incremented on the negative edges of DMC.

A reset phase (phase 0) is initiated on the 4th DMC after conversion is complete. SCC returns low at the phase 0 comparator crossing indicating a conversion start.

If the DMC oscillator is set up to free run (C8 in Figure 6b causes DMC to run at about 1.5kHz), the AD7555 will continuously convert and update the displays.

Externally controlling the generation of DMC pulses provides a means of controlling data outputting for computer interface applications. Pages 10 and 11 illustrate how to use this feature to interface the AD7555 to a microprocessor.

DISPLAY

The output data format of the AD7555 is multiplexed BCD as per the Timing Diagram of Figure 3. The output code format is shown in Table 1.

Overflow causes digit 1 through digit 4 (digit 1 through digit 5 in 5 1/2 digit mode) to output a BCD 12 (1100). Overflow does not affect digit 0. Therefore, a positive overflow is displayed as +1, and a negative overflow as –1, , when using the 7447 seven-segment decoder.

PRINTED CIRCUIT LAYOUT

To ensure performance with the system specifications Figures 5a and 5b show the recommended P.C. board layout for the AD7555. Figure 4 shows the component overlay for Figure 5a.

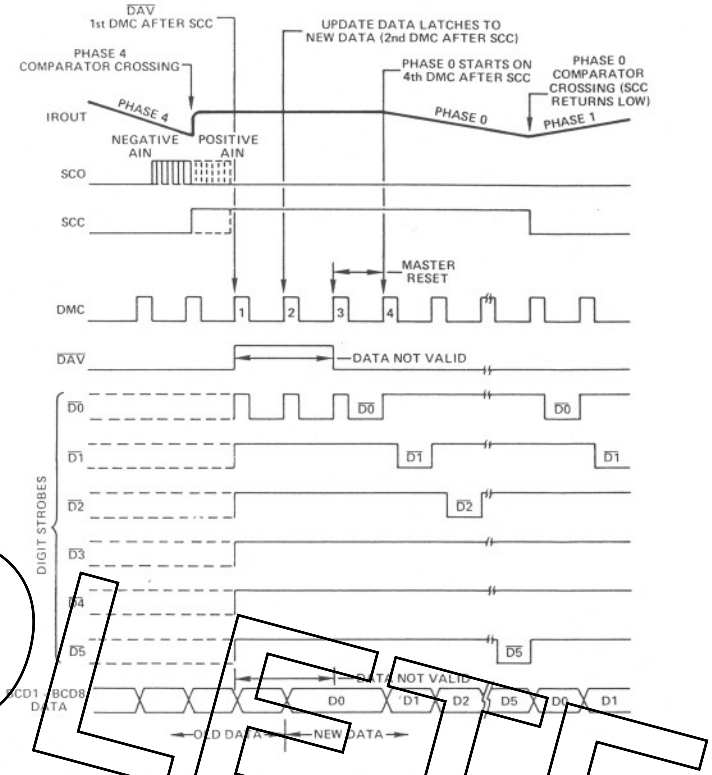


Figure 3. Timing Diagram (Self Start DPM Mode)

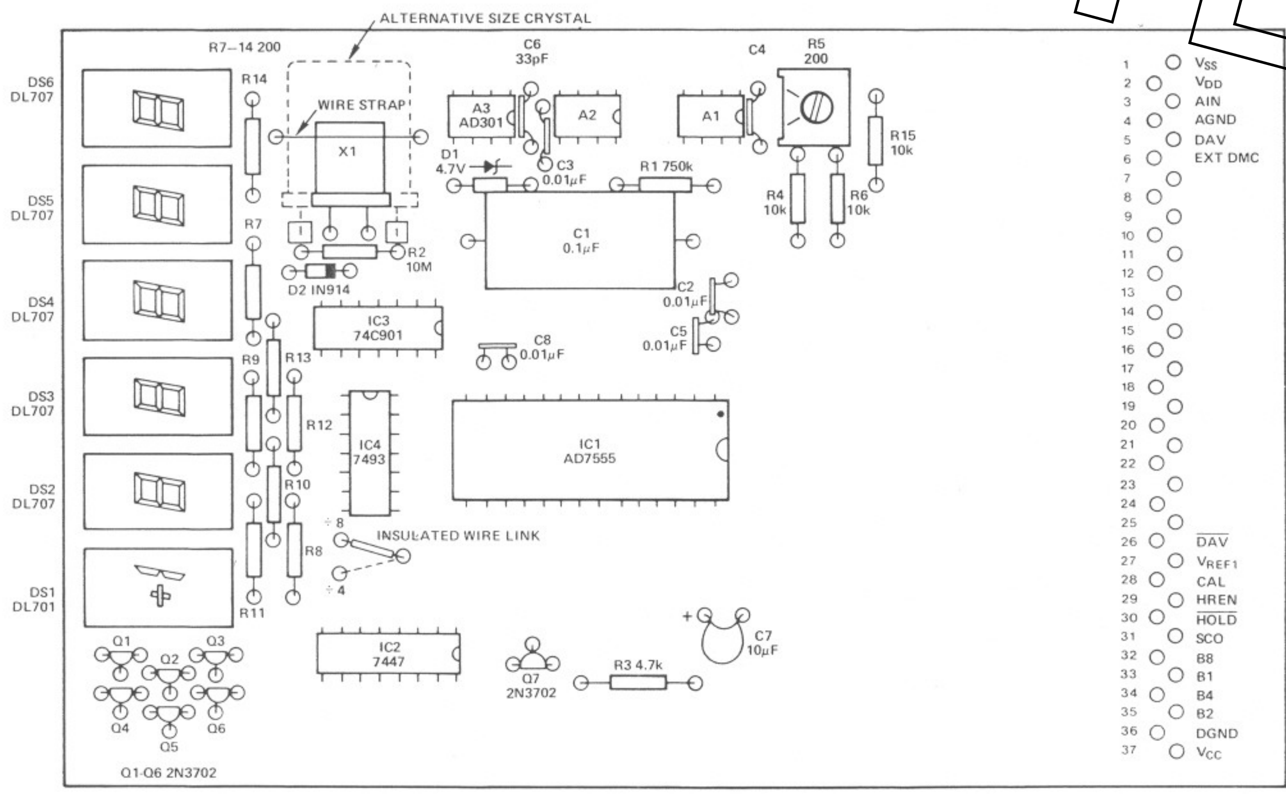


Figure 4. Component Overlay for Figure 5a

PCB Layout is reproduced on a one to one scale. Note that a pad already exists on the PCB layout for an AD584LH voltage reference, suitable for 4 1/2 digit operation.

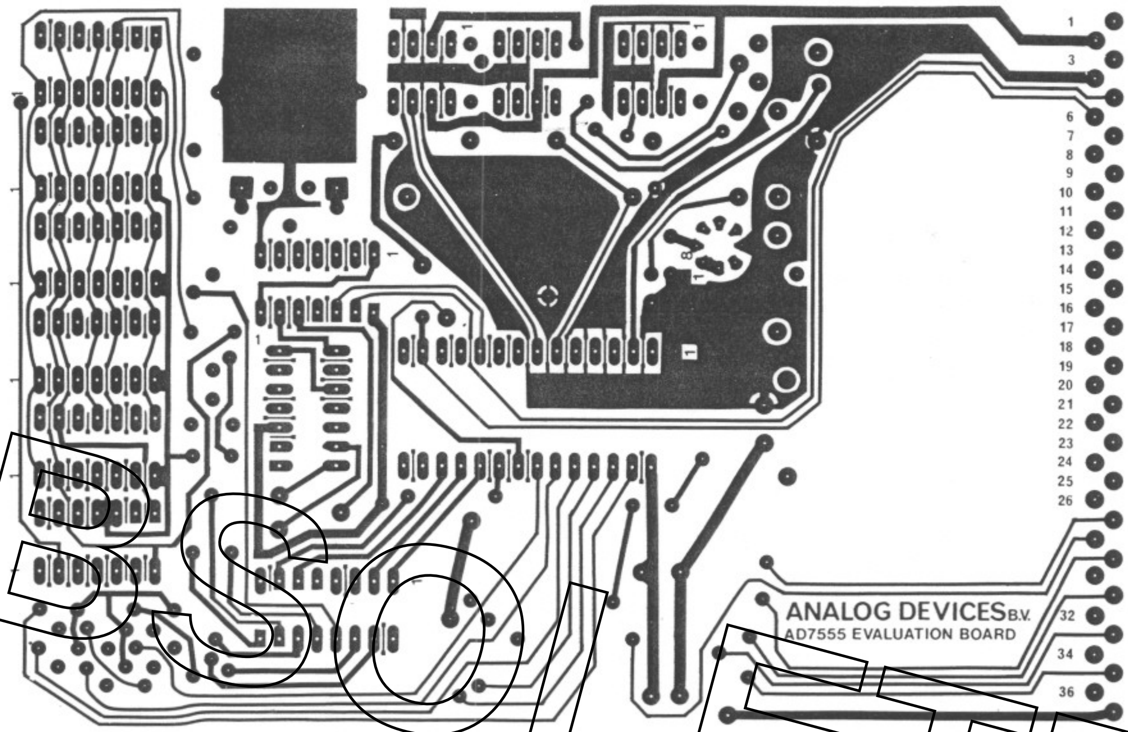


Figure 5a. Component Side

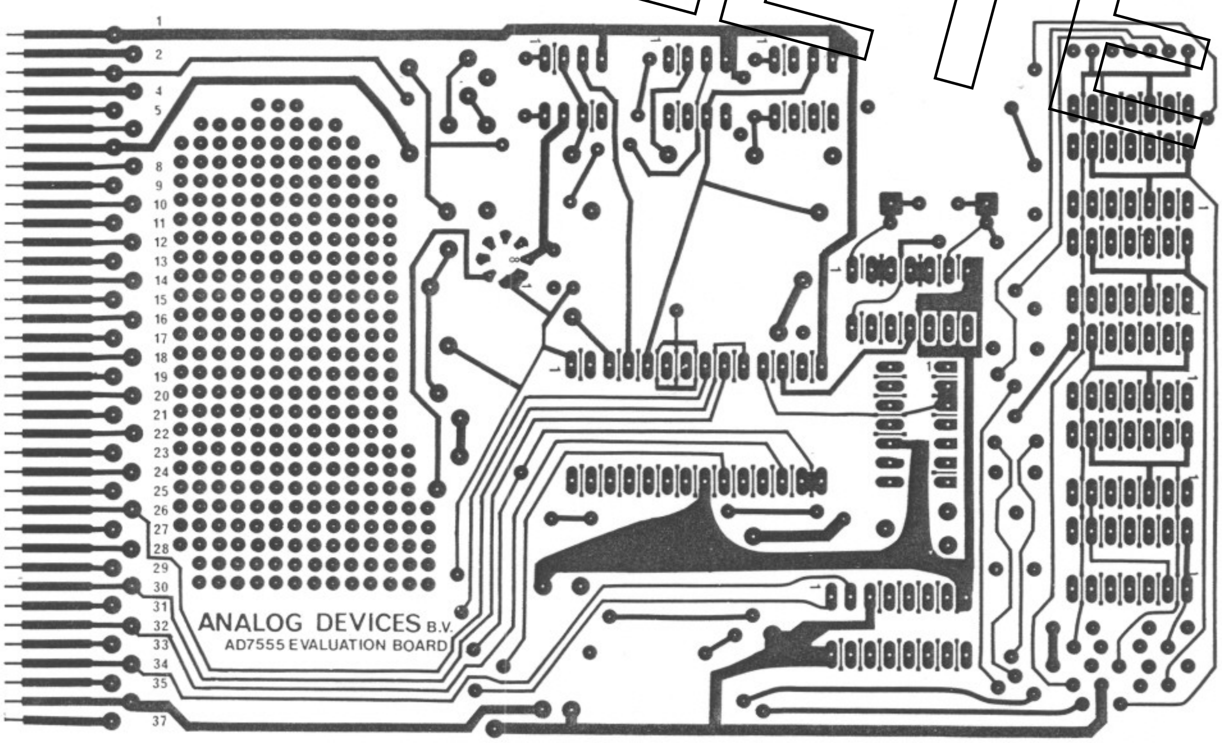


Figure 5b. Foil Side

ANALOG CIRCUIT SET-UP AND OPERATION

The following steps, in conjunction with the analog circuitry of Figure 6a explain the selection of the various component values required for proper operation.

1. **Selection of Integrator Components R_1 and C_1**
   Improper selection of the integrator time constant (time constant = R_1C_1) may cause excessive noise due to the integrator output level being too low, or may cause non-linear operation if the integrator output attempts to exceed the rated output voltage of the amplifier. The integrator time constant R_1C_1 must be:

   $$\frac{(V_{REF1})(K_a)}{(f_{CLK})(7V)} \geqslant R_1C_1 \geqslant \frac{(V_{REF1})(K_a)}{(f_{CLK})(V_{DD}-5V)}$$

   Where:

   V_{DD} is the integrator amplifier positive supply voltage
   f_{CLK} is the clock frequency at pin 12
   $K_a = 8.2 \times 10^4$ (4 1/2 digit mode)
   or 4.0×10^5 (5 1/2 digit mode)

   The integrating capacitor must be a low leakage, low dielectric absorption type such as teflon (5 1/2 digit mode), polystyrene or polypropylene (4 1/2 digit mode). To minimize noise injection, the outside foil of C1 must be connected to the output of the integrating amplifier, not to its summing junction.

   The recommended maximum value for R1 in both the 4 1/2 digit and 5 1/2 digit mode is 750kΩ. Higher values may cause noise injection.

2. **Determing Conversion Time**
   Maximum conversion time occurs when A_{IN} = –FS and is given by

   4 1/2 DIGIT MODE

   $$t_{CONVERT} = (325{,}760)(t_{CLK}) + R_1C_1$$

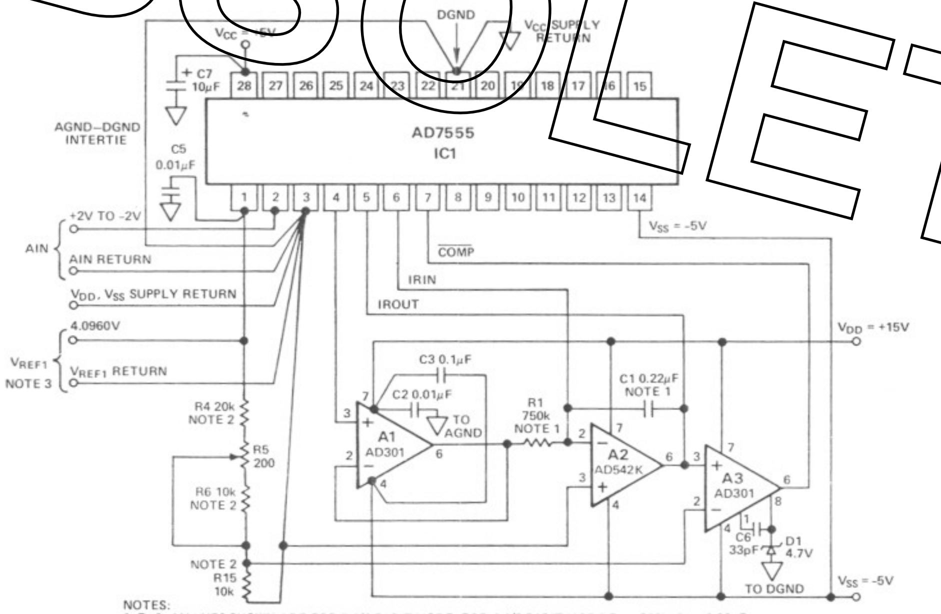
   5 1/2 DIGIT MODE

   $$t_{CONVERT} = (1{,}628{,}800)(t_{CLK}) + R_1C_1$$

   Where:

   t_{CLK} = Period of CLK as measured at pin 12
   R_1C_1 = Integrator Time Constant

3. **Initial Calibration**
   a. Adjust V_{REF1} so that the voltage at pin 1 (V_{REF1}) of the AD7555 is +4.0960V.
   b. Apply 0V to AIN and adjust R5 (V_{REF2} Adjust) for display 0.0000. (See optional calibration procedure on the next page for more precise calibration.)



NOTES:
1. R_1C_1 VALUES SHOWN ARE FOR 5 1/2 DIGIT MODE. FOR 4 1/2 DIGIT MODE R_1 = 360k, C_1 = 0.22μF. SUITABLE CAPACITORS AVAILABLE FROM COMPONENT RESEARCH CO. INC., 1655 26th STREET, SANTA MONICA, CA. 90404. (STOCK NUMBER FOR 0.22μF CAPACITOR IS D11B224KXW).
2. R4, R6, R15 1% TOLERANCE
3. FOR 4 1/2 DIGIT MODE USE AD584LH, FOR 5 1/2 DIGIT MODE A TEMPERATURE CONTROLLED BURIED ZENER REFERENCE SUCH AS THE LM399H SHOULD BE USED.

Figure 6a. Analog Circuit Diagram

APPLICATION HINTS

1. See Note under Absolute Maximum Ratings for proper power sequencing and input/output voltage ratings.
2. For linear operation the absolute magnitude of AIN cannot exceed 1/2 V_{REF1}. In no case must AIN be more negative than V_{SS}.
3. Do not leave unused CMOS inputs floating.
4. Check that integrator components R1 and C1 are chosen as per paragraph 1 of the setup and operation section on this page and that initial calibration as per paragraph 3 has been accomplished. A resistor value no larger than 750k is reccommended to minimize noise pickup.
5. For optimum normal mode noise rejection, use the crystal frequencies shown on page 4.
6. In order for the calibrate mode (on the next page) to display the error count properly it can be shown that
   $V_{REF2} \geqslant V_{REF1} \times 0.4883$
   Specifically, for V_{REF1} = 4.0960V
   $V_{REF1} \geqslant 2V$

LOGIC AND DISPLAY CIRCUITRY

The AD7555 possesses 4 1/2 digit accuracy with potential for 5 1/2 digit resolution. Figure 6b shows the logic and display circuitry when operating the AD7555 with this high resolution.

MODIFYING THE FULL SCALE DISPLAY

Availability of the SCO and SCI terminals on the AD7555 provides flexibility for range-switching and modified data-format applications.

For example, in the 5 1/2 digit mode, inserting a ÷5 counter between SCO and SCI provides a full scale count at SCI of 39,999 counts (199,999÷5).

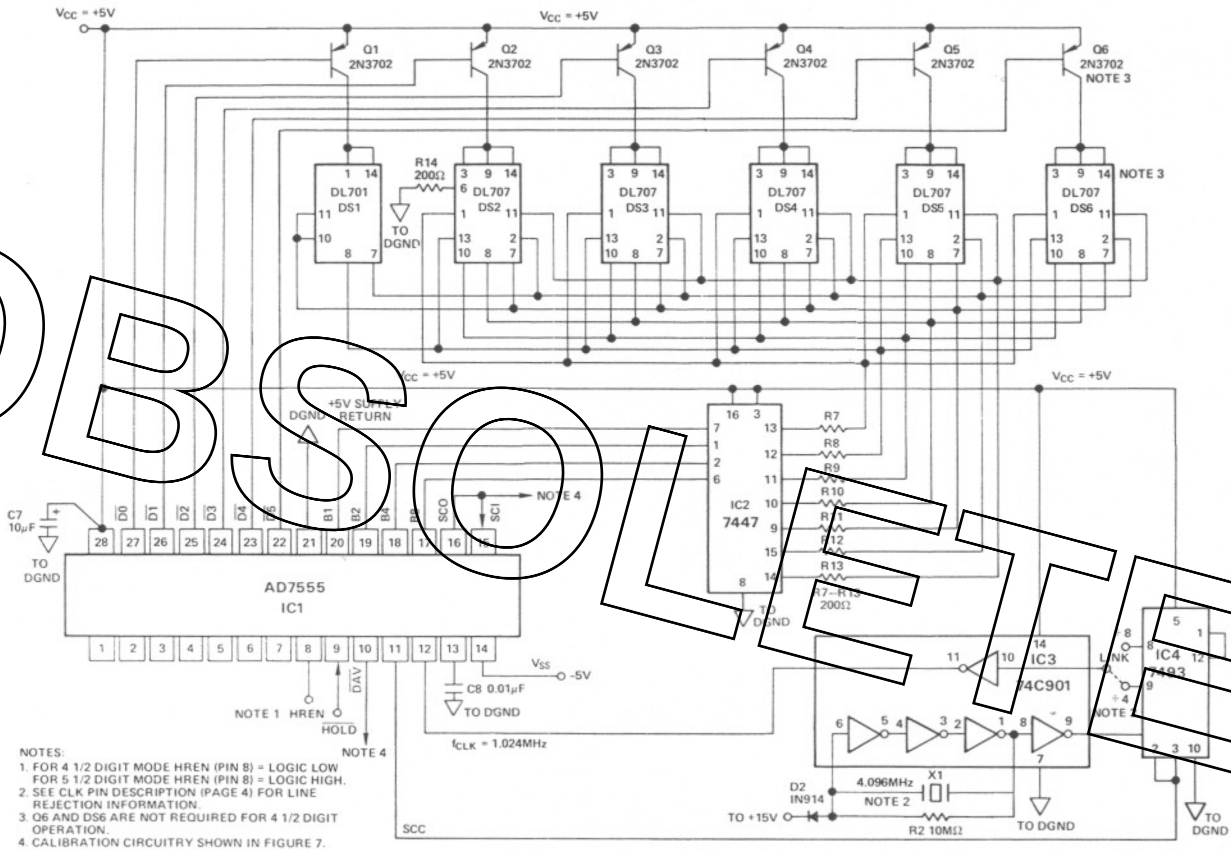


Figure 6b. Logic and Display Circuitry (for 5 1/2 Digit Resolution)

CALIBRATING THE AD7555

When the AD7555 is placed in the *calibrate* mode, any resulting error voltage in V_S (summing junction voltage), due to drift, etc., will be contained in the resulting display. To display the error SC1 and SC0 must be taken HIGH (only allowable when $\overline{\text{DAV}}$ is HIGH). In the *calibrate* mode the display indicates +b̸.0480 ±n (+b̸.04800 ±n in 5 1/2 digit mode) where b̸ indicates a blanked digit and n is a number representing the reference input errors. This gives the change required in V_{REF2} ($\pm\Delta V_{REF2}$) for proper calibration (ie., $n \approx 0$). The exact relationship between n and ΔV_{REF2} can be shown to be equal to:

$$\Delta V_{REF2} = \frac{(V_{REF1})n}{40{,}960 + n} \quad \text{(4 1/2 digit operation)}$$

$$\Delta V_{REF2} = \frac{(V_{REF1})\,10n}{40{,}960 + 10n} \quad \text{(5 1/2 digit operation)}$$

For this capability to operate, $|V_{REF2}|$ must be 1/2 V_{REF1} ±2%.

Figure 7 shows the hardware connections for manual calibration. With the switch in the *calibrate* mode, adjust V_{REF2} (potentiometer R5 as shown in Figure 6a) until the display reads +b̸.0480 (+b̸0.04800 in 5 1/2 digit mode). The AD7555 is now calibrated to the center of its error correcting range.

Return the switch to *normal* to resume normal conversion.

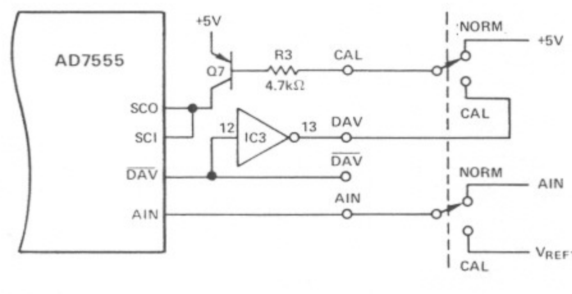


Figure 7. Hardware Requirements for Manual Calibration of n = 0

Microprocessor Interfacing

AD7555 AS A POLLED INPUT DEVICE (MCS-85 SYSTEM)

Figure 8 shows an AD7555/8085 interface. The DMC clock input of the AD7555 is controlled by the microcomputer via an output port of the 8155.

Typical timing for this interface mode is shown in Figure 9. $\overline{DAV}$ goes HIGH on the 1st DMC leading edge after SCC goes HIGH. It returns LOW on the rising edge of the 3rd DMC pulse. Digit zero is availabe on B1, B2, B4 and B8 at this time. The leading edge of the 4th DMC pulse initiates a new conversion and places digit 1 on B1, B2, B4 and B8.

Table 3 shows a procedure for polling the AD7555.

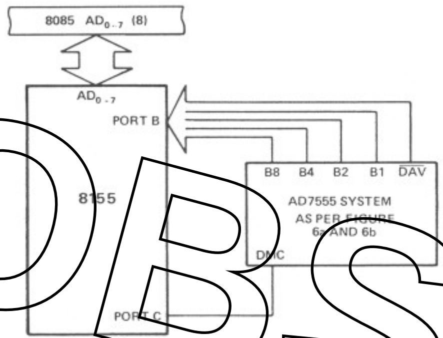


Figure 8. AD7555 as a Polled Input Device

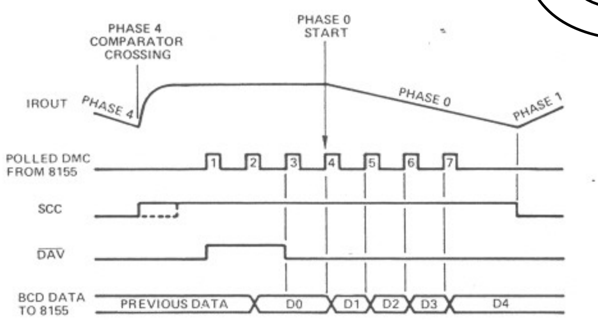


Figure 9. Timing Diagram for Operation as a Polled Input Device (8085/AD7555)

Put DMC HIGH
$\overline{DAV}$ HIGH?

NO:
Put DMC LOW
Delay or
Main Program

YES:
Put DMC LOW
Put DMC HIGH
Put DMC LOW
Put DMC HIGH
Put DMC LOW
Read BCD Data (Digit 0)
Put DMC HIGH (Initiates New Conversion)
Put DMC LOW
Read BCD Data (Digit 1)
Put DMC HIGH
Put DMC LOW
Read BCD Data (Digit 2)
etc.
Read BCD Data (Digit 4)

Table 3. Procedure for Interfacing the AD7555 as a Polled Input Device

AD7555 AS AN INTERRUPTING INPUT DEVICE (MCS-85 SYSTEM)

The AD7555 DMC oscillator provides DMC pulses until SCC (System Conversion Complete) goes high. This causes an interrupt on the RST 7.5 line whereby the three-state buffer is activated and the microprocessor takes control of DMC. Table 4 shows a procedure for using the AD7555 in this mode. Figure 10 shows the basic hookup.

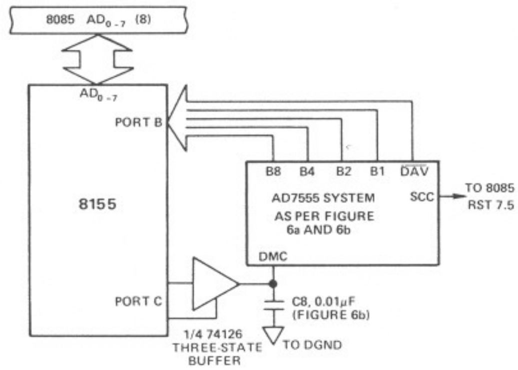


Figure 10. AD7555 as an Interrupting Input Device (MCS-85 System)

Interrupt Entry (SCC Goes High Causing Interrupt)

Enable Three-State Buffer (74126 as Shown in Figure 10)
Put DMC HIGH
$\overline{DAV}$ HIGH?

NO:
Put DMC LOW

YES:
Put DMC LOW
Put DMC HIGH
$\overline{DAV}$ LOW?

NO: (return to Put DMC LOW)

YES:
Put DMC LOW
Read BCD Data (Digit 0)
Put DMC HIGH
Put DMC LOW
Read BCD Data (Digit 1)
etc.
Read BCD Data (Digit 4)
Disable Three-State Buffer
Return to Main Program

Table 4. Procedure for Interfacing the AD7555 as an Interrupting Input Device

OPTO-ISOLATED SERIAL INTERFACE

Figure 11 shows a serial interface to the MCS-85 system. This system can accommodate a remote interface where a common-mode voltage is expected to exist between system grounds. The 8155 counter/timer is only 14 bits long, i.e., it can only count down from 2^{14}; therefore SCO output from the AD7555 (20k counts full scale) has to be divided by 2 with consequent reduction in system resolution.

Port C of the 8155 is configured as a control port. Port B is an input port. This port configuration is necessary if sign information is required. Magnitude information is obtained by interrogating the 8155 counter value. The rising edge of $\overline{DAV}$ is used to cause an interrupt on the RST 7.5 line. The value $\left(2^{14} - \left|\frac{SCO}{2}\right|\right)$ in the 8155 counter should now be read. When $\overline{DAV}$ returns low the 8155 counter is reset to FF_H. Sign information is checked at this time since $\overline{D_0}$ BCD data is present and stable on the BCD bus (see Figure 9). The B2 line of the BCD bus is latched into port B by the signal on B STB i.e. the falling edge of $\overline{DAV}$. This causes a rising edge signal on BF (buffer full) to call the 8085 CPU to read the B2 bit. B2 bit is HIGH for negative data, LOW for positive data.

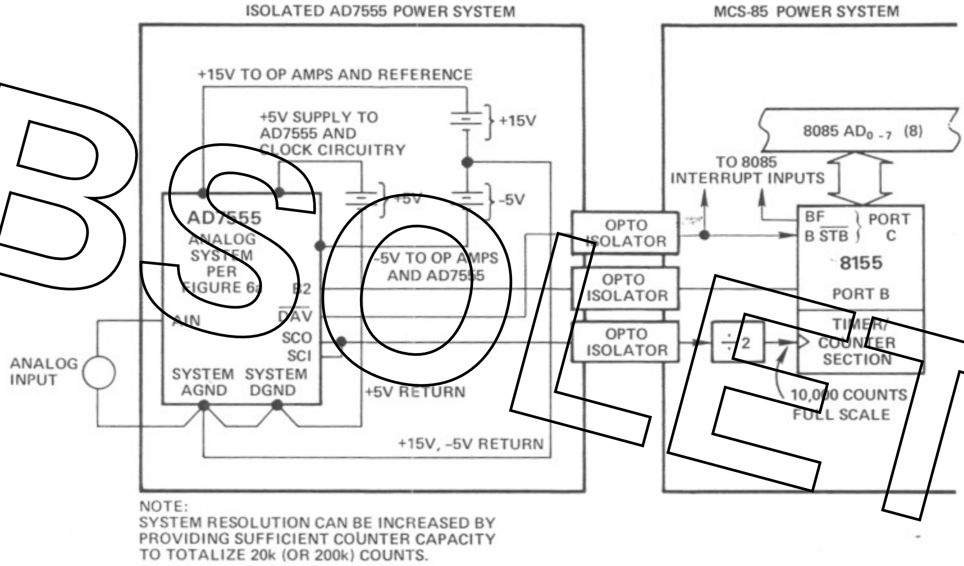
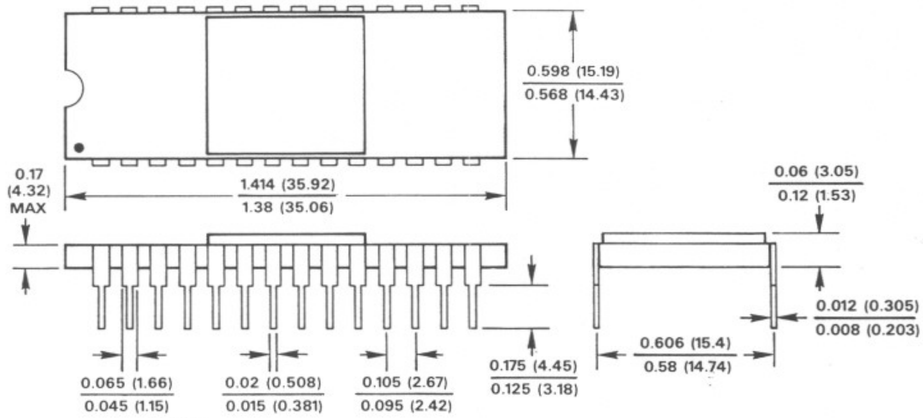


Figure 11. Optically Isolated Serial AD7555/MCS-85 Interface (Full Scale = 10,000 Counts)

OUTLINE DIMENSIONS

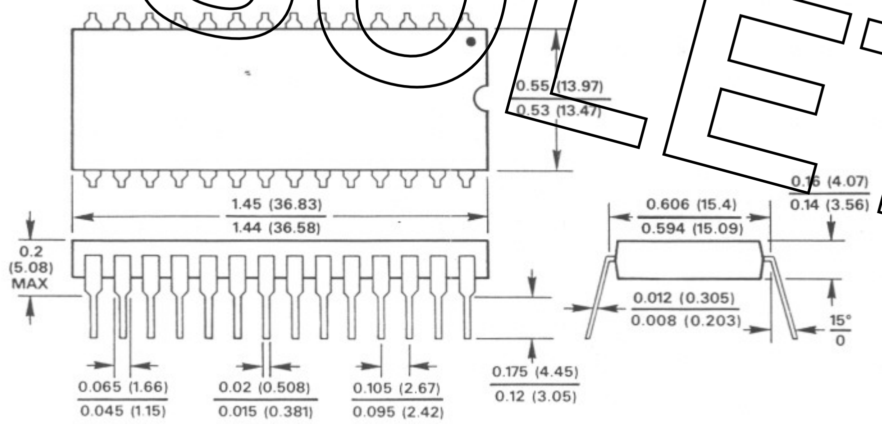
Dimensions shown in inches and (mm).

28-PIN CERAMIC DIP (SUFFIX D)



NOTES:
LEAD NO. 1 IS IDENTIFIED BY DOT OR NOTCH.
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42.

28-PIN PLASTIC DIP (SUFFIX N)



NOTES:
LEAD NO. 1 IS IDENTIFIED BY DOT OR NOTCH.
LEADS ARE GOLD-PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42.
CAVITY LID IS ELECTRICALLY ISOLATED.

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