

5 Line ESD Protection Diode Array

UESD6V85CT36 SC70-6 / SC88 / SOT363

General Description

The UESD6V85CT36 of TVS array is designed to protect sensitive electronics from damage or latch-up due to ESD, for use in applications where board space is at a premium. It is unidirectional device and may be used on lines where the signal polarities are above ground, each device will protect up to five lines.

TVS diodes are solid-state devices feature large cross-sectional area junctions for conducting high transient currents, specifically for transient suppression. It offers desirable characteristics for board level protection including fast response time, low clamping voltage, and no device degradation.

The UESD6V85CT36 may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4. The small package makes them ideal for use in portable electronics such as cell phones, PDAs, notebook computers, and digital cameras.

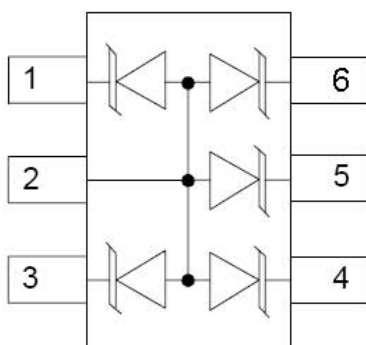
Applications

Cellular Handsets & Accessories
 Cordless Phones
 Personal Digital Assistants (PDAs)
 Notebooks & Handhelds
 Portable Instrumentation
 Digital Cameras
 Peripherals
 MP3 Players

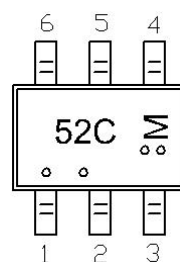
Features

Transient protection for data lines to
 IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact)
 Protects five I/O lines
 Ultra-small SC70-6/SC88/SOT363 package
 Working voltage: 5V
 Low leakage current
 Low operating and clamping voltages
 Solid-state silicon-avalanche technology

Pin Configurations



Top View



“.”:Option

M: Monthly Code

UESD6V85CT36

SC70-6 / SC88 / SOT363

Ordering Information

| Part Number | Working Voltage | Packaging Type | Channel | Marking Code | Shipping Qty |
|--------------|-----------------|------------------------|---------|--------------|---------------------|
| UESD6V85CT36 | 5.0V | SC70-6 / SC88 / SOT363 | 5 | 52C | 3000/7 Inch Reel |

Absolute Maximum Ratings

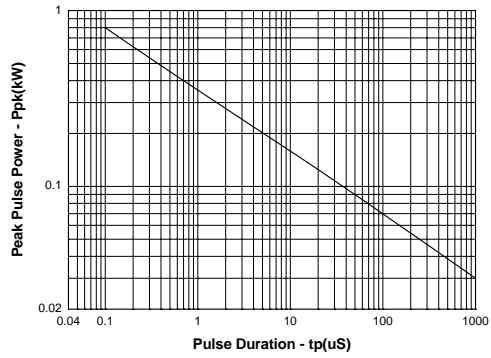
| RATING | SYMBOL | VALUE | UNITS |
|---|-----------------|--------------|--------------|
| Peak Pulse Power ($t_p = 8/20 \mu s$) @ $T_A \leq 25^\circ C$ | P_{PK} | 140 | Watts |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 325 | $^\circ C/W$ |
| Lead Soldering Temperature | T_L | 260(10 sec.) | $^\circ C$ |
| Operating Temperature | T_J | -55 to +125 | $^\circ C$ |
| Storage Temperature | T_{STG} | -55 to +125 | $^\circ C$ |
| Maximum Junction Temperature | T_{JMAX} | 150 | $^\circ C$ |

Electrical Characteristics

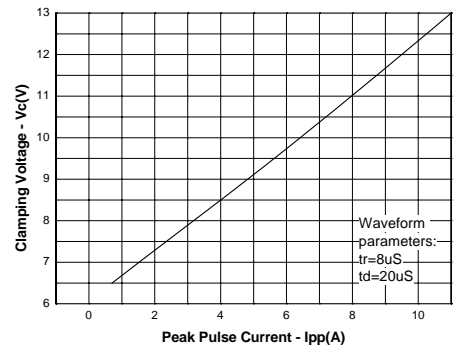
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|-----------|---|-----|-----|-----|---------|
| Reverse Stand-Off Voltage | V_{RWM} | | | | 5 | V |
| Reverse Breakdown Voltage | V_{BR} | $I_t = 1mA$ | 6 | 6.8 | 7.2 | V |
| Reverse Leakage Current | I_R | $V_{RWM} = 5V, T=25^\circ C$ | | | 0.1 | μA |
| Clamping Voltage | V_C | $I_{PP} = 5A, t_p = 8/20\mu S$ | | | 9.1 | V |
| | | $I_{PP} = 11A, t_p = 8/20\mu S$ | | | 13 | |
| Junction Capacitance | C_J | Pin 1, 3, 4, 5, 6 to 2 $V_R = 0V, f = 1MHz$ | | 40 | 50 | pF |
| Junction Capacitance | C_J | Pin 1, 3, 4, 5, 6, to 2 $V_R = 2.5V, f = 1MHz$ | | 30 | 40 | pF |

Typical Operating Characteristics

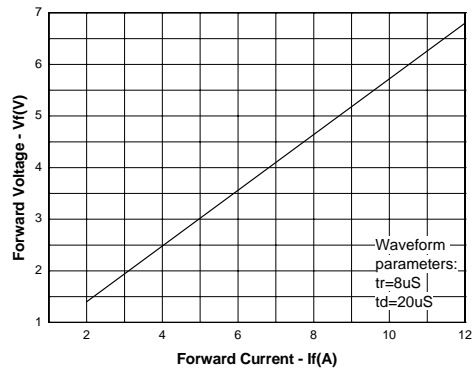
Non-Repetitive Peak Pulse Power vs. Pulse Time



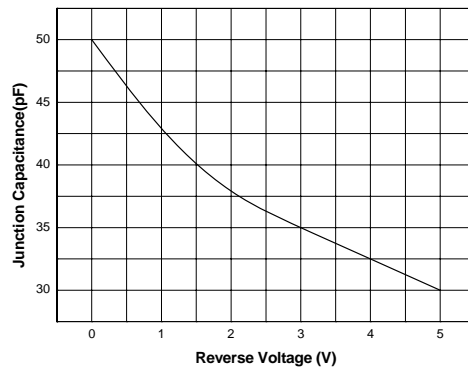
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Junction Capacitance vs. Reverse Voltage



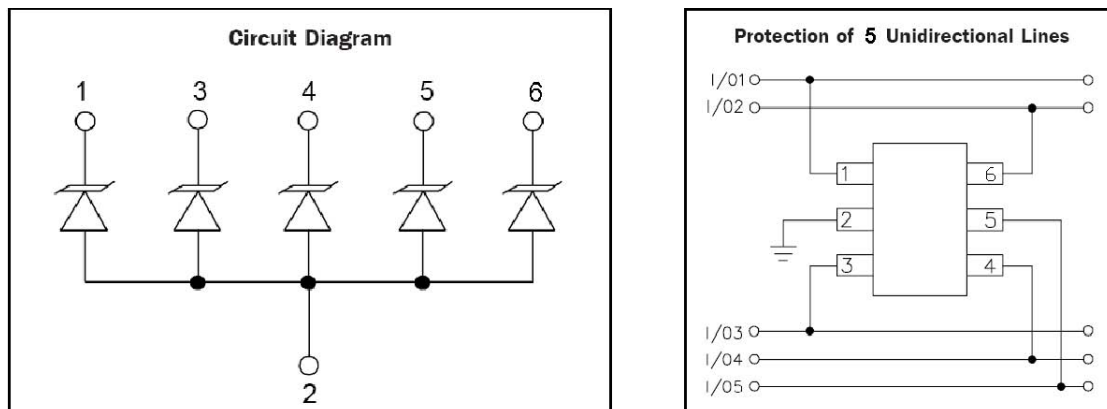
Applications Information

UESD6V85CT36 ESD protection diode is designed to protect 5 data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode should be placed towards the line that is to be protected.

Device Connection for Protection of Quad Data Lines

The UESD6V85CT36 TVS diode array is designed to protect up to five unidirectional data lines. The device as follows:

Unidirectional protection of five I/O lines is achieved by connecting pins 1, 3, 4, 5, and 6 to the data lines. Pin 2 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.



Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.

- Minimize the path length between the TVS and the protected line.

- Minimize all conductive loops including power and ground loops.

- The ESD transient return path to ground should be kept as short as possible.

- Never run critical signals near board edges.

- Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.

- Keep parallel signal paths to a minimum.

- Avoid running protection conductors in parallel with unprotected conductor.

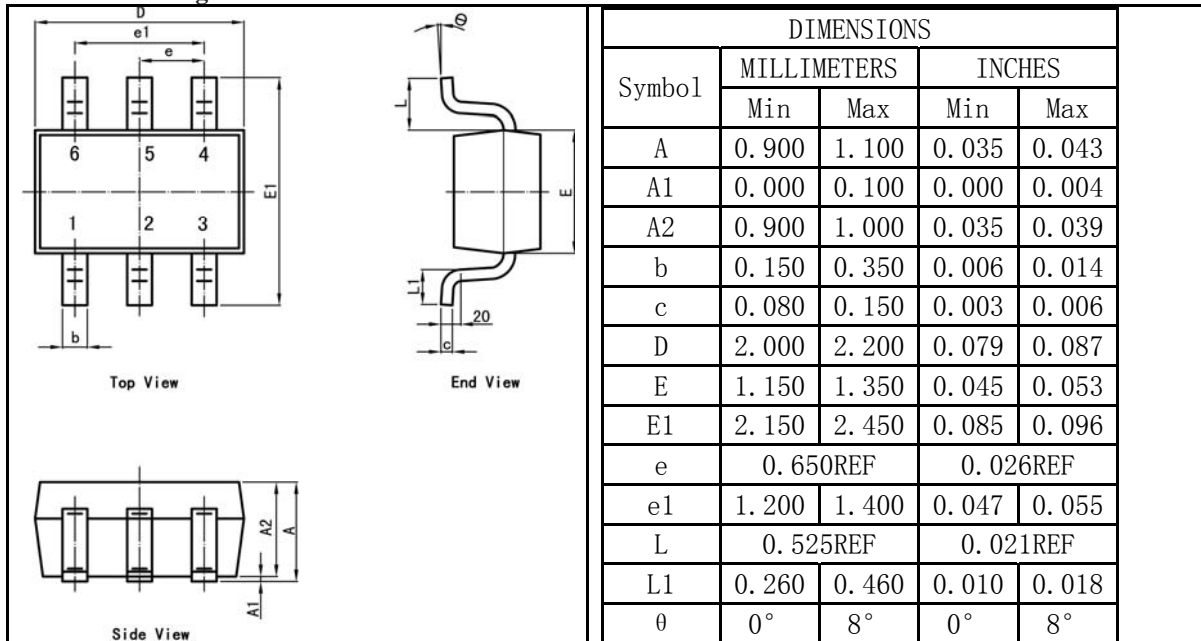
- Minimize all printed-circuit board conductive loops including power and ground loops.

- Avoid using shared transient return paths to a common ground point.

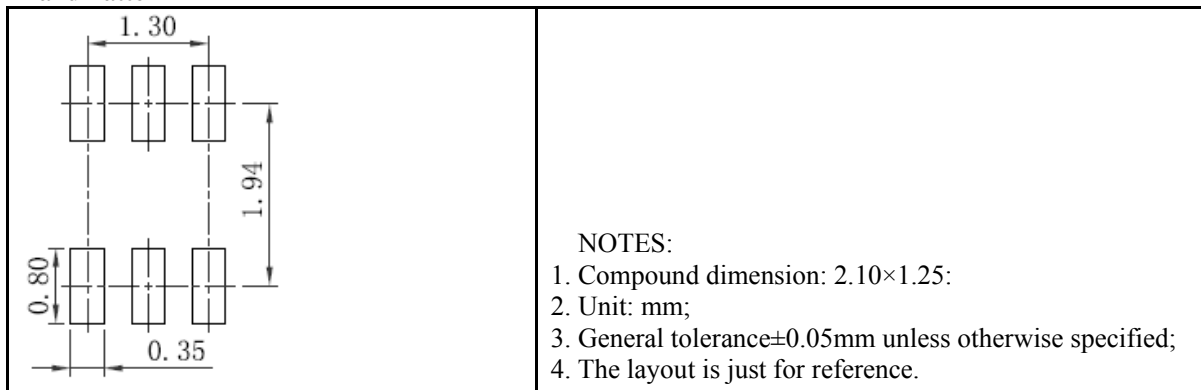
Package Information

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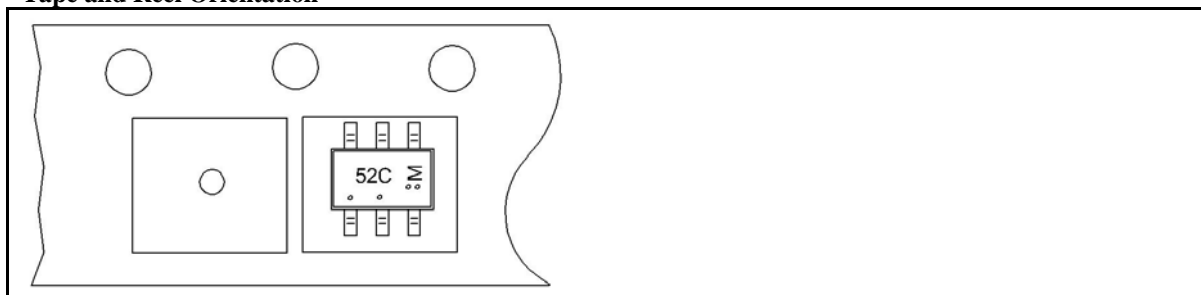
Outline Drawing



Land Pattern



Tape and Reel Orientation



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