To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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H7N1005DL, H7N1005DS

Silicon N Channel MOS FET
High Speed Power Switching

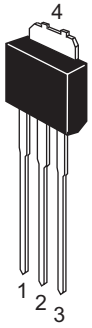
REJ03G1736-0100
Rev.1.00
Sep 19, 2008

Features

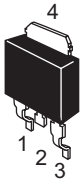
- Low on-resistance
  $R_{DS\ (on)}$ = 85 mΩ typ.
- Low drive current
- Capable of 4.5 V gate drive

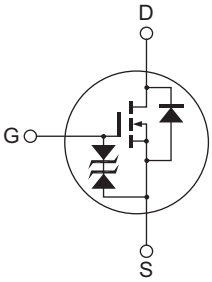
Outline

RENESAS Package code: PRSS0004ZD-B
(Package name: DPAK (L)-(2))



RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))





1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	12	A
Drain peak current	$I_{D\ (pulse)}$ Note 1	30	A
Body to drain diode reverse drain current	I_{DR}	12	A
Avalanche current	I_{AP} Note 2	8	A
Avalanche energy	E_{AR} Note 2	6.4	mJ
Channel dissipation	Pch Note 3	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. Value at Tc = 25°C

Electrical Characteristics

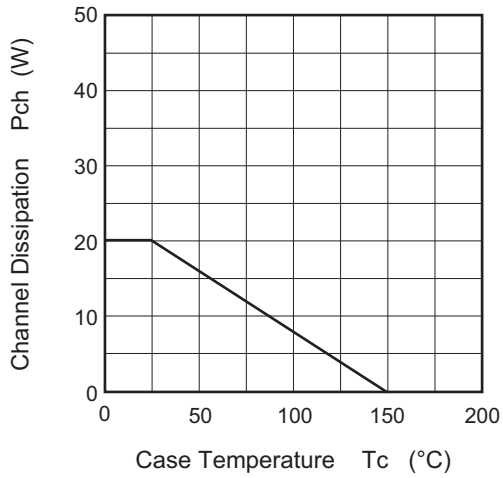
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 100 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS (off)}$	1.5	—	2.5	V	I_D = 1 mA, V_{DS} = 10 V Note 4
Static drain to source on state resistance	$R_{DS (on)}$	—	85	110	mΩ	I_D = 6.0 A, V_{GS} = 10 V Note 4
		—	105	155	mΩ	I_D = 6.0 A, V_{GS} = 4.5 V Note 4
Forward transfer admittance	$\|y_{fs}\|$	6.5	11	—	S	I_D = 6.0 A, V_{GS} = 10 V Note 4
Input capacitance	Ciss	—	830	—	pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	90	—	pF	
Reverse transfer capacitance	Crss	—	55	—	pF	
Total gate charge	Qg	—	15	—	nC	V_{DD} = 50 V V_{GS} = 10 V I_D = 12 A
Gate to source charge	Qgs	—	3.0	—	nC	
Gate to drain charge	Qgd	—	4.0	—	nC	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	V_{GS} = 10 V, I_D = 6.0 A R_L = 5 Ω Rg = 4.7 Ω
Rise time	t_r	—	62	—	ns	
Turn-off delay time	$t_{d(off)}$	—	42	—	ns	
Fall time	t_f	—	6.5	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 12 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	40	—	ns	I_F = 12 A, V_{GS} = 0 di_F/dt = 100 A/µs

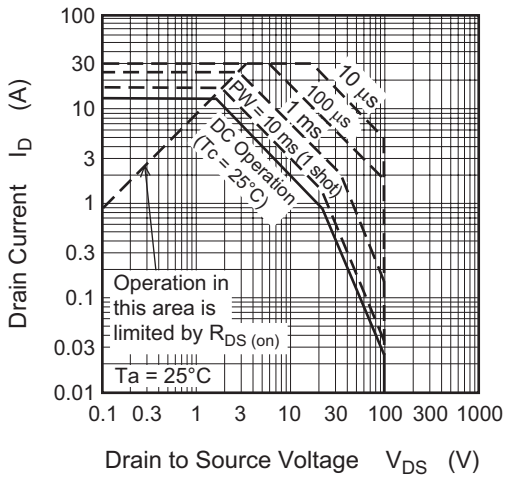
Note: 4. Pulse test

Main Characteristics

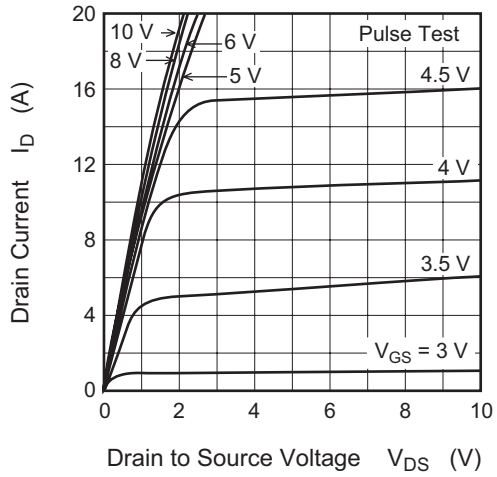
Power vs. Temperature Derating



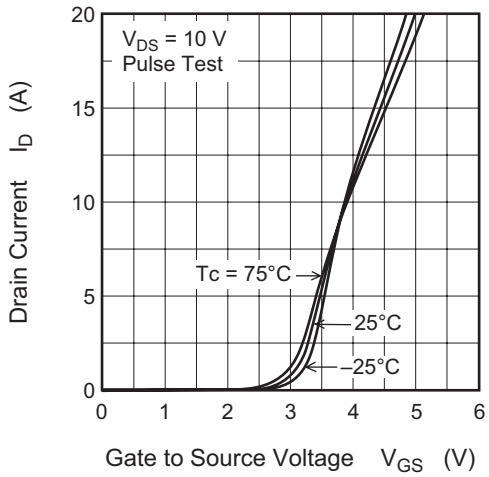
Maximum Safe Operation Area



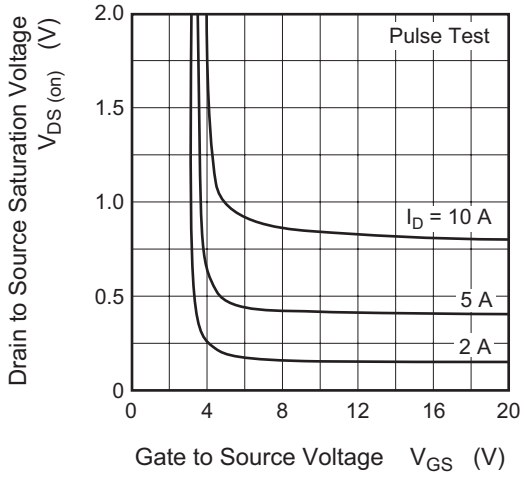
Typical Output Characteristics



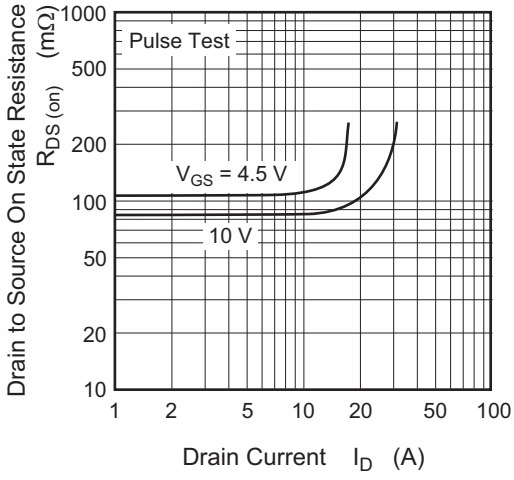
Typical Transfer Characteristics



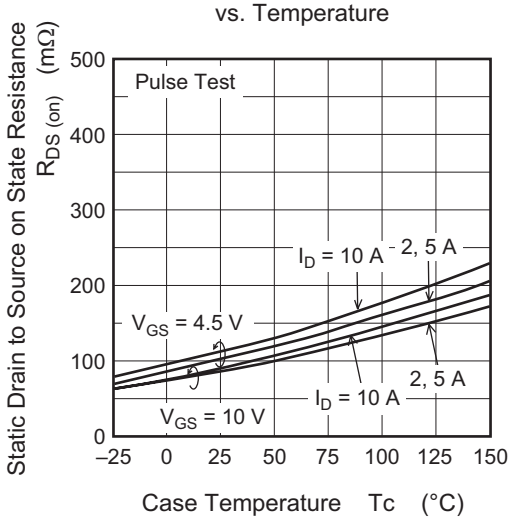
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



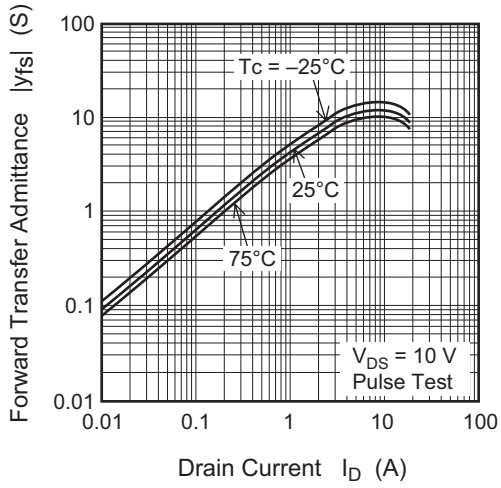
Static Drain to Source on State Resistance
vs. Drain Current



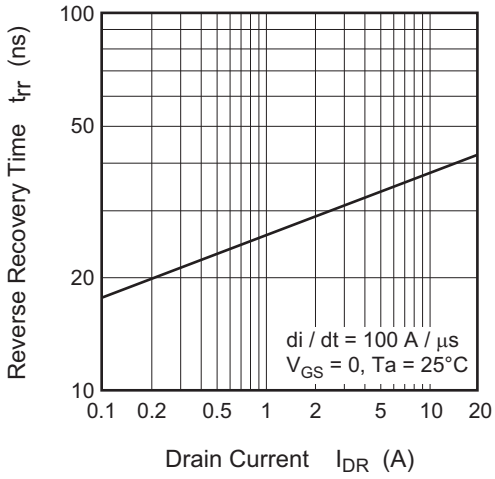
Static Drain to Source on State Resistance vs. Temperature



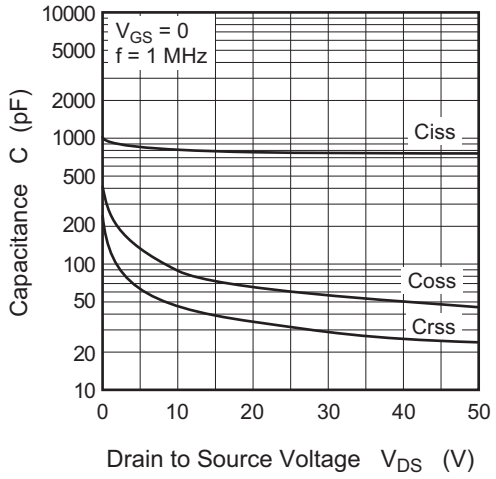
Forward Transfer Admittance vs. Drain Current



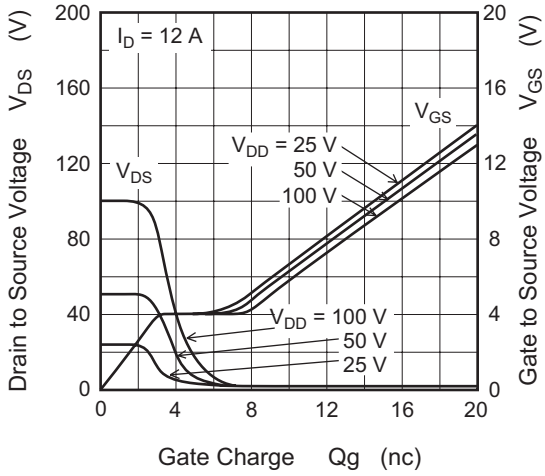
Static Drain to Source on State Resistance vs. Drain Current



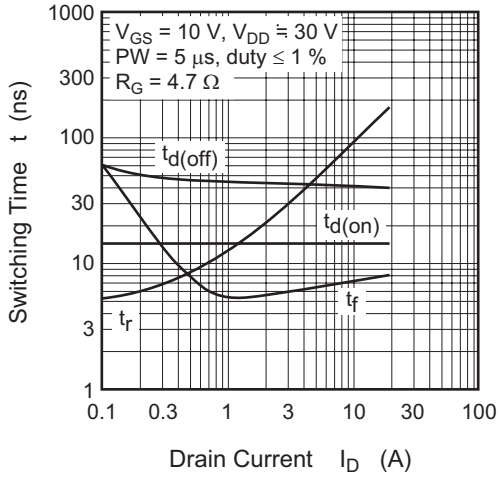
Typical Capacitance vs. Drain to Source Voltage



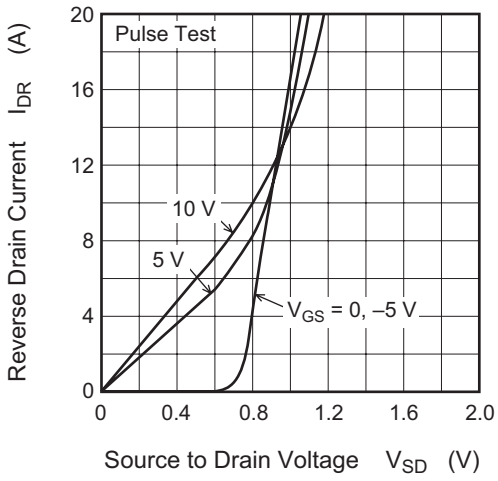
Dynamic Input Characteristics



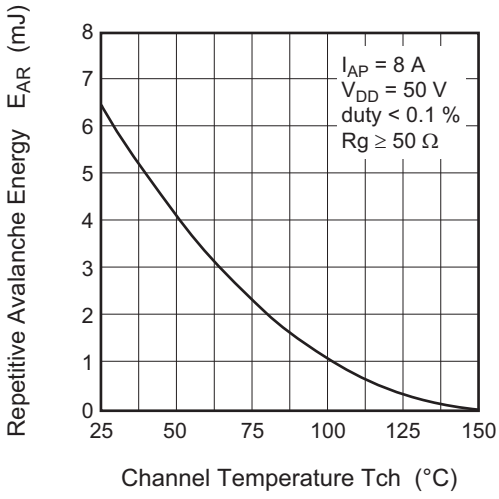
Switching Characteristics



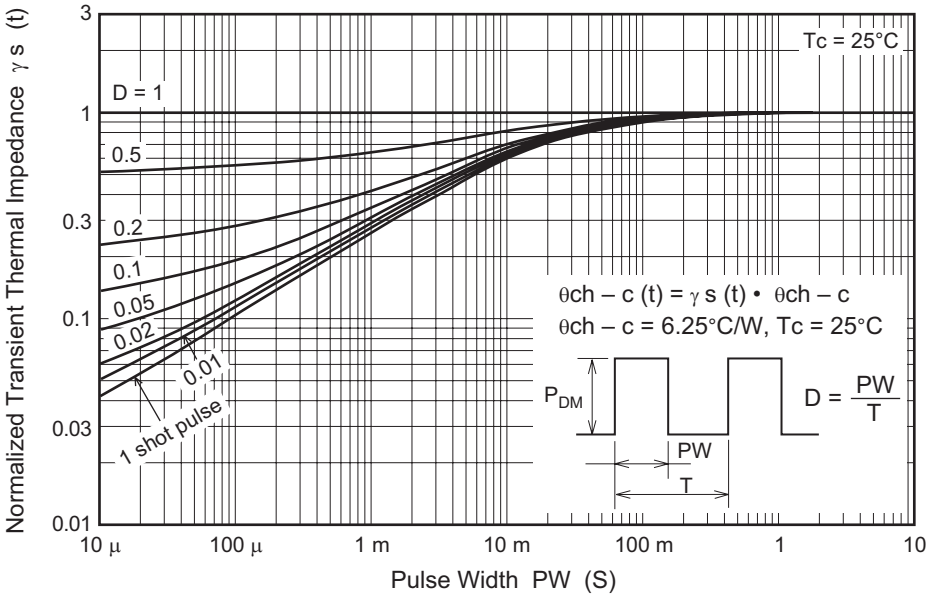
Reverse Drain Current vs. Source to Drain Voltage



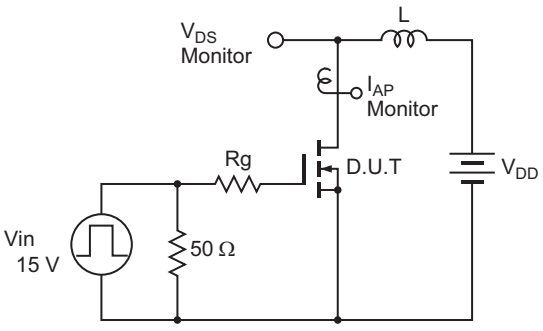
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

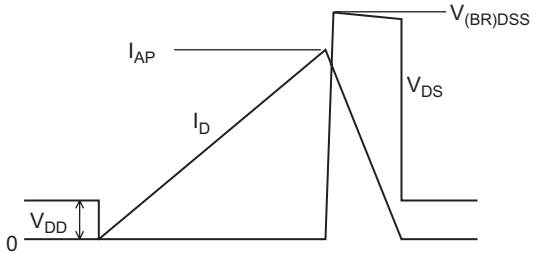


Avalanche Test Circuit

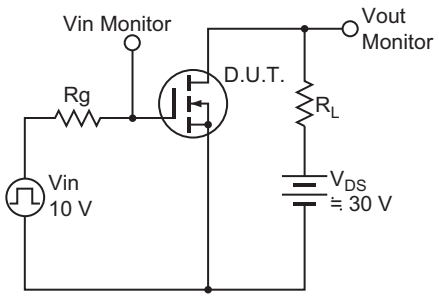


Avalanche Waveform

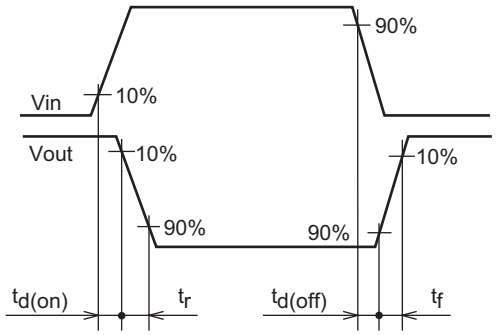
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



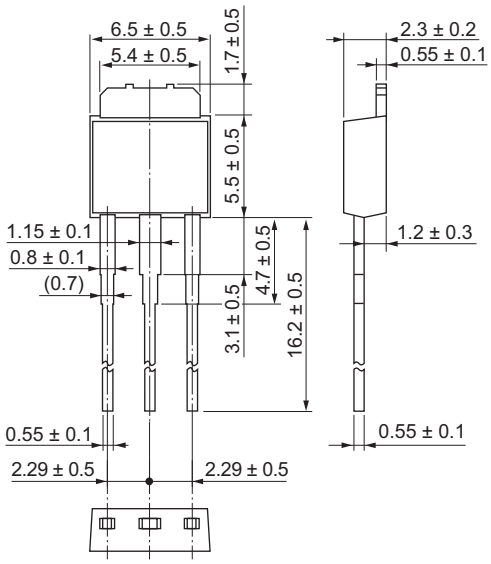
Switching Time Waveform



Package Dimensions

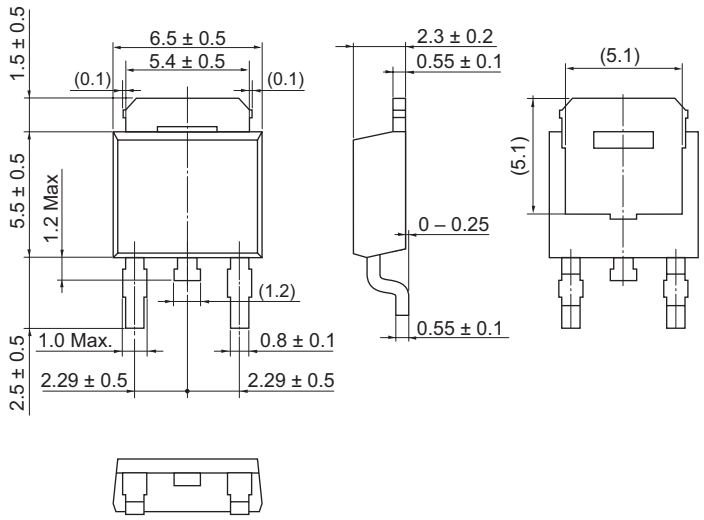
Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
DPAK(L)-(2)	—	PRSS0004ZD-B	DPAK(L)-(2) / DPAK(L)-(2)V	0.42g

Unit: mm



Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
DPAK(S)	SC-63	PRSS0004ZD-C	DPAK(S) / DPAK(S)V	0.28g

Unit: mm



Ordering Information

Part No.	Quantity	Shipping Container
H7N1005DL-E	3200 pcs	Box (Conductive Sack)
H7N1005DSTL-E	3000 pcs	Taping

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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Colophon .7.2