STANDARD
MICROSYSTEMS
CORPORATION

MON35W82

Hardware Monitoring IC – I²C Interface Only

FEATURES

- **Monitoring Items**
  - 3 Thermal Inputs From Remote Thermistors or 2N3904 NPN-type Transistors or Pentium™ II (Deschutes) thermal diode output
  - 6 Voltage Inputs Typical for Vcore, +3.3V, +12V, -12V, +5V, -5V (Optional)
  - 3 Fan Speed Monitoring Inputs
  - WATCHDOG™ Comparison of all Monitored Values
  - Programmable Hysteresis and Setting Points (Alarm Thresholds) for all Monitored Items
- **Actions Enabling**
  - Beep Tone Warning
  - 2 PWM (Pulse Width Modulation) Outputs for Fan Speed Control (MUX Optional)
    - Total up to 2 Sets of Fan Speed Monitoring and Controlling.
  - Issues nSMI, nOVT and nGPO Signals to Activate System Protection
  - Warning Signal Pop-Up in Application Software
- **General**
  - I²C™ Serial Bus Interface
  - 5 VID Input Pins for CUP Vcore Identification (for Pentium™ II)
  - Initial Power Fault Beep (for +3.3V, Vcore)
  - Intel™ LDCM (DMI Driver 2.0) Support
  - Acer™ ADM (DMI Driver 2.0) Support
  - Input Clock Rate Optional for 24, 48, and 14.318 MHz
  - 5V Vcc Operation
- **Package**
  - 24 Pin SOP

GENERAL DESCRIPTION

The MON35W82 is an enhanced version of the MON35W42. The MON35W82 can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for proper operation and stability of a high-end computer system. The MON35W82 provides an I²C™ serial bus interface.

An 8-bit analog-to-digital converter (ADC) is contained inside the MON35W82. The MON35W82 can monitor 6 analog voltage inputs, 3 fan tachometer inputs, and 3 remote temperatures. The remote temperature sensing can be performed by thermistors, 2N3904 NPN-type transistors, or directly from Intel's™ Deschutes CPU thermal diode output. The MON35W82 also provides: 2 PWM (pulse width modulation) outputs for the fan speed control; beep tone output for warning; nSMI, nOVT, and nGPO signals for system protection events.

With application software such as the Intel™ LDCM (LAN Desk Client Management) the user

can read all the monitored parameters of the system from time to time. And a pop-up warning can be activated when the monitored item drifts out of the proper/preset range. Also the user can set the upper and lower limits (alarm thresholds) of these monitored parameters and activate programmable and maskable interrupts. An optional beep tone could be used as a warning signal when the monitored parameters are out of the preset range.

Additionally, 5 VID inputs are provided to read the VID of the CPU (i.e. Pentium™ II) if applicable. This will provide automatic correction of the Vcore voltage. The MON35W82 also uniquely provides an optional feature: early stage (before BIOS is loaded) beep warning. This is to detect if the fatal elements such as Vcore or 3.3V voltage fail are present.

KEY SPECIFICATIONS

- Voltage monitoring accuracy ±1% (Max)
- Monitoring Temperature Range and Accuracy
  - 40°C to +120°C ± 3°C (Max)
- Supply Voltage 5V
- Operating Supply Current 5 mA typ.
- ADC Resolution 8 Bits

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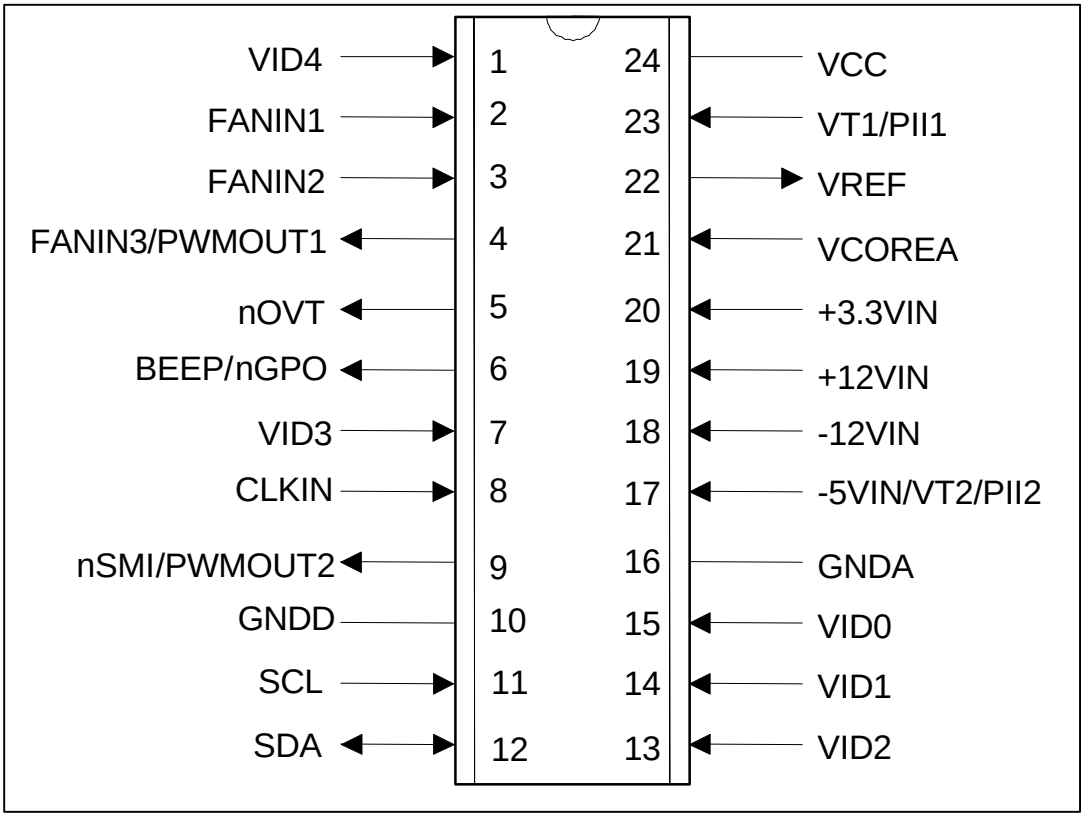
PIN CONFIGURATION



PIN DESCRIPTION

PIN NAME	PIN NO.	TYPE	DESCRIPTION
VID4	1	IN_t	Voltage Supply readouts from Pentium II™.
FANIN1	2	IN_{ts}	0V to 5V amplitude fan tachometer input.
FANIN2	3	IN_{ts}	0V to 5V amplitude fan tachometer input.
FANIN3 / PWMOUT1	4	IN_{ts} / OUT_{12t}	0V to 5V amplitude fan tachometer input. Fan speed control (PWM) output. This multi-functional pin is programmable.
nOVT	5	OUT_{12t}	Over temperature Shutdown Output.
BEEP/nGPO	6	OD_{48}	Beep (Default) / General purpose output This multi-functional pin is programmable.
VID3	7	IN_t	Voltage Supply readouts from Pentium II™.
CLKIN	8	IN_t	System clock input. Can select 48MHz or 24MHz or 14.318MHz. The default is 24MHz.
nSMI / PWMOUT2	9	OD_{12} / OUT_{12t}	System Management Interrupt (open drain). The default state is disabled. Fan speed control (PWM) output. This multi-functional pin is programmable.
GNDD	10	DGROUND	Internally connected to all digital circuitry.
SCL	11	IN_{ts}	Serial Bus Clock.
SDA	12	I/O_{12ts}	Serial Bus bi-directional Data.
VID2	13	IN_t	Voltage Supply readouts from Pentium II™.
VID1	14	IN_t	Voltage Supply readouts from Pentium II™.
VID0	15	IN_t	Voltage Supply readouts from Pentium II™.
GNDA	16	AGROUND	Internally connected to all analog circuitry. The ground reference for all analog inputs.
-5VIN / VT2 / PII2	17	AIN	0V to 4.096V FSR Analog Inputs (Default). Thermistor 2 terminal input. Pentium II™ thermal 2 diode input. This multi-functional pin is programmable.
-12VIN	18	AIN	0V to 4.096V FSR Analog Inputs.
+12VIN	19	AIN	0V to 4.096V FSR Analog Inputs.
+3.3VIN	20	AIN	0V to 4.096V FSR Analog Inputs.
VCOREA	21	AIN	0V to 4.096V FSR Analog Inputs.
VREF	22	AOUT	Reference Voltage.
VT1 / PII1	23	AIN	Thermistor 1 terminal input. / Pentium II™ thermal diode 1 input.
V_{CC} (+5V)	24	POWER	+5V V_{CC} power. Bypass with the parallel combination of 10µF (electrolytic or tantalum) and 0.1µF (ceramic) bypass capacitors.

PIN DESCRIPTION

I/O_{12t}	TTL level bi-directional pin with 12 mA source-sink capability
I/O_{12ts}	TTL level and schmitt trigger
OUT_{12}	Output pin with 12 mA source-sink capability
AOUT	Output pin(Analog)
OD_{12}	Open-drain output pin with 12 mA sink capability
IN_t	TTL level input pin
IN_{ts}	TTL level input pin and schmitt trigger
AIN	Input pin(Analog)

FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

The MON35W82 provides 6 analog positive inputs, 3 fan speed monitor inputs, 2 PWM (Pulse Width Modulation) output controls, 2 sets for fan PWM (Pulse Width Modulation) control, 2 thermal inputs from remote thermistors or 2N3904 transistors or Penitum™ II (Deschutes) thermal diode outputs, a beep function output and a monitor function for the voltage, temperature and fan counters. Once the monitor function is initiated, the watchdog monitors each function and stores the value. If the monitored value is not within the limits values, the interrupt status is set and an interrupt can be generated.

Access Interface

The MON35W82 provides an I^2C Serial Bus to read/write internal registers. There are two serial bus address registers, CR[48h] and CR[4Ah] used to read/write all of the internal registers. CR[48h] (default value 0101101) is used to access all registers excluding the Bank 1 temperature sensor registers. CR[4Ah] (default value 1001001)is used to access the Bank 1 temperature sensor registers.

The serial bus access timings are shown in the following figures.

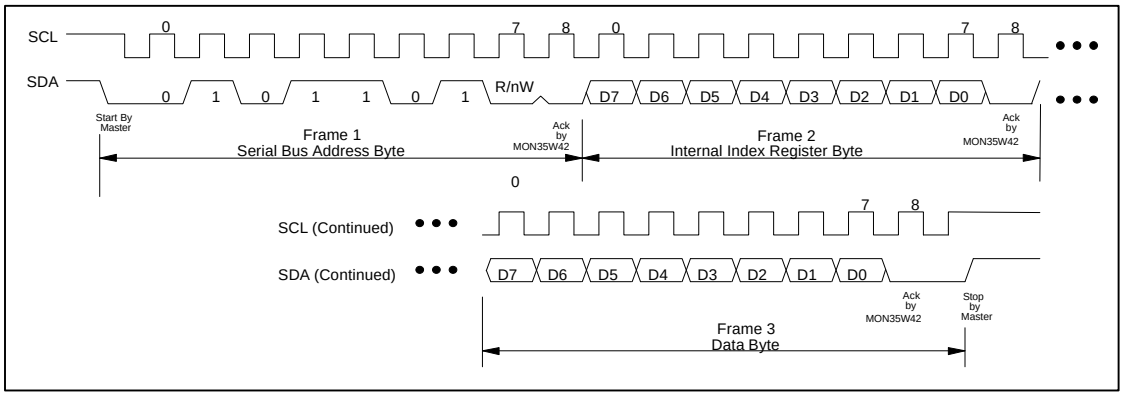


FIGURE 1 - SERIAL BUS WRITE TO INTERNAL ADDRESS REGISTER FOLLOWED BY THE DATA BYTE

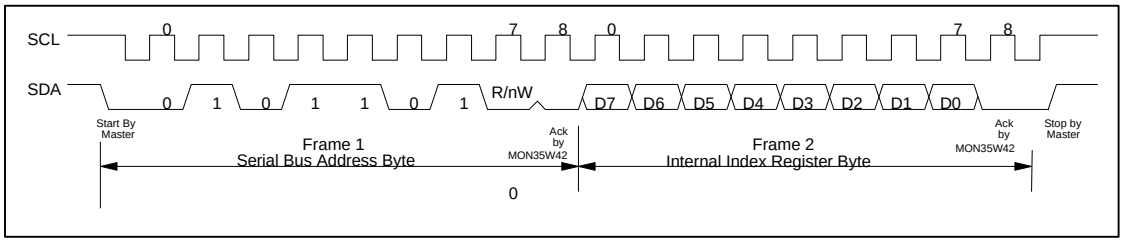


FIGURE 2 - SERIAL BUS WRITE TO INTERNAL ADDRESS REGISTER ONLY

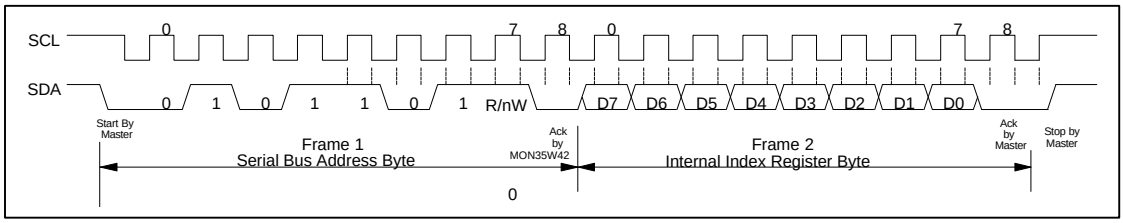


FIGURE 3 - SERIAL BUS READ FROM A REGISTER WITH THE INTERNAL ADDRESS REGISTER PRESET TO DESIRED LOCATION

The serial bus timing of the temperature 2 and 3 is shown below:

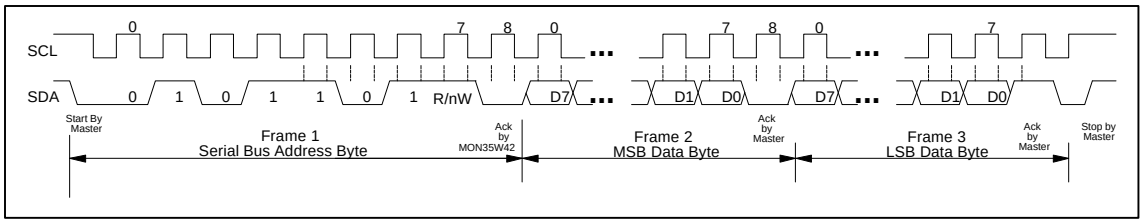


FIGURE 4 - TYPICAL 2-BYTE READ FROM PRESET POINTER LOCATION (TEMP, T_{OS}, T_{HYST})

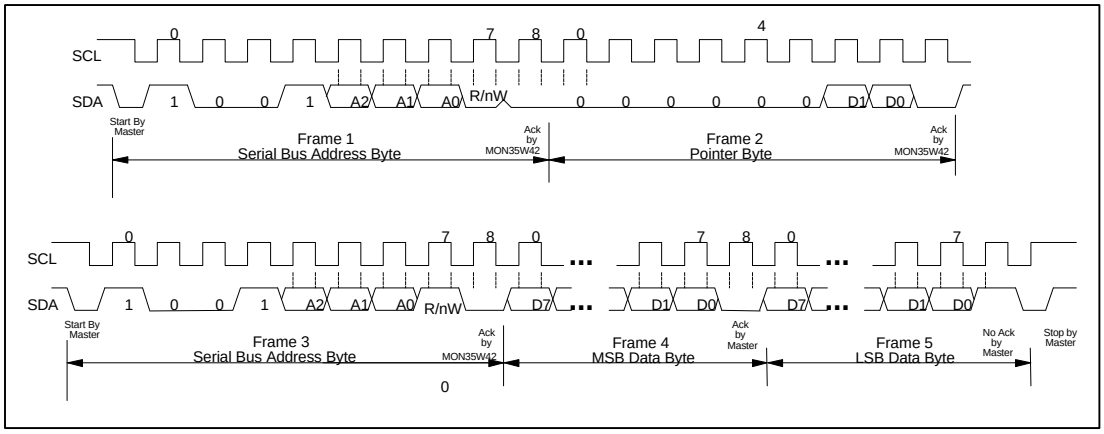


FIGURE 5 - TYPICAL POINTER SET FOLLOWED BY IMMEDIATE READ FOR 2-BYTE REGISTER (TEMP, T_{OS}, T_{HYST})

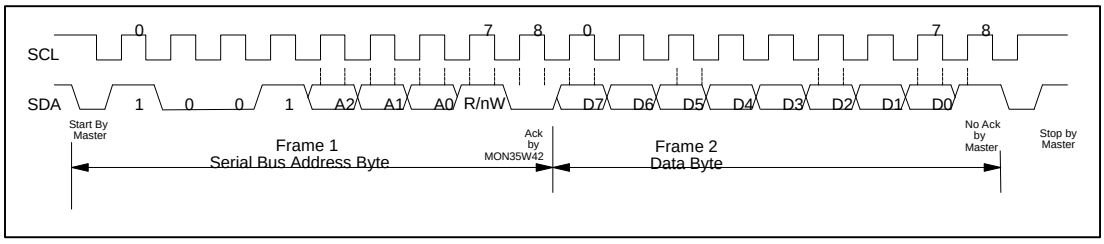


FIGURE 6 - TYPICAL READ 1-BYTE FROM CONFIGURATION REGISTER WITH PRESET POINTER

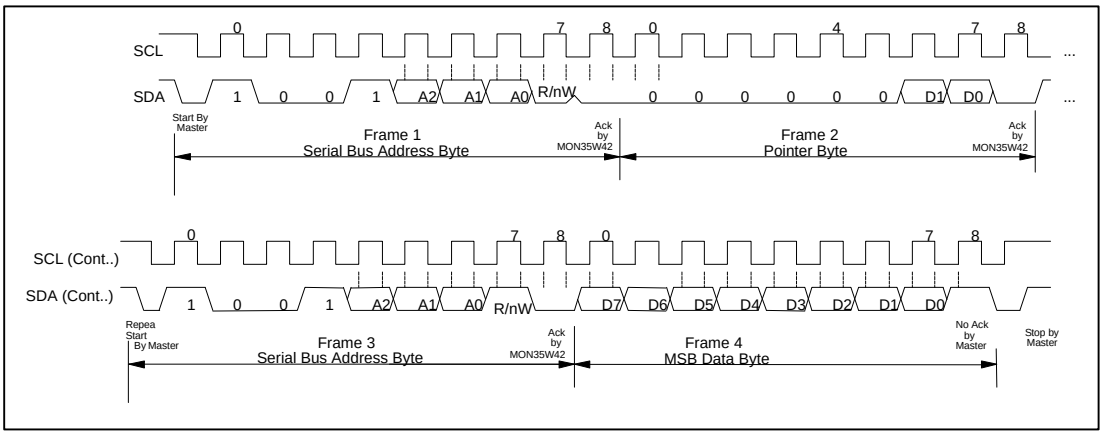


FIGURE 7 - TYPICAL POINTER SET FOLLOWED BY IMMEDIATE READ FROM CONFIGURATION REGISTER

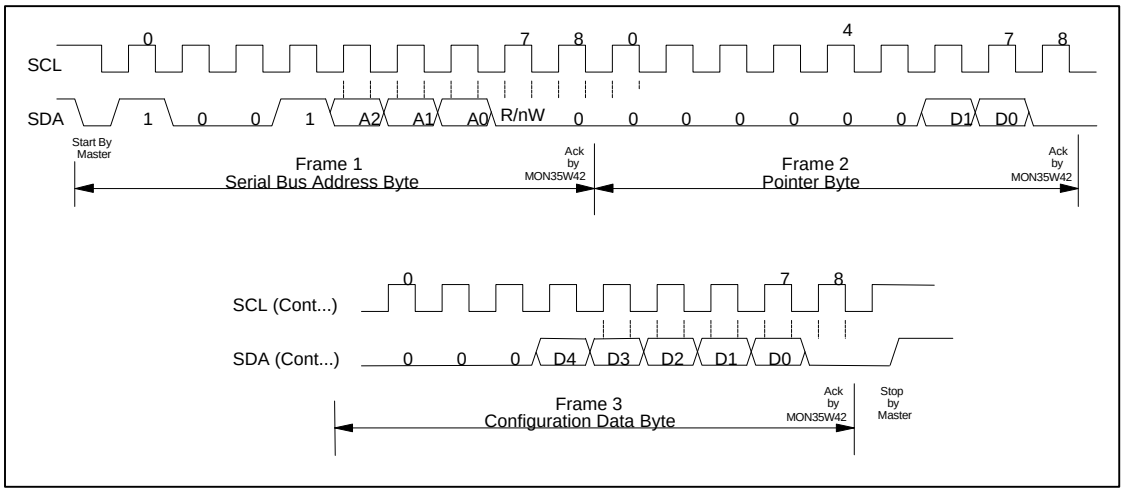


FIGURE 8 - TEMPERATURE 2/3 CONFIGURATION REGISTER WRITE

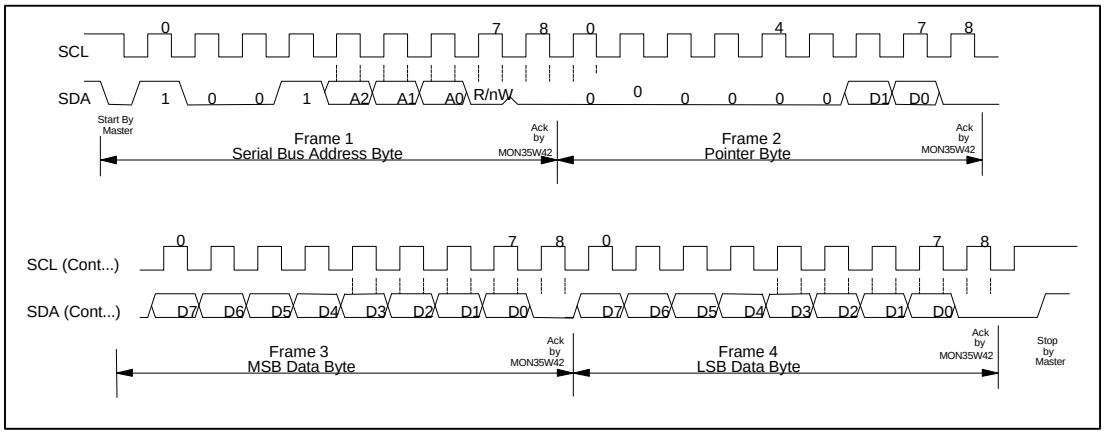


FIGURE 9 - TEMPERATURE 2/3 T_{OS} AND T_{HYST} WRITE

ANALOG INPUTS

The analog inputs are normally used to monitor the PC power supplies. The 8-bit ADC has a 16mv LSB and supports an input range of 0V to 4.096V. The CPU V-core, 3.3V and battery voltage can be directly connected to these analog inputs. Voltages higher than 4.096V must be reduced to the specified input range. An example using external resistors is shown in Figure 10.

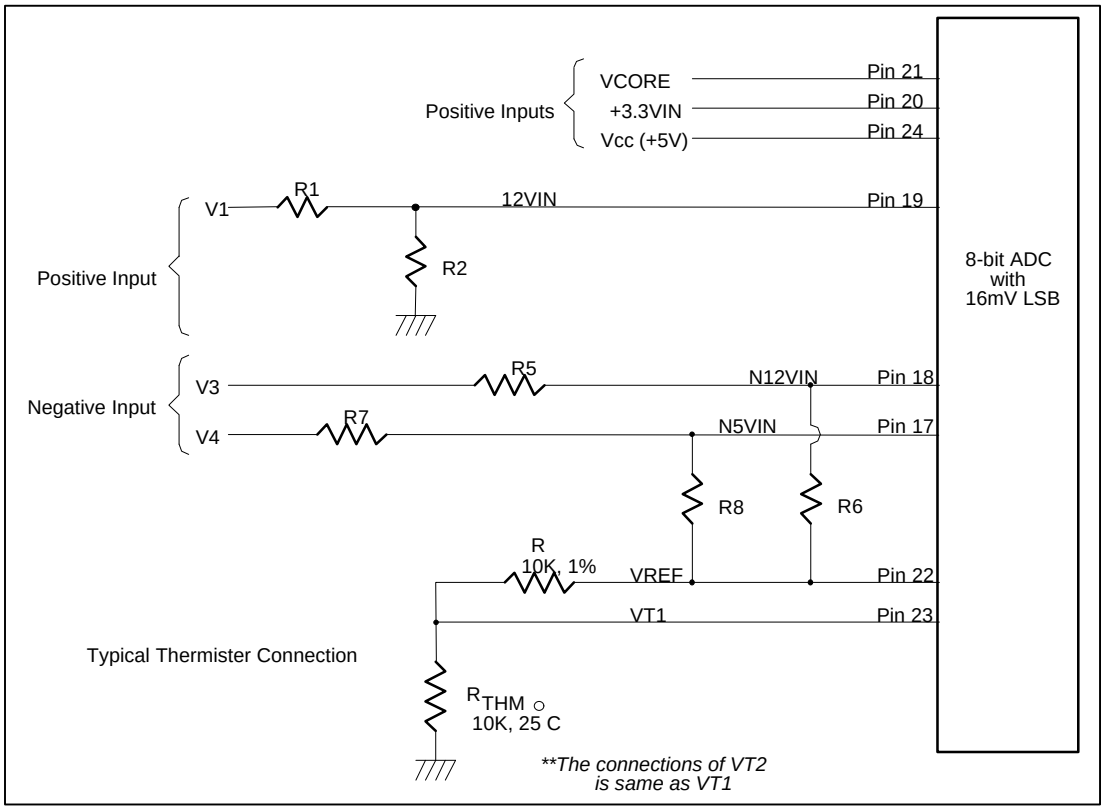


FIGURE 10

Monitor over 4.096V voltage:

The input voltage +12VIN can be expressed as following equation.

$$12VIN = V_1 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected as 28K Ohms and 10K Ohms, respectively, when the input voltage V1 is 12V. The node voltage of +12VIN must be less than 4.096V for the maximum input range of the 8-bit ADC. The Vcc Pin (Pin 24) is connected to the power supply VCC (+5V). There are two functions in this pin. The first function is to supply internal analog power in the MON35W82 and the second function is to monitor this voltage. The Vcc Pin is connected to internal serial resistors to monitor the +5V voltage. The value of two serial resistors are 34K ohms and 50K ohms so that the input voltage to the ADC is 2.98V which is less than 4.096V of ADC maximum input voltage. The voltage equation can be represented as follows.

$$V_{in} = VCC \times \frac{50K\Omega}{50K\Omega + 34K\Omega} \cong 2.98V$$

where VCC is set to 5V.

Monitor negative voltage:

The negative voltage should be connected to two series resistors and a positive voltage VREF (equal to 3.6V). In Figure 10, voltages V3 and V4 are two negative voltages, -12V and -5V respectively. The voltage V3 is connected to two series resistors and then is connected to VREF which is a positive voltage. The voltage on node N12VIN must be between 0V and 4.096V. If R5=232K ohms and R6=56K ohms, the input voltage of node N12VIN can be calculated as follows:

$$N12VIN = (VREF + |V_3|) \times (\frac{232K\Omega}{232K\Omega + 56K\Omega}) + V_3$$

where VREF is equal 3.6V.

If the V_3 is equal to -12V then the voltage is equal to 0.567V and the converted hexadecimal data is set to 35h by the 8-bit ADC with 16mV-LSB.This monitored value should be converted to the real negative voltage and the express equation is shown as follows.

$$V_3 = \frac{N12VIN - VREF \times b}{1 - b}$$

Where b is 232K/(232K+56K). If the N2VIN is 0.567 then the V3 is approximately equal to -12V.

The another negative voltage input V6 (approximate -5V) can also be evaluated by a similar method and the serial resistors can be selected with R7=120K ohms and R8=56K ohms. The expression equation of V6 With -5V voltage is shown as follows.

$$V_6 = \frac{N5VIN - VREF \times g}{1 - g}$$

Where the Υ is set to 120K/(120K+56K). If the monitored ADC value in the N5VIN channel is 0.8635, VREF=3.6V and the parameter Υ is 0.6818 then the negative voltage of V6 can be evaluated to be -5V.

Monitor temperature from thermistor:

The MON35W82 can connect to three thermistors to measure three different environmental temperatures. The specification of the thermistors are (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In Figure 10, the thermistor R_{THM} is connected to VT1 and VT1 is connected through a 10K ohm series resistor to VREF.

Monitor temperature from Pentium II™ thermal diode or bipolar transistor 2N3904

The MON35W82 can interface to the Pentium II™ (Deschutes) thermal diode interface or a 2N3904 transistor. The circuit connection is shown in Figure 11. The Pentium II™ D- pin is connected to ground (GND) and the D+ pin is connected to the PII1 or PII2 pin of the MON35W82. A 30K-ohm resistor must be connected from the PIIx pin to the VREF pin to supply the diode bias current and a bypass capacitor C=3300pF must be added to filter the high frequency noise. If a 2N3904 transistor is used, the Base (B) and Collector (C) must be tied together to act as a thermal diode.

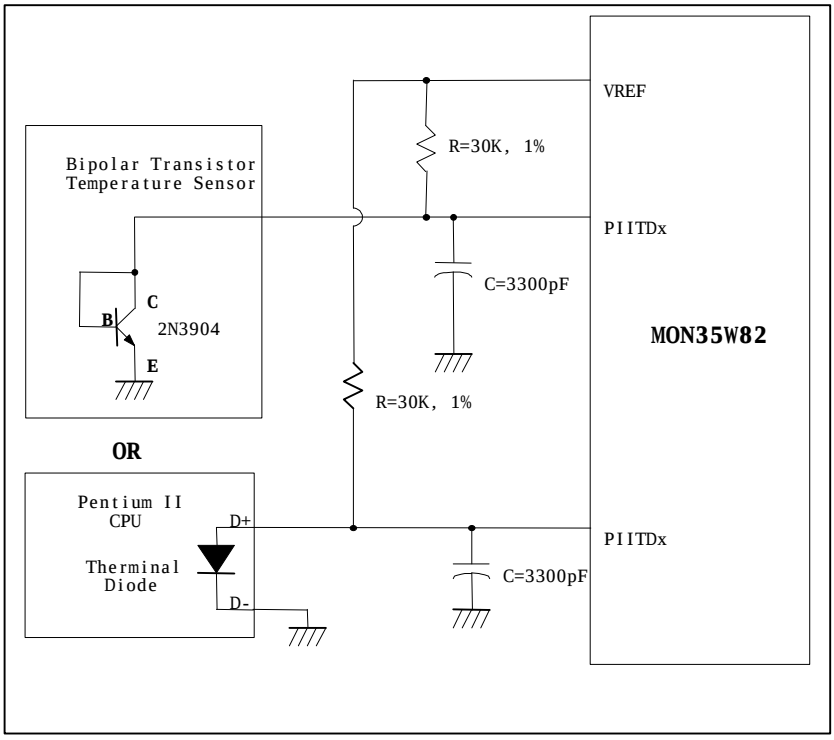


FIGURE 11

FAN Speed Count and FAN Speed Control

Fan Speed Count

Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and the maximum input voltage can not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown in Figure 12.

Determine the fan counter according to:

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

Once the fan speed counter has been read from register CR28, CR29 or CR2A, the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR47.bit7:4, CR4B.bit7:6, and Bank0 CR5D.bit5:7 which are three bits for the divisor. These provide support for very low speed fans such as power supply fans. The followed table is an example for the relation of divisor, RPM, and count.

DIVISOR	NOMINAL RPM	TIME PER REVOLUTION	COUNTS	70% RPM	TIME FOR 70%
1	8800	6.82 ms	*153*	6160	9.74 ms
2 (default)	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms
16	550	109.08 ms	*153*	385	155.84 ms
32	275	218.16 ms	*153*	192	311.68 ms
64	137	436.32 ms	*153*	96	623.36 ms
128	68	872.64 ms	*153*	48	1246.72 ms

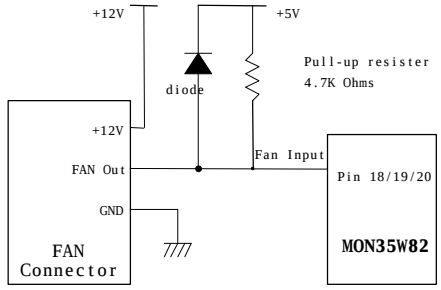


Figure 12A - Fan with Tach Pull-Up to +5V

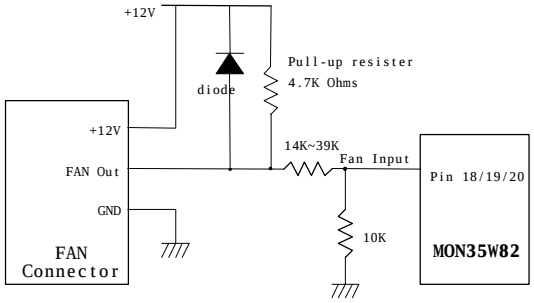


Figure 12B - Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Register Attenuator

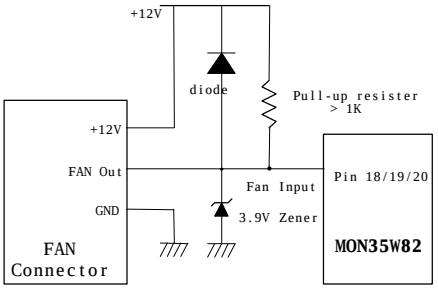


Figure 12C - Fan with Tach Pull-Up to +12V and Zener Clamp

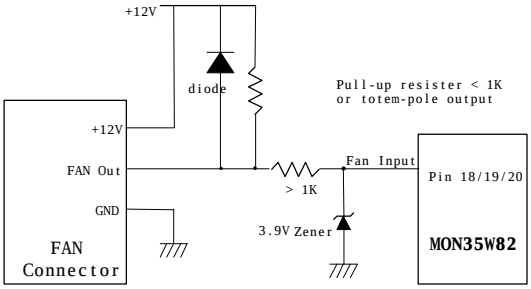


Figure 12D - Fan with Tach Pull-Up to +12V, or Totem-Pole Putput and Zener Clamp

Fan Speed Control

The MON35W82 provides four pins for fan PWM speed control. The duty cycle of the PWM can be programmed by an 8-bit register which is defined in Bank0 CR5A and CR5B. The default duty cycle is set to 100%, that is, the default 8-bit register is set to FFh. The duty cycle can be represented as follows:

$$\text{Duty cycle}(\%) = \frac{\text{Programmed 8-bit Register Value}}{255} \times 100\ \%$$

The PWM clock frequency also can be program and defined in the Bank0.CR5C. The application circuit is shown in Figure 13.

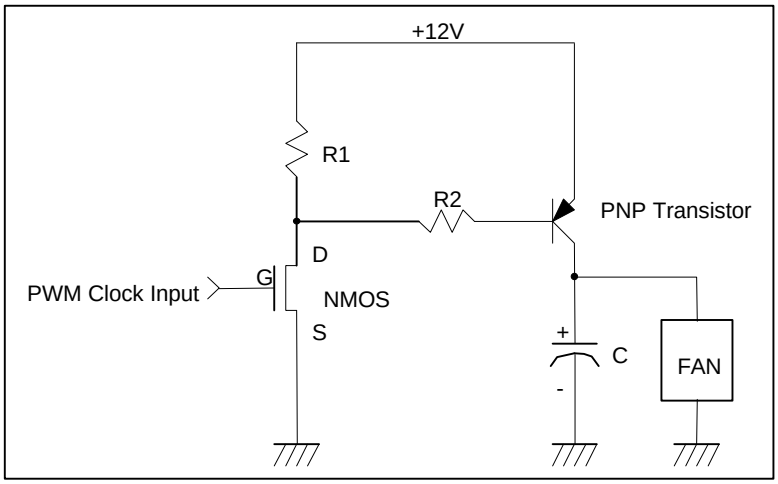


FIGURE 13

Temperature Measurement Machine

The temperature data format is 8-bit two's-complement for sensor 2 and 9-bit two -complement for sensor 1. The 8-bit temperature data can be obtained by reading CR[27h]. The 9-bit temperature data can be obtained by reading the 8 MSBs from the Bank1 CR[50h] and the LSB from the Bank1 CR[51h] bit 7. The format of the temperature data is show in the following table.

	8-BIT DIGITAL OUTPUT		**9-BIT DIGITAL OUTPUT**	
TEMPERATURE	8-Bit Binary	8-Bit Hex	9-Bit Binary	9-Bit Hex
+125øC	0111,1101	7Dh	0,1111,1010	0FAh
+25øC	0001,1001	19h	0,0011,0010	032h
+1øC	0000,0001	01h	0,0000,0010	002h
+0.5øC	-	-	0,0000,0001	001h
+0øC	0000,0000	00h	0,0000,0000	000h
-0.5øC	-	-	1,1111,1111	1FFh
-1øC	1111,1111	FFh	1,1111,1110	1FFh
-25øC	1110,0111	E7h	1,1100,1110	1CEh
-55øC	1100,1001	C9h	1,1001,0010	192h

Temperature Sensor 2 Interrupt Mode

The MON35W82 temperature sensor 2 nSMI interrupt has two modes:

(1) Comparator Interrupt Mode

Setting the T_{HYST} (Temperature Hysteresis) limit to 127øC will set temperature sensor 2 nSMI to the Comparator Interrupt Mode. Temperatures which exceed T_O (Over Temperature) Limit cause an interrupt and this interrupt will be reset by reading the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_O, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_O. (Figure 14A)

(2) Two-Times Interrupt Mode

Setting the T_{HYST} lower than T_O will set temperature sensor 2 nSMI to the Two-Times Interrupt Mode. Temperatures exceeding T_O causes an interrupt and then the temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 14B)

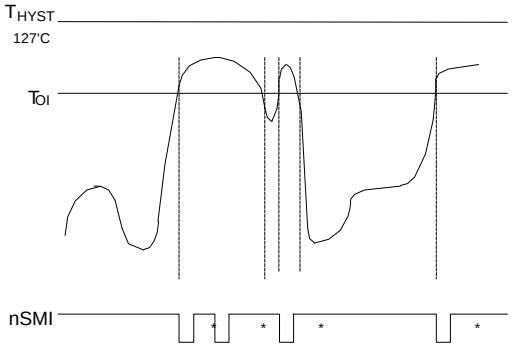


Figure 14A - Comparator Interrupt Mode

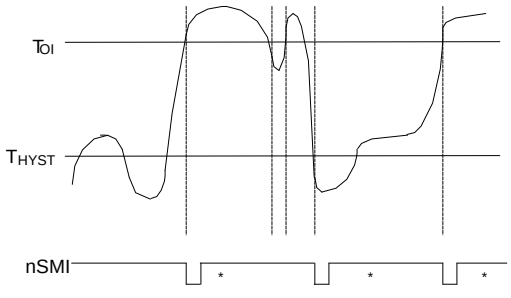


Figure 14B - Two-Times Interrupt Mode

*Interrupt Reset when Interrupt Status Registers are read

Temperature Sensor 1 Interrupt Mode

The MON35W82 temperature sensor 1 nSMI interrupt has three modes

(1) Comparator Interrupt Mode

Temperatures exceeding T_O cause an interrupt and this interrupt will be reset by reading the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupt continues to occur in this manner until the temperature goes below T_{HYST}. (Figure 15A)

(2) Two-Times Interrupt Mode

The temperature exceeding T_O causes an interrupt and then the temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 15B)

(3) One-Time Interrupt Mode

The temperature exceeding T_O causes an interrupt and then the temperature going below T_{HYST} will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below $T_{HYST,}$ an interrupt will not occur again until the temperature exceeds T_O. (Figure 15C)

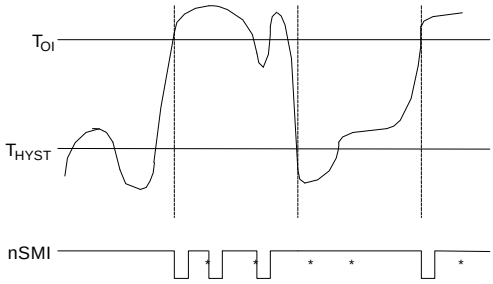


Figure 15A - Comparator Interrupt Mode

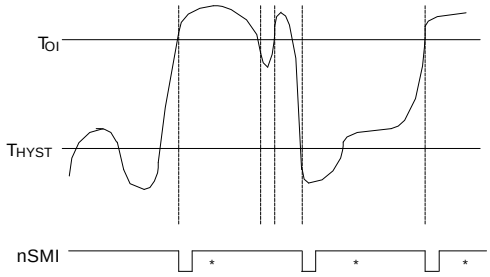


Figure 15B - Two-Times Interrupt Mode

*Interrupt Reset when Interrupt Status Registers are read

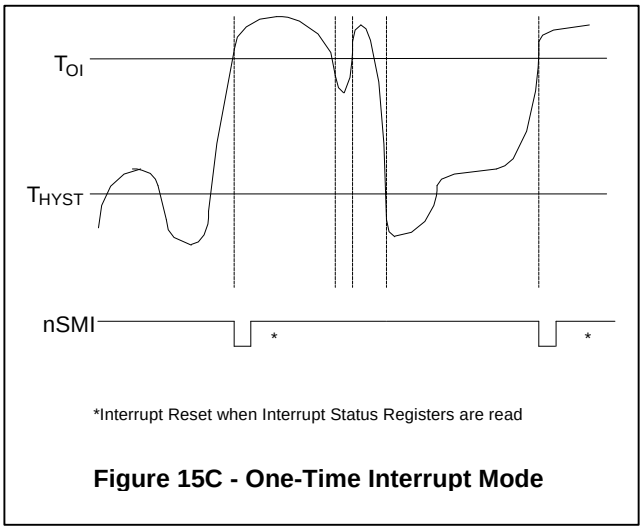


Figure 15C - One-Time Interrupt Mode

Temperature sensor 1
Over-Temperature (nOVT) Modes

(1) Comparator Mode:

Setting Bank1 CR[52h] bit 2 to 0 will set nOVT signal to comparator mode. The temperature exceeding T_O causes the nOVT output activated until the temperature is less than T_{HYST}. (Figure 16)

(2) Interrupt Mode:

Setting Bank1 CR[52h] bit 2 to 1 will set nOVT signal to interrupt mode. Setting Temperature exceeding T_O causes the nOVT output activated indefinitely until reset by reading temperature sensor 2 or sensor 3 registers. The temperature exceeding T_O, then nOVT reset, and then temperature going below T_{HYST} will also cause the nOVT activated indefinitely until reset by reading temperature sensor 2 or sensor 3 registers. Once the nOVT is activated by exceeding T_O , then reset, if the temperature remains above T_{HYST}, the nOVT will not be activated again.(Figure 16)

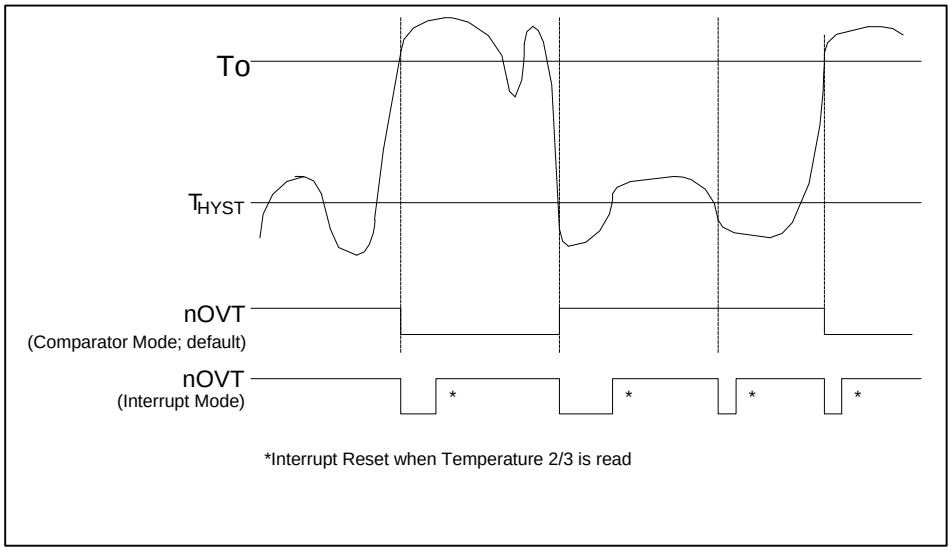


FIGURE 16 – OVER-TEMPERATURE RESPONSE DIAGRAM

Voltage and Fan nSMI mode

Voltage nSMI mode:

nSMI interrupt for voltage monitoring is Two-Times Interrupt Mode. Voltage exceeding the high limit or going below the low limit will cause an interrupt if the previous interrupt has been reset by reading the interrupt Status Register. (Figure 17)

Fan nSMI mode:

nSMI interrupt for fan monitoring is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit, will causes an interrupt if the previous interrupt has been reset by reading the interrupt Status Register. (Figure 17)

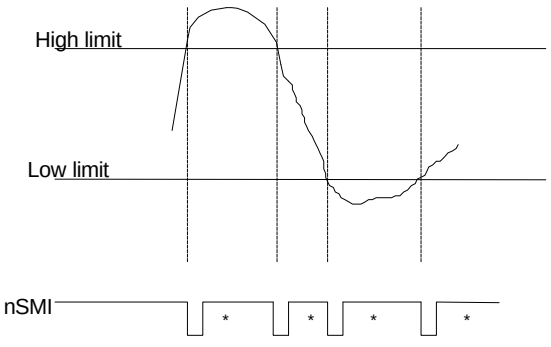


Figure 17A - Voltage nSMI Mode

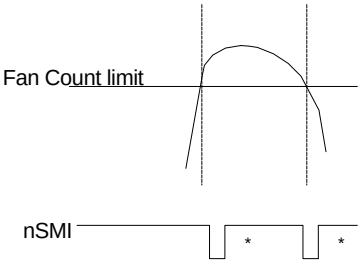


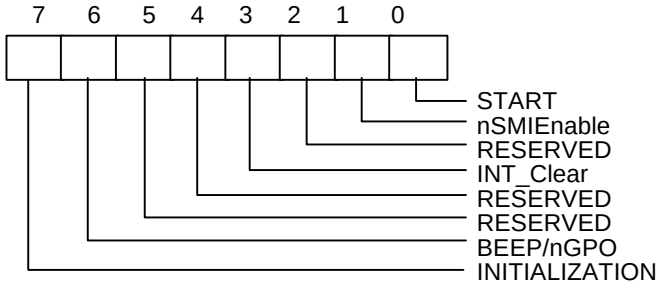
Figure 17B - Fan nSMI Mode

*Interrupt Reset when Interrupt Status Registers are read

REGISTERS AND RAM

Configuration Register - Index 40h

Register Location:	40h
Power on Default Value	00000001 binary
Attribute:	Read/write
Size:	8 bits

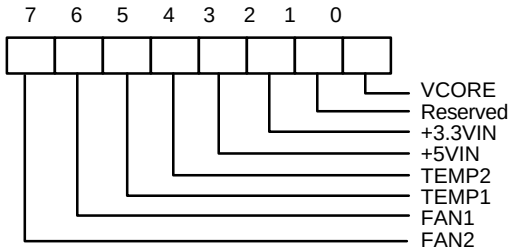


Bit 7: A one restores power on default values to all registers except the Serial Bus Address register. This bit clears itself since the power on default is zero.
Bit 6: A one drives a zero on BEEP/nGPO pin.
Bit 5: Reserved
Bit 4: Reserved
Bit 3: A one disables the nSMI output without affecting the contents of the Interrupt Status Registers. The device will stop monitoring. It will resume monitoring when this bit is cleared.
Bit 2: Reserved
Bit 1: A one enables the nSMI Interrupt output.
Bit 0: A one enables startup of monitoring operations, a zero puts the part in standby mode.

Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

Interrupt Status Register 1 - Index 41h

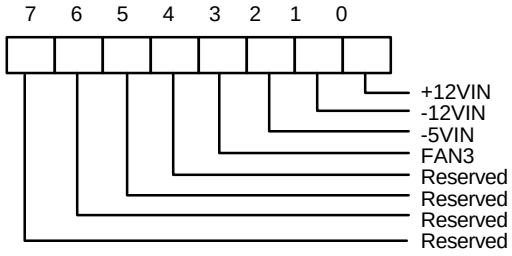
Register Location:	41h
Power on Default Value	00h
Attribute:	Read Only
Size:	8 bits



Bit 7: A one indicates the fan count limit of FAN2 has been exceeded.
Bit 6: A one indicates the fan count limit of FAN1 has been exceeded.
Bit 5: A one indicates a High limit of VT1 has been exceeded from temperature sensor.
Bit 4: A one indicates a High limit of VT2 has been exceeded from temperature sensor.
Bit 3: A one indicates a High or Low limit of +5VIN has been exceeded.
Bit 2: A one indicates a High or Low limit of +3.3VIN has been exceeded.
Bit 1: Reserved.
Bit 0: A one indicates a High or Low limit of VCORE has been exceeded.

Interrupt Status Register 2 - Index 42h

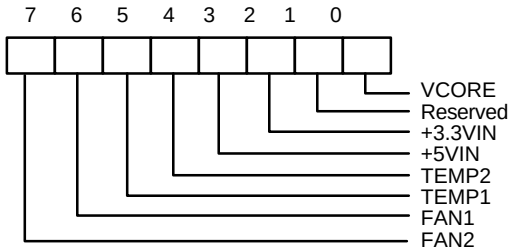
Register Location:	42h
Power on Default Value	00h
Attribute:	Read Only
Size:	8 bits



Bit 7-4: Reserved.This bit should be set to 0.
Bit 3: A one indicates the fan count limit of FAN3 has been exceeded.
Bit 2: A one indicates a High or Low limit of -5VIN has been exceeded.
Bit 1: A one indicates a High or Low limit of -12VIN has been exceeded.
Bit 0: A one indicates a High or Low limit of +12VIN has been exceeded.

nSMI Mask Register 1 - Index 43h

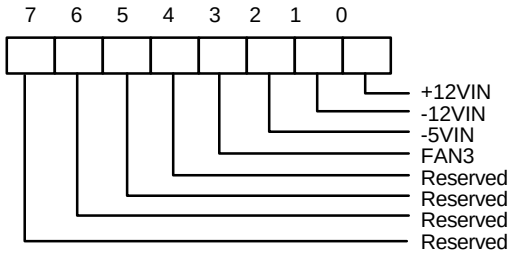
Register Location:	43h
Power on Default Value	00h
Attribute:	Read/Write
Size:	8 bits



Bit 7-0: A one disables the corresponding interrupt status bit for nSMI interrupt.

nSMI Mask Register 2 - Index 44h

Register Location:	44h
Power on Default Value	00h
Attribute:	Read/Write
Size:	8 bits

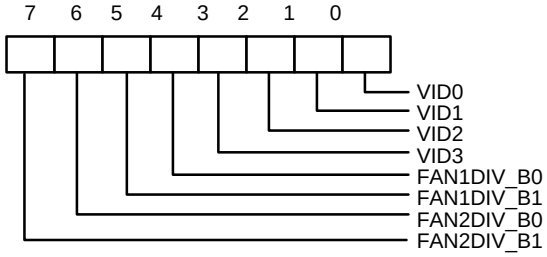


Bit 7-4: Reserved. This bit should be set to 0.
Bit 3-0: A one disables the corresponding interrupt status bit for nSMI interrupt.

Reserved Register — Index 45h-- 46h

VID/Fan Divisor Register - Index 47h

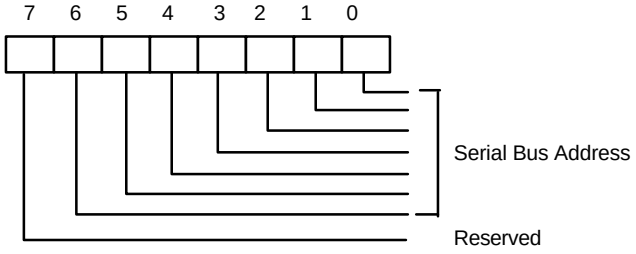
Register Location: 47h
Power on Default Value <7:4> is 0101, <3:0> is mapped to VID<3:0>
Attribute: Read/Write
Size: 8 bits



Bit 7-6: FAN2 Speed Control.
Bit 5-4: FAN1 Speed Control.
Bit 3-0: The VID <3:0> inputs
Note: Please refer to Bank0 CR[5Dh] , Fan divisor table.

Serial Bus Address Register - Index 48h

Register Location: 48h
Power on Default Value Serial Bus address <6:0> = 0101101 and <7> = 0 binary
Size: 8 bits



Bit 7: Read Only - Reserved.
Bit 6-0: Read/Write - Serial Bus address <6:0>.

Value RAM — Index 20h- 3Fh or 60h - 7Fh

INDEX	DESCRIPTION
20h or 60h	VCORE reading
21h or 61h	Reserved
22h or 62h	+3.3VIN reading
23h or 63h	+5VIN reading
24h or 64h	+12VIN reading
25h or 65h	-12VIN reading
26h or 66h	-5VIN reading
27h or 67h	Temperature sensor 2 (VT2) reading
28h or 68h	FAN1 reading **Note:** This location stores the number of counts of the internal clock per revolution.
29h or 69h	FAN2 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Ah or 6Ah	FAN3 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Bh or 6Bh	VCORE High Limit, default value is defined by Vcore Voltage +0.2v.
2Ch or 6Ch	VCORE Low Limit, default value is defined by Vcore Voltage - 0.2v.
2Dh or 6Dh	Reserved
2Eh or 6Eh	Reserved
2Fh or 6Fh	+3.3VIN High Limit
30h or 70h	+3.3VIN Low Limit
31h or 71h	+5VIN High Limit
32h or 72h	+5VIN Low Limit

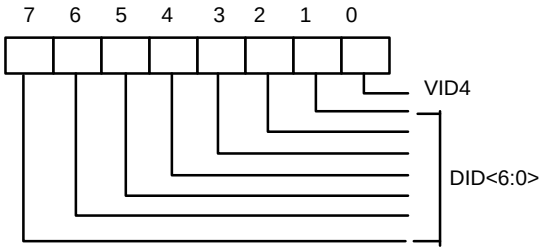
Value RAM — Index 20h- 3Fh or 60h - 7Fh, continued

ADDRESS A6-A0	DESCRIPTION
33h or 73h	+12VIN High Limit
34h or 74h	+12VIN Low Limit
35h or 75h	-12VIN High Limit
36h or 76h	-12VIN Low Limit
37h or 77h	-5VIN High Limit
38h or 78h	-5VIN Low Limit
39h or 79h	Temperature sensor 2 (VT2) High Limit
3Ah or 7Ah	Temperature sensor 2 (VT2) Hysteresis Limit
3Bh or 7Bh	FAN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Ch or 7Ch	FAN2 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Dh or 7Dh	FAN3 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3E- 3Fh or 7E-7Fh	Reserved

Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will never be generated except the case when voltages go below the low limits.

Voltage ID (VID4) & Device ID - Index 49h

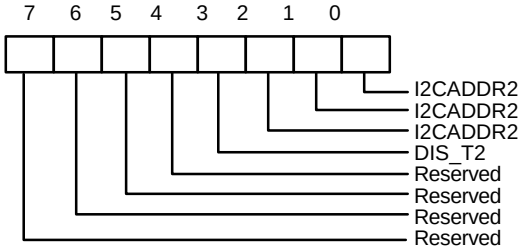
Register Location:	49h
Power on Default Value	<7:1> is 000,0001b <0> is mapped to VID <4>
Size:	8 bits



Bit 7-1: Read Only - Device ID<6:0>
Bit 0 : Read/Write - The VID4 inputs.

Temperature 2 and Temperature 3 Serial Bus Address Register--Index 4Ah

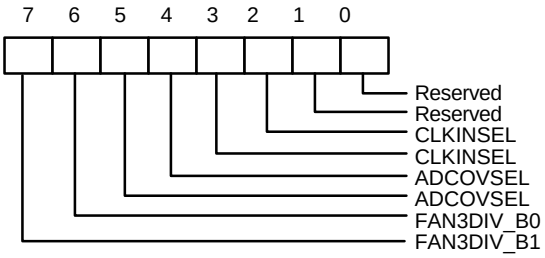
Register Location:	4Ah
Power on Default Value	<7:0> = 0000,0001 binary. Reset by MR
Attribute:	Read/Write
Size:	8 bits



Bit 7-4 : Reserved
Bit 3: Set to 1, disable temperature Sensor 1 and can not access any data from Temperature Sensor 1.
Bit 2-0: Temperature 2 Serial Bus Address. The serial bus address is 1001xxx. Where xxx are defined in these bits.

Pin Control Register - Index 4Bh

Register Location:	4Bh
Power on Default Value	<7:0> 44h. Reset by MR.
Attribute:	Read/Write
Size:	8 bits



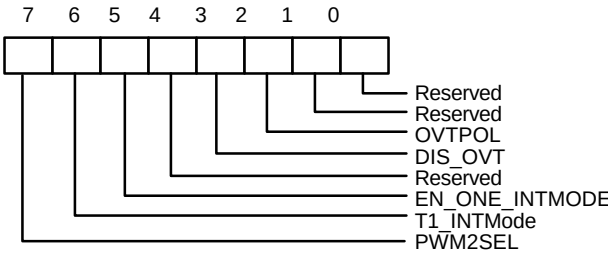
Bit 7-6:Fan3 speed divisor.
Please refer to Bank0 CR[5Dh] , Fan divisor table.

Bit 5-4: Select A/D Converter Clock Input.
<5:4> = 00 - Default. ADC clock select 22.5 kHz
<5:4> = 01- ADC clock select 5.6 kHz. (22.5K/4)
<5:4> = 10 - ADC clock select 1.4kHz. (22.5K/16)
<5:4> = 11 - ADC clock select 0.35 kHz. (22.5K/64)

Bit 3-2: Clock Input Select.
<3:2> = 00 - Pin 3 (CLKIN) select 14.318MHz clock.
<3:2> = 01 - Default. Pin 3 (CLKIN) select 24MHz clock.
<3:2> = 10 - Pin 3 (CLKIN) select 48MHz clock .
<3:2> = 11 - Reserved. Pin3 no clock input.
Bit 1-0: Reserved. User defined.

nIRQ/nOVT Property Select - Index 4Ch

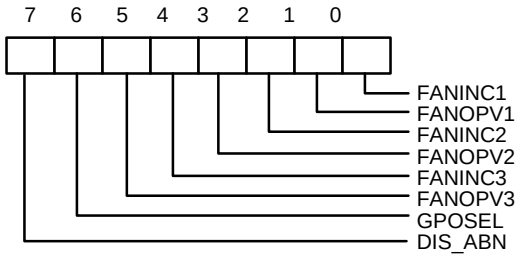
Register Location: 4Ch
Power on Default Value <7:0> --0000,0001. Reset by MR.
Attribute: Read/Write
Size: 8 bits



Bit 7: Set to 1 , select pin 9 nSMI/PWMOUT2 as PWM output. Set to 0, select pin 9 as nSMI output.
Bit6: Set to 1, the nSMI output type of temperature sensor 1 is set to Comparator Interrupt mode. Set to 0, the nSMI output type is set to Interrupt mode (defined by CR[4Ch] Bit 5).
Bit 5: Set to 1, the nSMI output type of temperature sensor 1 is set to One-Time interrupt mode. Set to 0, the nSMI output type of temperature sensor 1 is set to Two-Times interrupt mode.
Bit 4 : Reserved. User Defined.
Bit 3: Disable temperature sensor 1 over-temperature (OVT) output if set to 1. Default 0, enable OVT1 output through pin nOVT.
Bit 2: Over-temperature polarity. Write 1, nOVT active high. Write 0, nOVT active low. Default 0.
Bit 1-0: Reserved. User Defined.

FAN IN/OUT and BEEP/nGPO Control Register - Index 4Dh

Register Location:	4Dh
Power on Default Value	<7:0> 0001,0101. Reset by MR.
Attribute:	Read/Write
Size:	8 bits



Bit 7: Disable power-on abnormal voltage monitoring including V-Core A and +3.3V. If these voltages exceed the limit value, the BEEP pin (Open Drain) will drive a 300Hz or 600Hz frequency signal. Write 1, the frequency will be disable. Default 0. After power on, the system should set this bit to 1 in order to disable BEEP.

Bit 6: BEEP/nGPO Pin Function Select. Write 1 Select nGPO function. Set 0, select BEEP function. This bit defaults to 0.

Bit 5: FAN 3 output value if FANINC3 is set to 0. If this bit is a 1, then pin 4 always generates a logic high signal. If this bit is a 0, pin 4 always generates logic low signal. This bit defaults to 0.

Bit 4: FAN 3 Input Control. Set to 1(default), pin 4 acts as FAN clock input. Set to 0, pin 4 acts as FAN control signal and the output value of FAN control is set by register bit 5. This output pin can connect to power PMOS gate to control FAN ON/OFF.

Bit 3: FAN 2 output value if FANINC2 is set to 0. If this bit is 1, then pin 3 always generates a logic high signal. If 0 (default), pin 3 always generates a logic low signal.

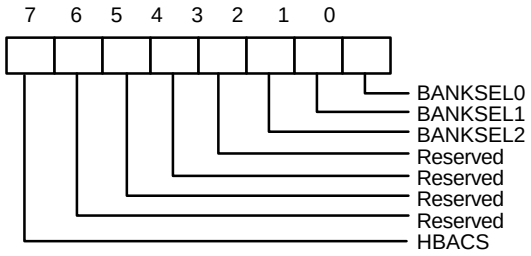
Bit 2: FAN 2 Input Control. Set to 1(default), pin 3 acts as FAN clock input. Set to 0, pin 3 acts as FAN control signal and the output value of FAN control is set by this register bit 3. This output pin can connect to power NMOS gate to control FAN ON/OFF.

Bit 1: FAN 1 output value if FANINC1 is sets to 0. If 1, then pin 2 always generates a logic high signal. If 0(default), pin 2 always generates a logic low signal.

Bit 0: FAN 1 Input Control. Set to 1(default), pin 2 acts as FAN clock input. Set to 0, pin 2 acts as FAN control signal and the output value of FAN control is set by register bit 1. This output pin can connect to power PMOS gate to control FAN ON/OFF.

Register 50h ~ 5Fh Bank Select - Index 4Eh

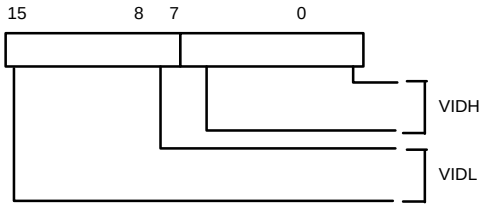
Register Location:	4Eh
Power on Default Value	<6:3> = Reserved, <7> = 1, <2:0> = 0. Reset by MR
Attribute:	Read/Write
Size:	8 bits



Bit 7: HBACS- High byte access. Set to 1(default), access Register 4Fh high byte register. Set to 0, access Register 4Fh low byte register.
Bit 6-3: Reserved. This bit should be set to 0.
Bit 2-0: Index ports 0x50~0x5F Bank select.

SMSC Vendor ID - Index 4Fh

Register Location:	4Fh
Power on Default Value	<15:0> = 5CA3h
Attribute:	Read Only
Size:	16 bits

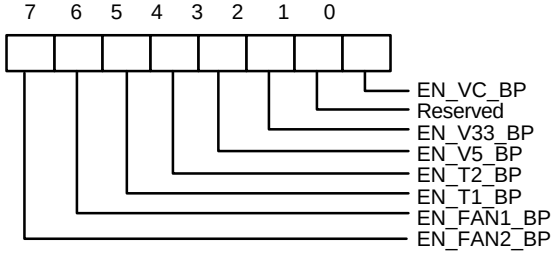


Bit 15-8: Vendor ID High Byte if CR4E.bit7=1. Default 5Ch.
Bit 7-0: Vendor ID Low Byte if CR4E.bit7=0. Default A3h.

SMSC Test Register -- Index 50h - 55h (Bank 0)

BEEP Control Register 1-- Index 56h (*Bank 0*)

Register Location:	56h
Power on Default Value	<7:0> 0000,0000. Reset by MR.
Attribute:	Read/Write
Size:	8 bits



Bit 7: Enable BEEP Output from FAN 2 if the monitor value exceeds the limit value. If set to 1(default) enable BEEP output.

Bit 6: Enable BEEP Output from FAN 1 if the monitor value exceeds the limit value. If set to 1(default), enable BEEP output.

Bit 5: Enable BEEP Output from Temperature Sensor 1 if the monitor value exceeds the limit value. If set to 1, enable BEEP output. Default is 0.

Bit 4: Enable BEEP output for Temperature Sensor 2 if the monitor value exceed the limit value. If set to 1, enable BEEP output. Default is 0

Bit 3: Enable BEEP output from VDD (+5V), If set to 1, enable BEEP output if the monitor value exceeds the limits value. Default is 0, disable BEEP output.

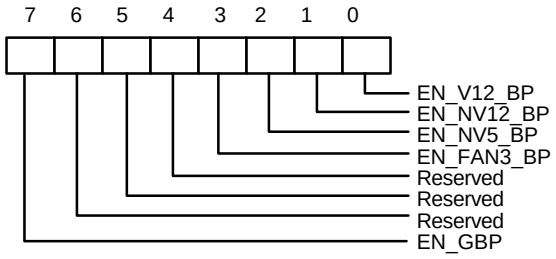
Bit 2: Enable BEEP output from +3.3V. If set to 1(default), enable BEEP output.

Bit 1: Reserved.

Bit 0: Enable BEEP Output from VCORE if the monitor value exceeds the limits value. If set to 1(default), enable BEEP output.

BEEP Control Register 2-- Index 57h (*Bank 0*)

Register Location:	57h
Power on Default Value	<7:0> 1000-0000. Reset by MR.
Attribute:	Read/Write
Size:	8 bits



Bit 7: Enable Global BEEP. If set to 1, enable global BEEP output. Default 1. If set to 0, disable all BEEP outputs.

Bit 6-4: Reserved.

Bit 3: Enable BEEP Output from FAN 3 if the monitor value exceeds the limit value. If set to 1, enable BEEP output. Default 0.

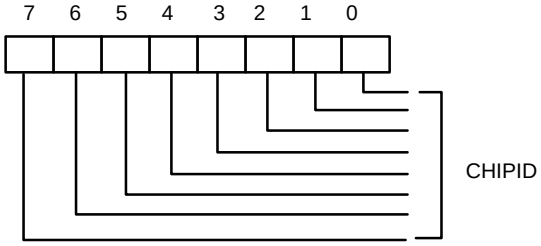
Bit 2: Enable BEEP output from -5V, If set to 1, enable BEEP output if the monitor value exceeds the limits value. Default 0, disable BEEP output.

Bit 1: Enable BEEP output from -12V, If set to 1, enable BEEP output if the monitor value exceeds the limits value. Default 0, disable BEEP output.

Bit 0: Enable BEEP output from +12V, If set to 1, enable BEEP output if the monitor value exceed the limits value. Default 0, disable BEEP output.

Chip ID -- Index 58h (*Bank 0*)

Register Location:	58h
Power on Default Value	<7:0> 0100-0000. Reset by MR.
Attribute:	Read Only
Size:	8 bits

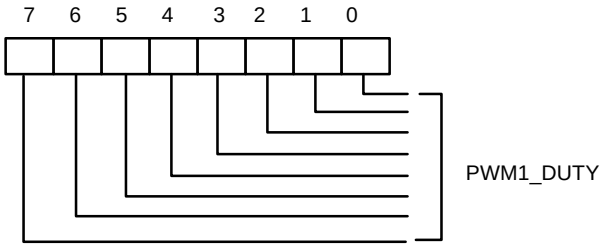


Bit 7: SMSC Chip ID number. Read this register will return 40h.

Reserved Register -- Index 59h (*Bank 0*)

PWMOUT1 Control Register -- Index 5Ah (*Bank 0*)

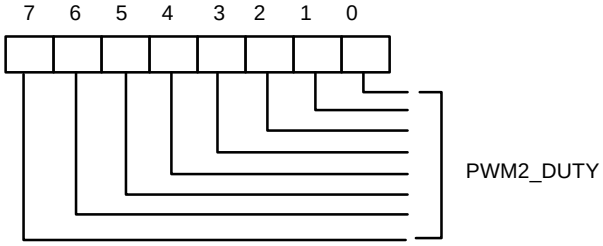
Register Location:	5Ah
Power on default value:	<7:0> 1111-1111. Reset by MR.
Attribute:	Read/Write
Size:	8 bits



Bit 7: PWMOUT1 duty cycle control
If “FF”, Duty cycle is 100%, If “00”, Duty cycle is 0%.

PWMOUT2 Control Register -- Index 5Bh (*Bank 0*)

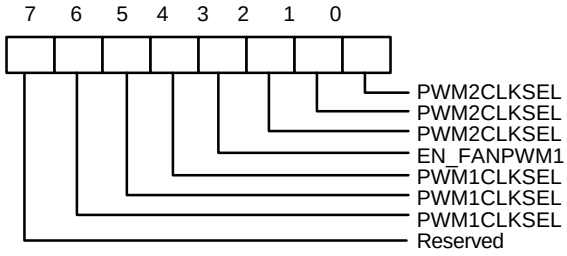
Register Location: 5Bh
Power on default value: <7:0> 1111-1111. Reset by MR.
Attribute: Read/Write
Size: 8 bits



Bit 7: PWMOUT2 duty cycle control
IF “FF”, Duty cycle is 100%,
IF “00”, Duty cycle is 0%.

PWMOUT1/2 Clock Select Register -- Index 5Ch (*Bank 0*)

Register Location: 5Ch
Power on Default Value <7:0> 0001-0001. Reset by MR.
Attribute: Read/Write
Size: 8 bits

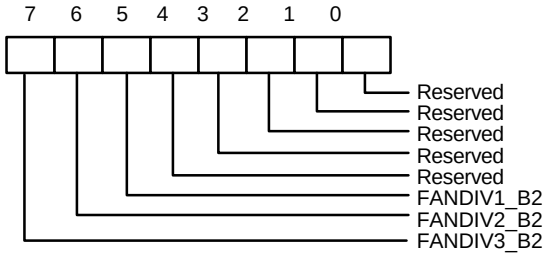


Bit 7: Reserved
Bit 6-4: PWMOUT1 clock selection.
The clock-defined frequency is same as PWMOUT2 clock selection.

Bit 3: Set to 1. Enable PWMOUT1 PWM Control
Bit 2-0: PWMOUT2 clock Selection.
<2:0> = 000: 46.87kHz
<2:0> = 001: 23.43kHz (Default)
<2:0> = 010: 11.72kHz
<2:0> = 011: 5.85kHz
<2:0> = 100: 2.93kHz

Fan Divisor Control Register -- Index 5Dh (*Bank 0*)

Register Location:	5Dh
Power on Default Value	<7:0> 0000-0000. Reset by MR.
Attribute:	Read/Write
Size:	8 bits



Bit 7: Fan3 divisor Bit 2.
Bit 6: Fan2 divisor Bit 2.
Bit 5: Fan1 divisor Bit 2.
Bit 4-0: Reserved

FAN DIVISOR TABLE

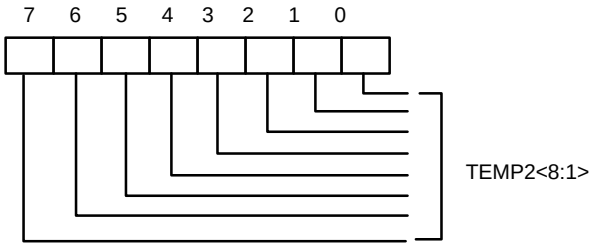
BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
0	0	0	1	1	0	0	16
0	0	1	2	1	0	1	32
0	1	0	4	1	1	0	64
0	1	1	8	1	1	1	128

Reserved Register -- Index 5Eh (*Bank 0*)

Reserved Register -- Index 5Fh (*Bank 0*)

Temperature Sensor 1 Temperature (High Byte) Register - Index 00h

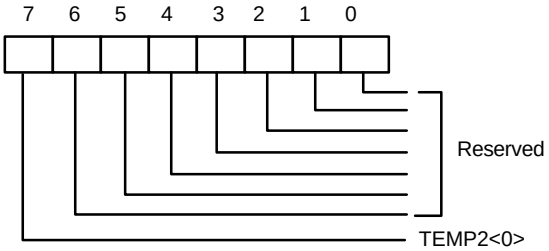
Register Location: 00h
Attribute: Read Only
Size: 8 bits



Bit 7-0: Temperature <8:1> of sensor 2, Bit 7 is MSB.

Temperature Sensor 1 Temperature (Low Byte) Register - Index 00h

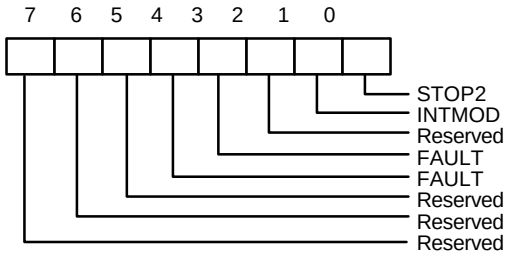
Register Location: 00h
Attribute: Read Only
Size: 8 bits



Bit 7: Temperature <0> of sensor2, LSB.
Bit 6-0: Reserved. This bit should be set to 0.

Temperature Sensor 1 Configuration Register - Index 01h

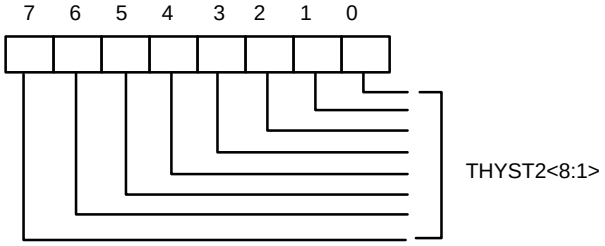
Register Location: 01h
Power on Default Value <7:0> = 0x00
Size: 8 bits



Bit 7-5: Read - Reserved. This bit should be set to 0.
Bit 4-3: Read/Write - Number of faults to detect before setting nOVT output to avoid false tripping due to noise.
Bit 2: Read - Reserved. This bit should be set to 0.
Bit 1: Read/Write - nOVT Interrupt mode select. If set to 0(default), compared mode. If set to 1, interrupt mode will be selected.
Bit 0: Read/Write - When set to 1 the sensor will stop monitoring.

Temperature Sensor 1 Hysteresis (High Byte) Register - Index 02h

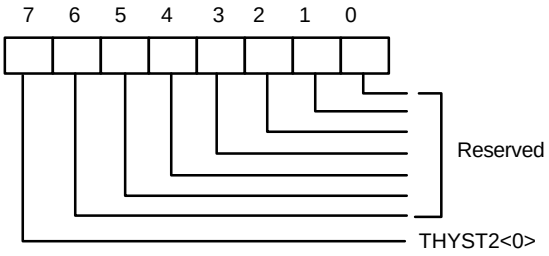
Register Location:	02h
Power on Default Value	<7:0> = 0x4B
Attribute:	Read/Write
Size:	8 bits



Bit 7-0: Temperature hysteresis bit 8-1, Bit 7 is MSB. The temperature default is 75 degree C.

Temperature Sensor 1 Hysteresis (Low Byte) Register - Index 02h

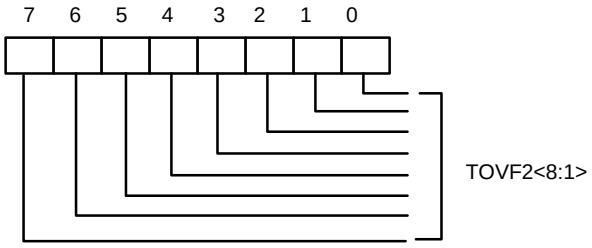
Register Location:	02h
Power on Default Value	<7:0> = 0x0
Attribute:	Read Only
Size:	8 bits



Bit 7: Temperature hysteresis bit 0, LSB.
Bit 6-0: Reserved. This bit should be set to 0.

Temperature Sensor 1 Over-temperature (High Byte) Register - Index 03h

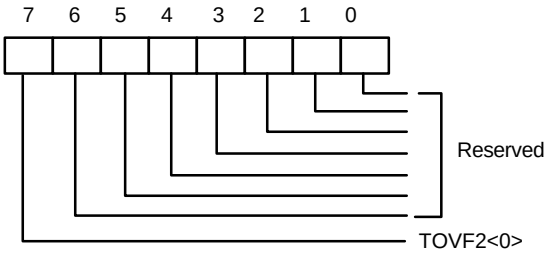
Register Location:	03h
Power on Default Value	<7:0> = 0x50
Attribute:	Read/Write
Size:	8 bits



Bit 7-0: Over-temperature bit 8-1, Bit 7 is MSB. The temperature default 80 degree C.

Temperature Sensor 1 Over-temperature (Low Byte) Register - Index 03h

Register Location:	03h
Power on Default Value	<7:0> = 0x0
Size:	8 bits

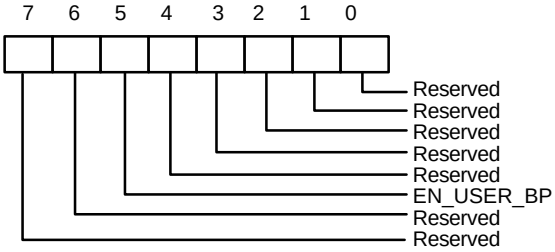


Bit 7: Read/Write - Over-temperature bit 0, LSB.
Bit 6-0: Read Only - Reserved. This bit should be set to 0.

Reserved Register -- Index 50h--52h (BANK4)

BEEP Control Register 3 -- Index 53h (*Bank 4*)

Register Location: 53h
Power on Default Value <7:0> 0000,0000. Reset by MR.
Attribute: Read/Write
Size: 8 bits

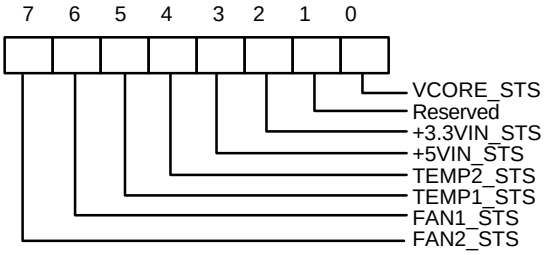


Bit 7-6: Reserved.
Bit 5: User define BEEP output function. If set to 1, the BEEP is always active. If set to 0, this function is inactive. (Default 0)
Bit 4-0: Reserved.

Reserved Register -- Index 54h--58h (*Bank 4*)

Real Time Hardware Status Register I -- Index 59h (*Bank 4*)

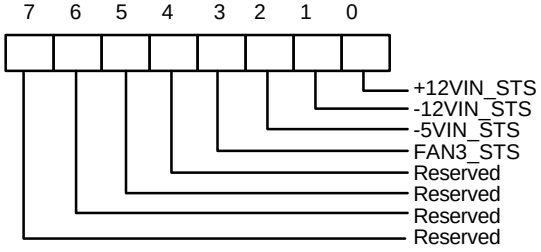
Register Location: 59h
Power on Default Value <7:0> 0000,0000. Reset by MR.
Attribute: Read Only
Size: 8 bits



Bit 7: FAN 2 Status. If 1, the fan speed counter is over the limit value. If 0, the fan speed counter is in the limit range.
Bit 6: FAN 1 Status. If 1, the fan speed counter is over the limit value. If 0, the fan speed counter is in the limit range.
Bit 5: Temperature sensor 1 Status. If 1, the voltage of temperature sensor is over the limit value. If 0, the voltage of temperature sensor is in the limit range.
Bit 4: Temperature sensor 2 Status. If 1, the voltage of temperature sensor is over the limit value. If 0, the voltage of temperature sensor is in the limit range.
Bit 3: +5V Voltage Status. If 1, the voltage of +5V is over the limit value. If 0, the voltage of +5V is in the limit range.
Bit 2: +3.3V Voltage Status. If 1, the voltage of +3.3V is over the limit value. If 0, the voltage of +3.3V is in the limit range.
Bit 1: Reserved.
Bit 0: VCORE Voltage Status. If 1, the voltage of VCORE is over the limit value. If 0, the voltage of VCORE is in the limit range.

Real Time Hardware Status Register II -- Index 5Ah (*Bank 4*)

Register Location: 5Ah
Power on Default Value <7:0> 0000,0000. Reset by MR.
Attribute: Read Only
Size: 8 bits



Bit 7-4: Reserved
Bit 3: FAN3 Voltage Status. If 1, the fan speed counter is over the limit value. If 0, the fan speed counter is during the limit range.
Bit 2: -5V Voltage Status. If 1, the voltage of -5V is over the limit value. If 0, the voltage of -5V is during the limit range.
Bit 1: -12V Voltage Status. If 1, the voltage of -12V is over the limit value. If 0, the voltage of -12V is during the limit range.
Bit 0: +12V Voltage Status. If 1, the voltage of +12V is over the limit value. If 0, the voltage of +12V is in the limit range.

SPECIFICATIONS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Characteristics

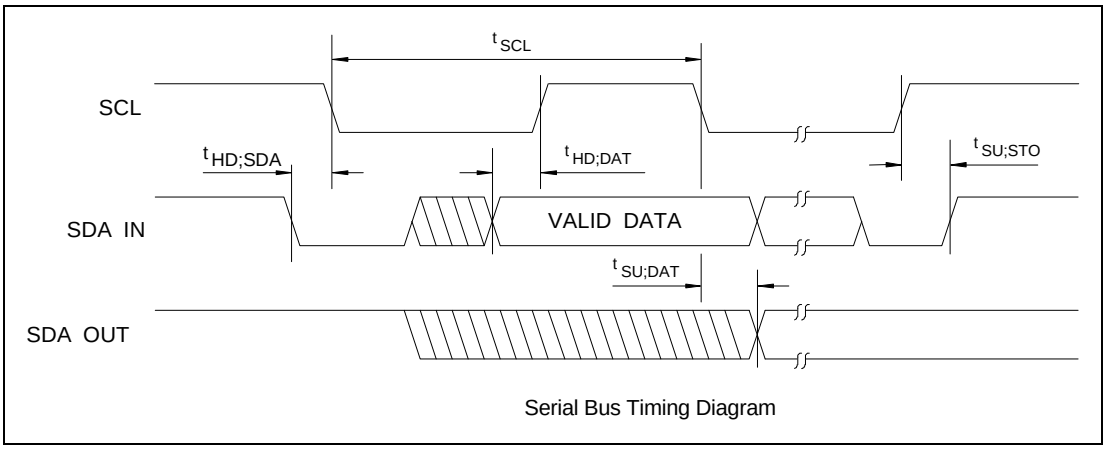
(Ta = 0° C to 70° C, VDD = 5V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = - 12 mA
Input High Leakage	ILIH			+10	µA	VIN = VDD
Input Low Leakage	ILIL			-10	µA	VIN = 0V
I/O_{12ts} - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 5 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 5 V
Hysteresis	VTH	0.5	1.2		V	VDD = 5 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = - 12 mA
Input High Leakage	ILIH			+10	µA	VIN = VDD
Input Low Leakage	ILIL			-10	µA	VIN = 0V
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
OD_8 - Open-drain output pin with sink capability of 8 mA						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
OD_{12} - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
OD_{48} - Open-drain output pin with sink capability of 48 mA						
Output Low Voltage	VOL			0.4	V	IOL = 48 mA
IN_t - TTL level input pin						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	µA	VIN = VDD

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Low Leakage	ILIL			-10	µA	VIN = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 5 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 5 V
Hysteresis	VTH	0.5	1.2		V	VDD = 5 V
Input High Leakage	ILIH			+10	µA	VIN = VDD
Input Low Leakage	ILIL			-10	µA	VIN = 0 V

AC CHARACTERISTICS

Serial Bus Timing Diagram



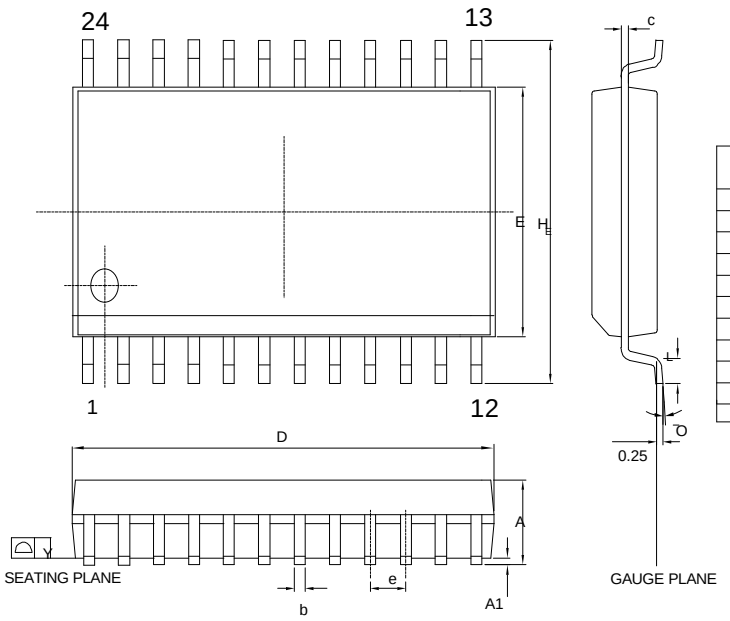
Serial Bus Timing Diagram

Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

PACKAGE DIMENSIONS

(24 Pin SOP)



Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	15.20	15.60	0.598	0.614
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	———	0.10	———	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

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