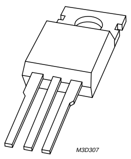


PHP45NQ11T

N-channel TrenchMOS™ standard level FET

Rev. 01 — 31 March 2004 **Product data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Fast switching
- Low on-state resistance.

1.3 Applications

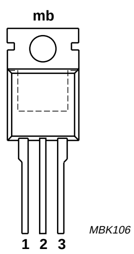
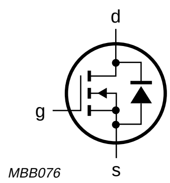
- DC-to-DC converters
- Switched-mode power supplies.

1.4 Quick reference data

- $V_{DS} \leq 105$ V
- $P_{tot} \leq 150$ W
- $I_D \leq 47$ A
- $R_{DSon} \leq 25$ mΩ.

2. Pinning information

Table 1: Pinning - SOT78 (TO-220AB), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 **SOT78 (TO-220AB)**	
2	drain (d)		
3	source (s)		
mb	mounting base; connected to drain (d)		

3. Ordering information

Table 2: Ordering information

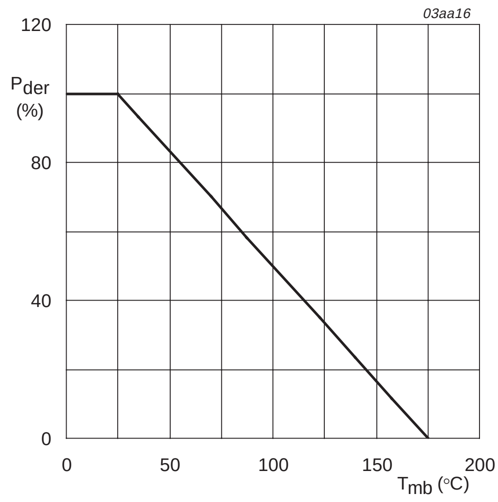
Type number	Package		
	Name	Description	Version
PHP45NQ11T	TO-220AB	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads	SOT78

4. Limiting values

Table 3: Limiting values

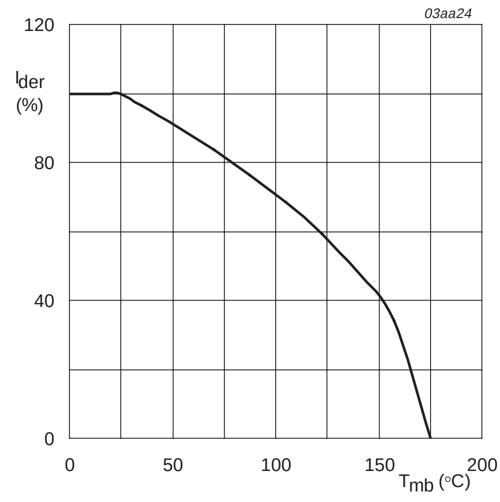
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 175 °C	-	105	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	105	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	-	47	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2	-	33	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	188	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	-	150	W
T_{stg}	storage temperature		–55	+175	°C
T_j	junction temperature		–55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	-	47	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	188	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_{AS} = 18 A; t_p = 120 µs; V_{DD} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C	-	160	mJ



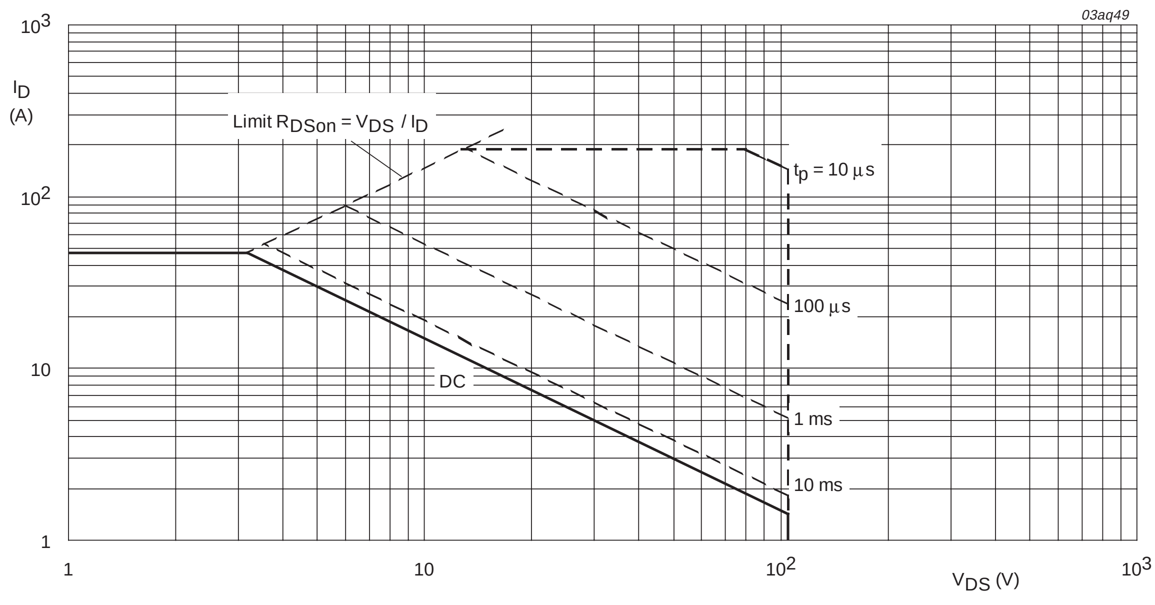
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W

5.1 Transient thermal impedance

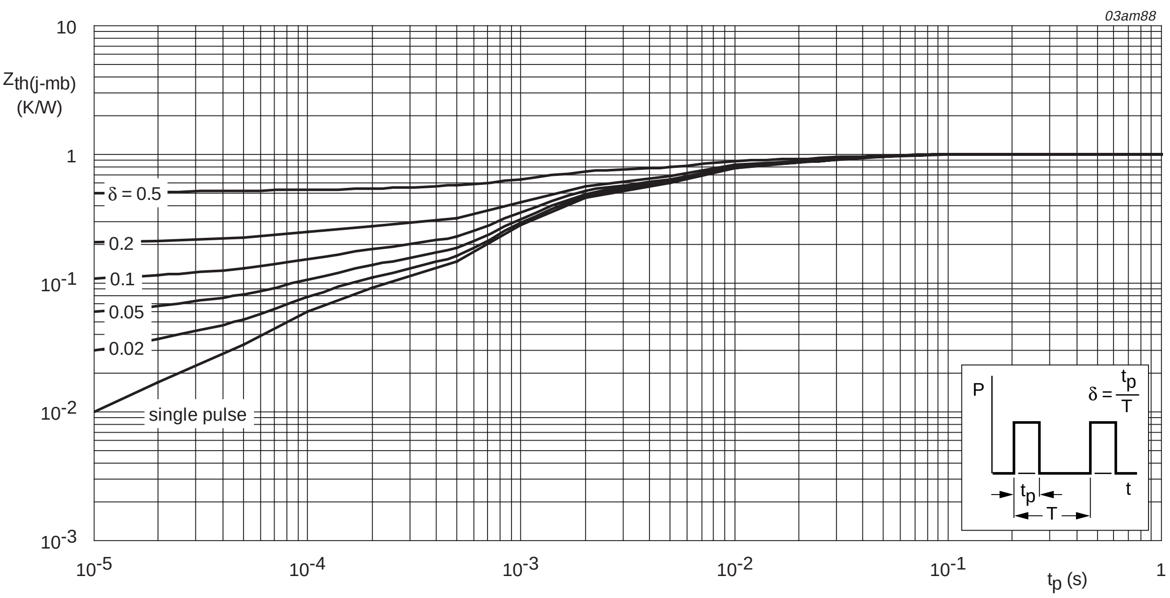


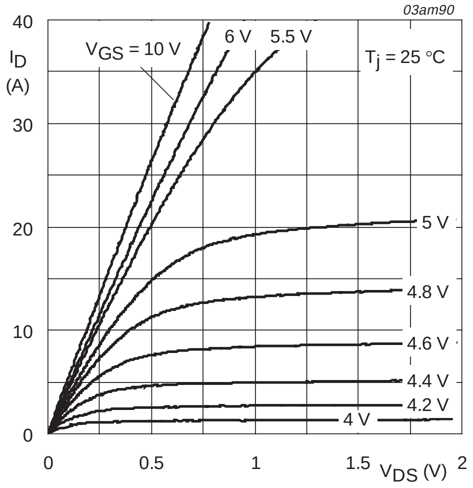
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

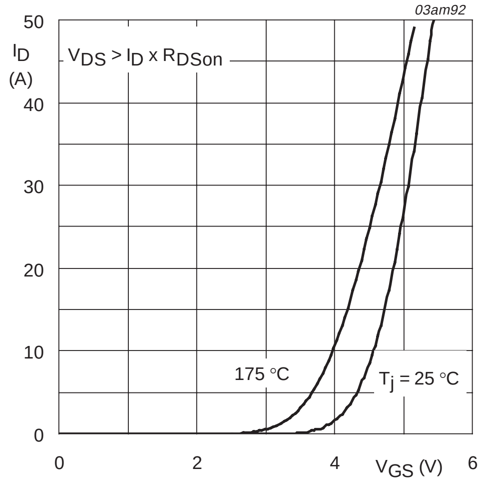
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	105	-	-	V
		T_j = –55 °C	95	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	2	3	4	V
		T_j = 175 °C	1	-	-	V
		T_j = –55 °C	-	-	4.4	V
I_{DSS}	drain-source leakage current	V_{DS} = 100 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	10	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; Figure 7 and 8				
		T_j = 25 °C	-	19	25	mΩ
		T_j = 175 °C	-	51.3	68	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 45 A; V_{DD} = 80 V; V_{GS} = 10 V; Figure 13	-	60	-	nC
Q_{gs}	gate-source charge		-	11.2	-	nC
Q_{gd}	gate-drain (Miller) charge		-	23.2	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 11	-	2930	-	pF
C_{oss}	output capacitance		-	245	-	pF
C_{rss}	reverse transfer capacitance		-	160	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 50 V; R_D = 1.8 Ω; V_{GS} = 10 V; R_G = 5.6 Ω	-	11.5	-	ns
t_r	rise time		-	40	-	ns
$t_{d(off)}$	turn-off delay time		-	40	-	ns
t_f	fall time		-	45	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 12	-	0.87	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 30 V	-	82	-	ns
Q_r	recovered charge		-	117	-	nC



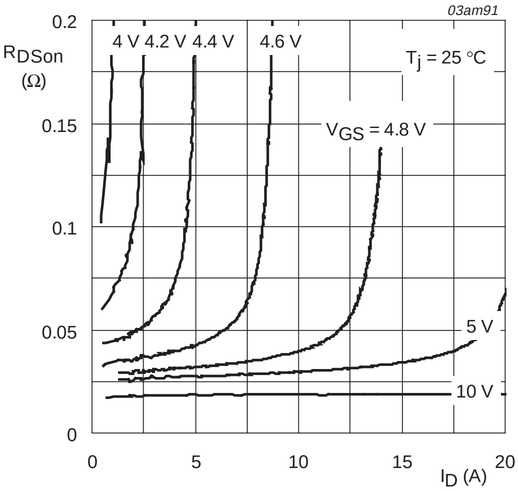
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



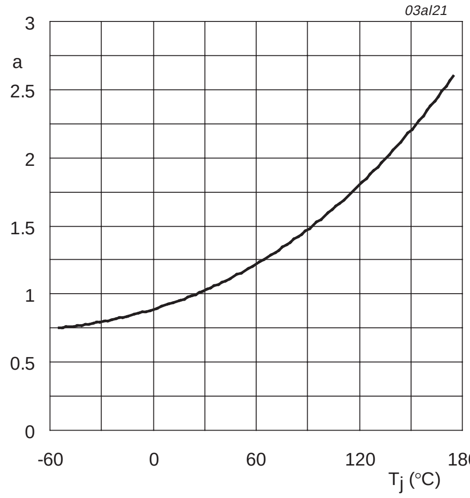
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



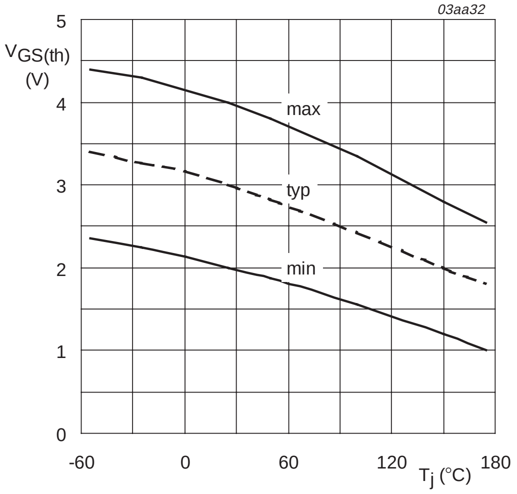
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



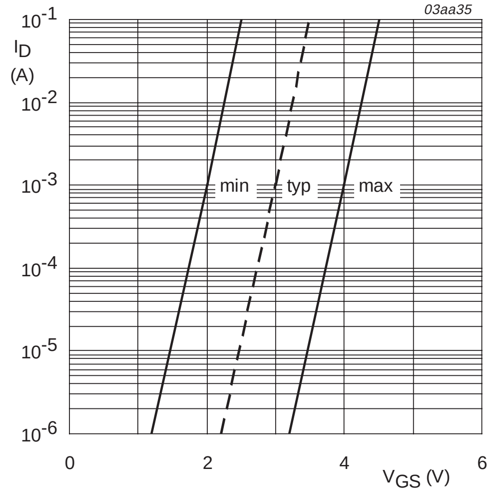
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



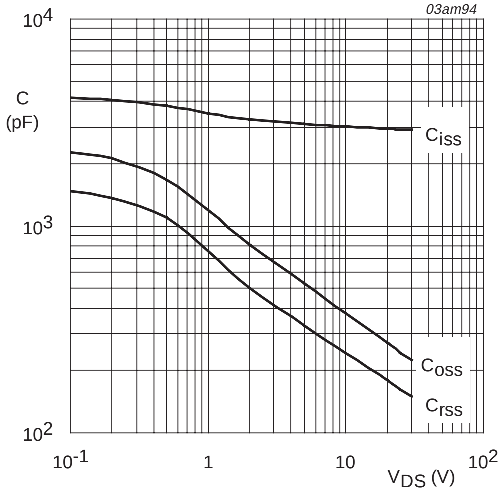
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



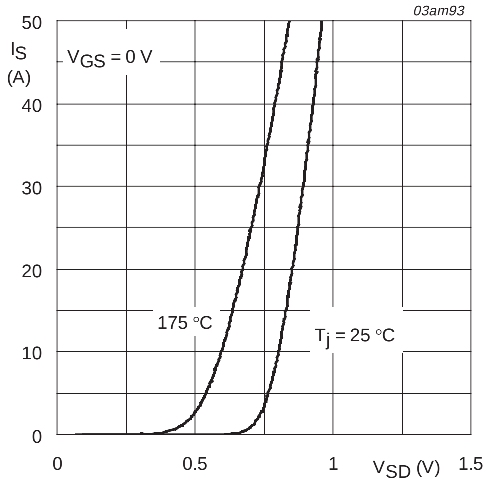
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



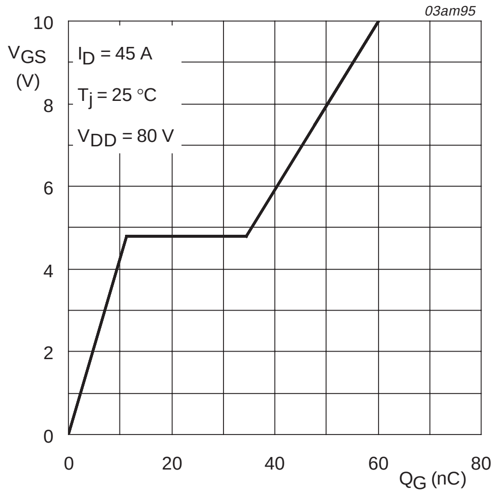
V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

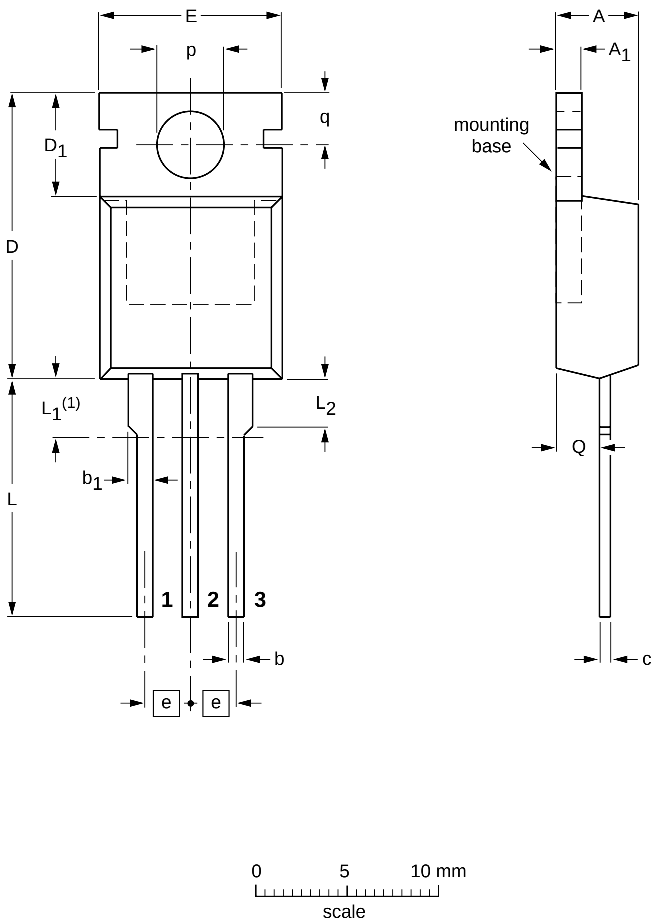


I_D = 45 A; V_{DD} = 80 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1(1)	L_2 max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			~~00-09-07~~ 01-02-16

Fig 14. SOT78 (TO-220AB).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040331	-	Product data (9397 750 13059)

9. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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