R6986

38 V 2 A synchronous step-down switching regulator with 30 µA quiescent current

Datasheet - preliminary data

HTSSOP16 (R_{TH} = 40 °C/W)

Features

- General features
  - 2 A DC output current
  - 4 V to 38 V operating input voltage
  - Large ambient temperature range: -40 °C to 125 °C
  - Low consumption mode or low noise mode
  - 30 µA IQ at light load (LCM V_{OUT} = 3.3 V)
  - 8 µA $I_{Q\text{-}SHTDWN}$
  - Adjustable f_{SW} (250 kHz - 2 MHz)
  - Output voltage adjustable from 0.85 V to V_{IN}
  - Embedded output voltage supervisor
  - Synchronization
  - Adjustable soft-start time
  - Internal current limiting
  - Overvoltage protection
  - Output voltage sequencing
  - Peak current mode architecture
  - $R_{DSON\ HS}$ = 180 mΩ, $R_{DSON\ LS}$ = 110 mΩ
  - Thermal shutdown
- Aerospace and defense features
  - Suitable for use in aerospace and defense applications
  - Dedicated traceability and part marking
  - Production parts approval documents available
  - Adapted extended life time and obsolescence management
  - Extended product change notification process
  - Designed and manufactured to meet sub-ppm quality goals
  - Advanced mold and frame designs for superior resilience in harsh environments (acceleration, EMI, thermal, humidity)
  - Extended screening capability on request

Applications

- Designed for aerospace applications
- Battery powered applications

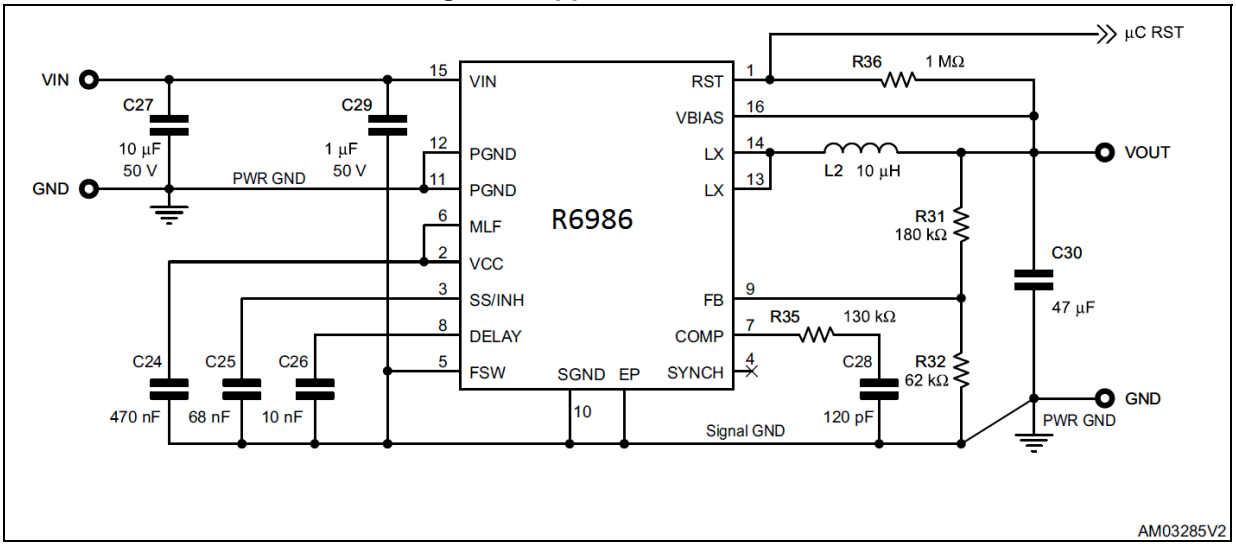
Description

The R6986 device is a step-down monolithic switching regulator able to deliver up to 2 A DC. The output voltage adjustability ranges from 0.85 V to V_{IN}. The 100% duty cycle, the wide input voltage range and the large ambient temperature range make it ideal for aerospace and defense applications. The “Low Consumption Mode” (LCM) is designed for always-on applications, so it maximizes the efficiency at light load with controlled output voltage ripple. The “Low Noise Mode” (LNM) makes the switching frequency constant and minimizes the output voltage ripple overload current range. The output voltage supervisor manages the reset phase for any digital load (µC, FPGA.). The RST open collector output can also implement output voltage sequencing during the power-up phase. The synchronous rectification, designed for high efficiency at medium - heavy load, and the high switching frequency capability make the size of the application compact. Pulse by pulse current sensing on both power elements implements an effective constant current protection.

Contents

1 Application schematic

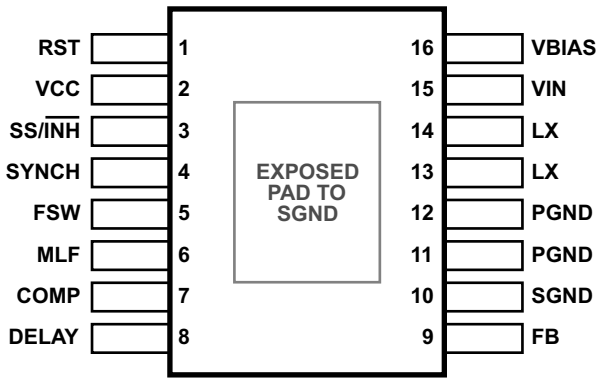
Figure 1. Application schematic



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection (top view)



2.2 Pin description

Table 1. Pin description

No.	Pin	Description
1	RST	The RST open collector output is driven low when the output voltage is out of regulation. The RST is released after an adjustable time DELAY once the output voltage is over the active delay threshold.
2	VCC	Connect a ceramic capacitor (≥ 470 nF) to filter internal voltage reference. This pin supplies the embedded analog circuitry.
3	SS/$\overline{\text{INH}}$	An open collector stage can disable the device clamping this pin to GND ($\overline{\text{INH}}$ mode). An internal current generator (2 µA typ.) charges the external capacitor to implement the soft-start.
4	SYNCH	Master / slave synchronization
5	FSW	A pull up resistor (E24 series only) to VCC or pull down to GND selects the switching frequency. Pinstrapping is active only before the soft-start phase to minimize the IC consumption.
6	MLF	A pull up resistor (E24 series only) to VCC or pull down to GND selects the low noise mode/low consumption mode and the active RST threshold. Pinstrapping is active only before the soft-start phase to minimize the IC consumption.
7	COMP	Output of the error amplifier. The designed compensation network is connected at this pin.
8	DELAY	An external capacitor connected at this pin sets the time DELAY to assert the rising edge of the RST o.c. after the output voltage is over the reset threshold. If this pin is left floating, RST is like a power good.
9	FB	Inverting input of the error amplifier
10	SGND	Signal GND
11	PGND	Power GND

Table 1. Pin description (continued)

No.	Pin	Description
12	PGND	Power GND
13	LX	Switching node
14	LX	Switching node
15	VIN	DC input voltage
16	V_{BIAS}	Typically connected to the regulated output voltage. An external voltage reference can be used to supply part of the analog circuitry to increase the efficiency at light load. Connect to GND if not used.
-	E. p.	Exposed pad must be connected to SGND

2.3 Maximum ratings

Stressing the device above the rating listed in *Table 2: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
V_{IN}	See *Table 1*	40	V	
DELAY		-0.3	V_{CC} + 0.3	V
PGND		SGND - 0.3	SGND + 0.3	V
SGND				V
V_{CC}		-0.3	(V_{IN} + 0.3) or (max. 4)	V
SS / $\overline{INH}$		-0.3	V_{IN} + 0.3	V
MLF		-0.3	V_{CC} + 0.3	V
COMP		-0.3	V_{CC} + 0.3	V
FB		-0.3	V_{CC} + 0.3	V
FSW		-0.3	V_{CC} + 0.3	V
SYNCH		-0.3	V_{IN} + 0.3	V
V_{BIAS}		-0.3	(V_{IN} + 0.3) or (max. 6)	V
RST		-0.3	V_{IN} + 0.3	V
LX		-0.3	V_{IN} + 0.3	V
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range		-65 to 150	°C
T_{LEAD}	Lead temperature (soldering 10 sec.)		260	°C
I_{HS}, I_{LS}	High-side / low-side switch current		2	A

2.4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ JA}$	Thermal resistance junction ambient (device soldered on the STMicroelectronics® demonstration board)	40	C/W

2.5 ESD protection

Table 4. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	2	KV
	MM	150	V
	CDM	500	V

3 Electrical characteristics

T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Note	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range			4		38	V
V_{INH}	V_{CC} UVLO rising threshold			2.7		3.5	
V_{INL}	V_{CC} UVLO falling threshold			2.5		3.5	
I_{PK}	Peak current limit	Duty cycle < 40%		2.6			A
		Duty cycle = 100% closed loop operation		2.1			
I_{VY}	Valley current limit			2.7			
I_{SKIP}	Skip current limit		(1)		0.6	0.8	
I_{VY_SNK}	Reverse current limit	LNM or V_{OUT} overvoltage		0.5	1	2	
$R_{DSON\ HS}$	High-side RDSON	I_{SW} = 1 A			0.18	0.360	Ω
$R_{DSON\ LS}$	Low-side RDSON	I_{SW} = 1 A			0.15	0.300	
f_{SW}	Selected switching frequency	FSW pinstrapping before SS		see *Table 6: f_{SW} selection*			
I_{FSW}	FSW biasing current	SS ended			0	500	nA
LCM/LNM	Low noise mode / Low consumption mode selection	MLF pinstrapping before SS		see *Table 7: LNM / LCM selection on page 12*			
I_{MLF}	MLF biasing current	SS ended			0	500	nA
D	Duty cycle		(2)	0		100	%
$T_{ON\ MIN}$	Minimum On time				100		ns
VCC regulator							
V_{CC}	LDO output voltage	V_{BIAS} = GND (no switchover)		2.9	3.3	3.6	V
		V_{BIAS} = 5 V (switchover)		2.9	3.3	3.6	
SWO	V_{BIAS} threshold	Switch internal supply from V_{IN} to V_{BIAS}		2.85		3.2	
		Switch internal supply from V_{BIAS} to V_{IN}		2.8		3.15	

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Note	Min.	Typ.	Max.	Unit
Power consumption							
I_{SHTDWN}	Shutdown current from V_{IN}	$V_{SS/INH}$ = GND		4	8	15	µA
$I_{Q\ OPVIN}$	Quiescent current from V_{IN}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(3)	4	10	15	µA
		LCM - NO SWO $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = GND	(3)	35	70	120	
		LNM - SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = 3.3 V		0.5	1.5	5	mA
		LNM - NO SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = GND		2	2.8	6	
$I_{Q\ OPVBIAS}$	Quiescent current from V_{BIAS}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(3)	20	50	115	µA
		LNM - SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = 3.3 V		0.5	1.2	5	mA
Soft-start							
V_{INH}	VSS threshold	SS rising		200	460	700	mV
$V_{INH\ HYST}$	VSS hysteresis				60		
$I_{SS\ CH}$	C_{SS} charging current	$V_{SS} < V_{INH}$ OR $t < T_{SS\ SETUP}$ OR $V_{EA+} > V_{FB}$	(2)		1		µA
		$t > T_{SS\ SETUP}$ AND $V_{EA+} < V_{FB}$	(2)		4		
$V_{SS\ CLMP}$	SS discharge voltage	$V_{CC} < V_{CCH}$ OR $t < T_{SS\ SETUP}$OR thermal fail		855	900	945	mV
$V_{SS\ START}$	Start of internal error amplifier ramp			0.995	1.1	1.150	V
SS_{GAIN}	SS/INH to internal error amplifier gain				3		
$V_{SS\ END}$	SS/INH voltage at the end of SS phase				2.5	3.6	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Note	Min.	Typ.	Max.	Unit
Error amplifier							
V_{FB}	Voltage feedback			0.841	0.85	0.859	V
I_{FB}	FB biasing current				50	500	nA
G_m	Transconductance			90	155	210	µS
			(4)	70	155	210	
A_V	Error amplifier gain		(2)		100		dB
I_{COMP}	EA output current capability			±6	±12	±25	µA
			(4)	±4			
Inner current loop							
g_{CS}	Current sense transconductance (V_{COMP} to inductor current gain)	Ipk = 1 A	(5)		2.5		A/V
$V_{PP} \cdot g_{CS}$	Slope compensation		(5)	0.4	0.75	1.0	A
Overvoltage protection							
V_{OVP}	Overvoltage trip (V_{OVP}/V_{REF})			1.15	1.2	1.25	
$V_{OVP\ HYST}$	Overvoltage hysteresis			1	2	6	%
Synchronization (fan out: 6 slave devices typ.)							
$f_{SYN\ MIN}$	Synchronization frequency	LNM; f_{SW} = VCC		266.5			kHz
$V_{SYN\ TH}$	SYNCH input threshold	LNM, SYNCH rising		0.70		1.2	V
I_{SYN}	SYNCH pulldown current	LNM, V_{SYN} = 1.2 V			0.7		mA
$V_{SYN\ OUT}$	high level output	LNM, 5 mA sinking load		1.40			V
	low level output	LNM, 0.7 mA sourcing load				0.6	
Reset							
V_{THR}	Selected RST threshold	MLF pinstrapping before SS		see *Table 7*			
$V_{THR\ HYST}$	RST hysteresis		(2)		2		%
V_{RST}	RST open collector output	$V_{IN} > V_{INH}$ AND $V_{FB} < V_{TH}$ 4 mA sinking load				0.4	V
		$2 < V_{IN} < V_{INH}$ 4 mA sinking load				0.8	
Delay							
V_{THD}	RST open collector released as soon as $V_{DELAY} > V_{THD}$	$V_{FB} > V_{THR}$		1.19	1.234	1.258	V
$I_{D\ CH}$	C_{DELAY} charging current	$V_{FB} > V_{THR}$		1	2	3	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Note	Min.	Typ.	Max.	Unit
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature		(2)		165		°C
T_{HYS}	Thermal shutdown hysteresis		(2)		30		

1. Parameter tested in static condition during testing phase. Parameter value may change over dynamic application condition.
2. Not tested in production.
3. LCM enables SLEEP mode at light load.
4. T_J = -40 °C.
5. Measured at fSW = 250 kHz.

All the population tested at T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 6. f_{SW} selection

Symbol	R_{VCC} (E24 series)	R_{GND} (E24 series)	f_{SW} min.	f_{SW} typ.	f_{SW} max.	Note	Unit
f_{SW}	0 Ω	NC	225	**250**	275	(1)	kHz
	1.8 kΩ	NC		**285**		(2)	
	3.3 kΩ	NC		**330**			
	5.6 kΩ	NC		**380**			
	10 kΩ	NC		**435**			
	NC	0 Ω	450	**500**	550	(1)	
	18 kΩ	NC		**575**		(2)	
	33 kΩ	NC		**660**			
	56 kΩ	NC		**755**			
	NC	1.8 kΩ		**870**			
	NC	3.3 kΩ	900	**1000**	1100		
	NC	5.6 kΩ		**1150**		(2)	
	NC	10 kΩ		**1310**			
	NC	18 kΩ		**1500**			
	NC	33 kΩ	1575	**1750**	1925		
	NC	56 kΩ	1800	**2000**	2200		

1. Preferred codifications don't require any external resistor.
2. Not tested in production.

All the population tested at T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 7. LNM / LCM selection

Symbol	R_{VCC} (E24 series)	R_{GND} (E24 series)	Operating mode	V_{RST}/V_{OUT} (tgt value)	V_{RST} min.	V_{RST} typ.	V_{RST} max.	Unit
V_{RST}	0 Ω	NC	**LCM**	**93%**	0.779	**0.791**	0.802	V
	8.2 kΩ ± 1%	NC		**80%**	0.670	**0.680**	0.690	
	18 kΩ ± 1%	NC		**87%**	0.728	**0.740**	0.751	
	39 kΩ ± 1%	NC		**96%**	0.804	**0.816**	0.828	
	NC	0 Ω	**LNM**	**93%**	0.779	**0.791**	0.802	
	NC	8.2 kΩ ± 1%		**80%**	0.670	**0.680**	0.690	
	NC	18 kΩ ± 1%		**87%**	0.728	**0.740**	0.751	
	NC	39 kΩ ± 1%		**96%**	0.804	**0.816**	0.828	

V_{RST} = 0.791 V typical, LNM and LCM preferred codifications don't require any external resistor.

4 Datasheet parameters over the temperature range

The 100% of the population in the production flow is tested at three different ambient temperatures (-40 °C, +25 °C, +135 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C, +135 °C).

The device operation is guaranteed when the junction temperature is inside the (-40 °C, +150 °C) temperature range. The designer can estimate the silicon temperature increase respect to the ambient temperature evaluating the internal power losses generated during the device operation.

However the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the T_{SHTDWN} (+165 °C typ.) temperature.

All the datasheet parameters can be guaranteed to a maximum junction temperature of +135 °C to avoid triggering the thermal shutdown protection during the testing phase because of self-heating.

5 Functional description

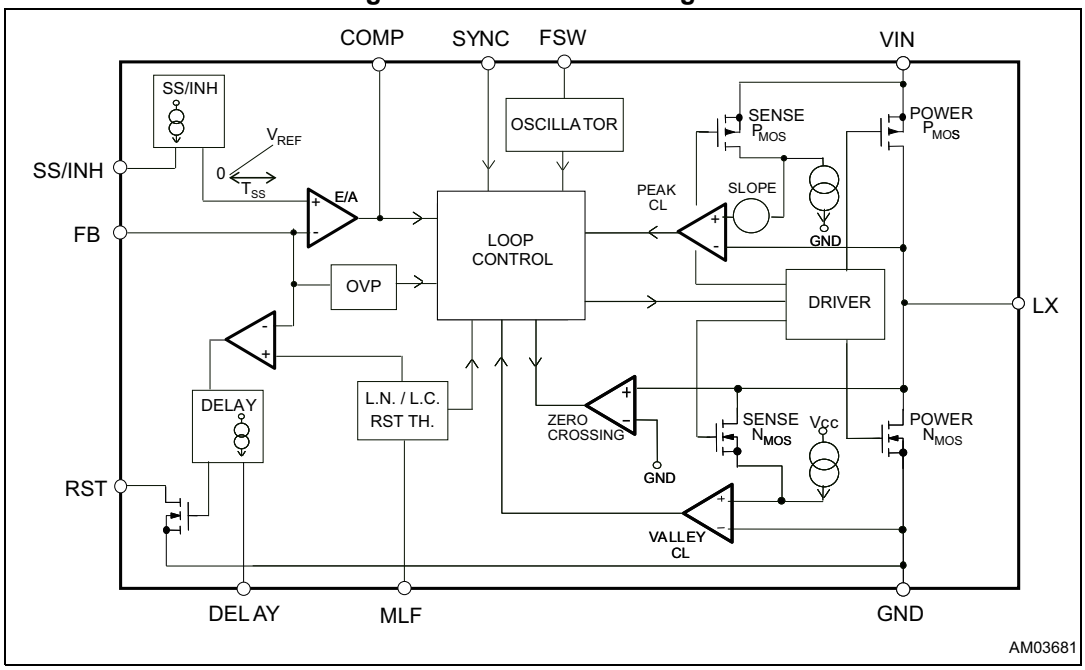
The R6986 device is based on a “peak current mode”, constant frequency control. As a consequence, the intersection between the error amplifier output and the sensed inductor current generates the PWM control signal to drive the power switch.

The device features LNM (low noise mode) that is forced PWM control, or LCM (low consumption mode) to increase the efficiency at light load.

The main internal blocks shown in the block diagram in *Figure 3* are:

- Embedded power elements. Thanks to the P-channel MOSFET as high-side switch the device features low dropout operation
- A fully integrated sawtooth oscillator with adjustable frequency
- A transconductance error amplifier
- The high-side current sense amplifier to sense the inductor current
- A “Pulse Width Modulator” (PWM) comparator and the driving circuitry of the embedded power elements
- The soft-start blocks to ramp the error amplifier reference voltage and so decreases the inrush current at power-up. The SS/$\overline{\text{INH}}$ pin inhibits the device when driven low.
- The switchover capability of the internal regulator to supply a portion of the quiescent current when the V_{BIAS} pin is connected to an external output voltage
- The synchronization circuitry to manage master / slave operation and the synchronization to an external clock
- The current limitation circuit to implement the constant current protection, sensing pulse by pulse high-side / low-side switch current. In case of heavy short-circuit the current protection is fold back to decrease the stress of the external components
- A circuit to implement the thermal protection function
- The OVP circuitry to discharge the output capacitor in case of overvoltage event
- MLF pin strapping sets the LNM/LCM mode and the thresholds of the RST comparator
- FSW pinstrapping sets the switching frequency
- The RST open collector output

Figure 3. Internal block diagram



5.1 Power supply and voltage reference

The internal regulator block consists of a start-up circuit, the voltage pre-regulator that provides current to all the blocks and the bandgap voltage reference. The starter supplies the startup current when the input voltage goes high and the device is enabled (SS/INH pin over the inhibits threshold).

The pre-regulator block supplies the bandgap cell and the rest of the circuitry with a regulated voltage that has a very low supply voltage noise sensitivity.

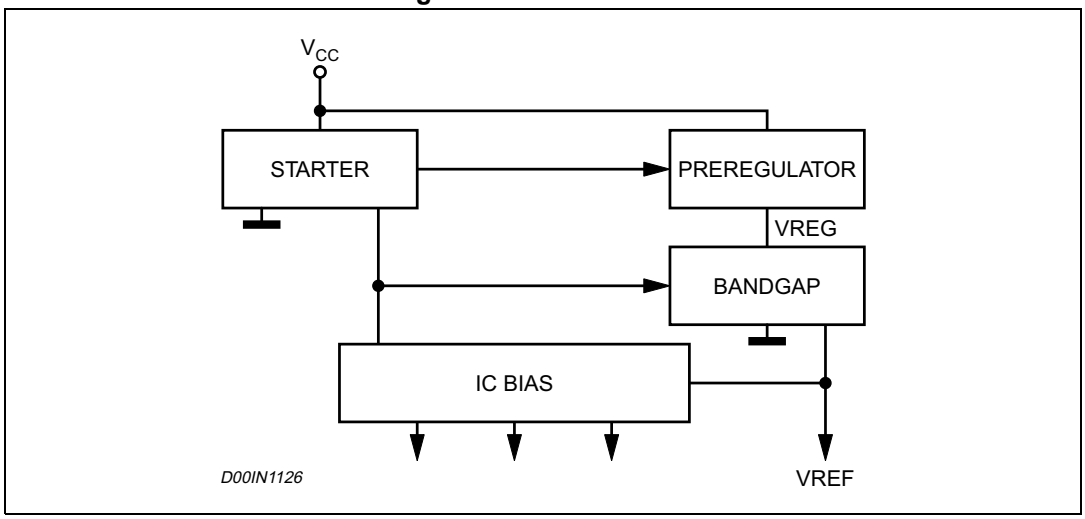
Switchover feature

The switchover scheme of the pre-regulator block features to derive the main contribution of the supply current for the internal circuitry from an external voltage (3 V < V_{BIAS} < 5.5 V is typically connected to the regulated output voltage). This helps to decrease the equivalent quiescent current seen at V_{IN}. (please refer to *Section 5.6: Switchover feature on page 25*).

5.2 Voltages monitor

An internal block continuously senses the V_{CC}, V_{BIAS} and V_{BG}. If the monitored voltages are good, the regulator starts operating. There is also a hysteresis on the V_{CC} (UVLO).

Figure 4. Internal circuit



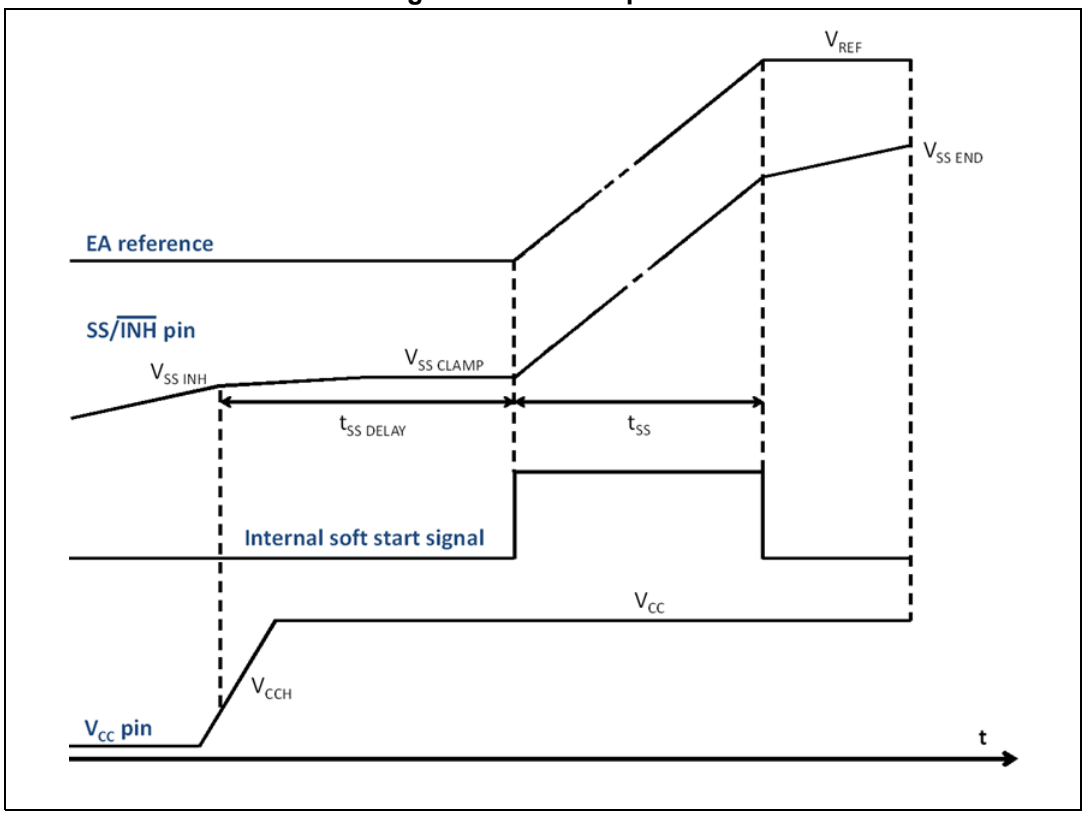
5.3 Soft-start and inhibit

The soft-start and inhibit features are multiplexed on the same pin. An internal current source charges the external soft-start capacitor to implement a voltage ramp on the SS/INH pin. The device is inhibited as long as the SS/INH pin voltage is lower than the V_{INH} threshold and the soft-start takes place when SS/INH pin crosses $V_{SS\ START}$. (see *Figure 5: Soft-start phase*).

The internal current generator sources 1 µA typ. current when the voltage of the VCC pin crosses the UVLO threshold. The current increases to 4 µA typ. as soon as the SS/INH voltage is higher than the V_{INH} threshold. This feature helps to decrease the current consumption in inhibit mode. An external open collector can be used to set the inhibit operation clamping the SS/INH voltage below V_{INH} threshold.

The startup feature minimizes the inrush current and decreases the stress of the power components during the power-up phase. The ramp implemented on the reference of the error amplifier has a gain three times higher (SS_{GAIN}) than the external ramp present at SS/INH pin.

Figure 5. Soft-start phase



The C_{SS} is dimensioned accordingly with *Equation 1*:

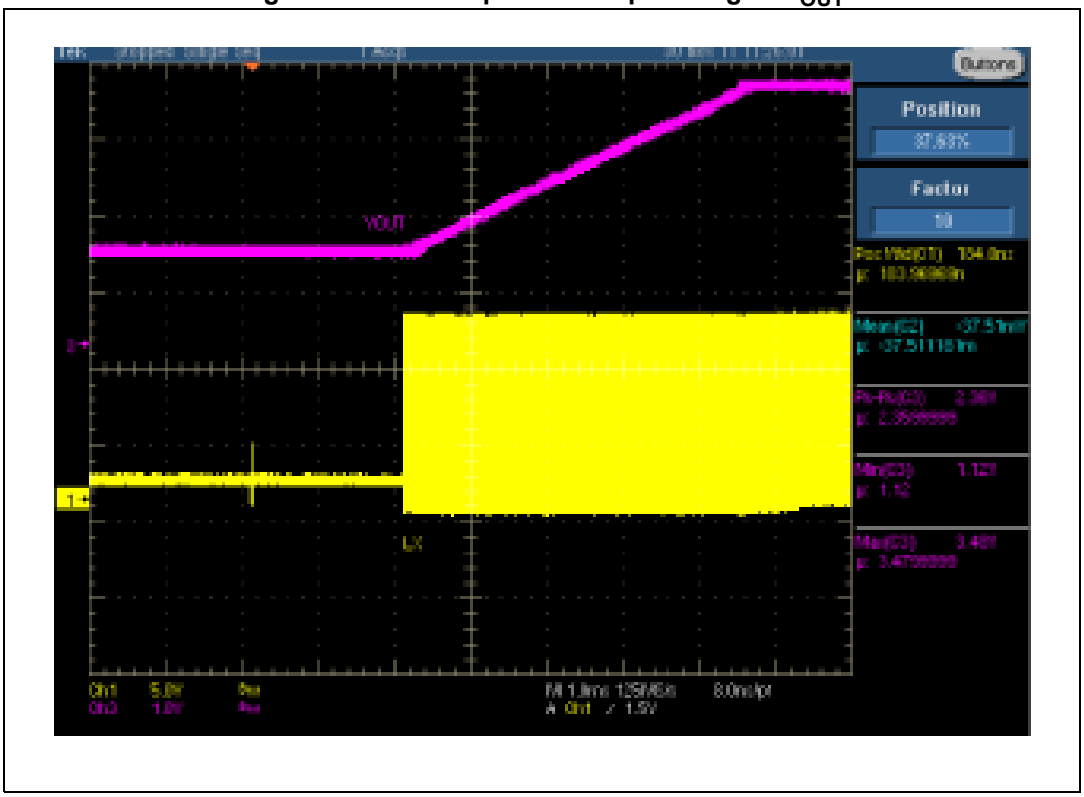
Equation 1

$$C_{SS} = SS_{GAIN} \bullet \frac{I_{SSCH} \bullet T_{SS}}{V_{FB}} = 3 \bullet \frac{4\mu A \bullet T_{SS}}{0.85V}$$

where T_{SS} is the soft-start time, $I_{SS\ CH}$ the charging current and V_{FB} the reference of the error amplifier.

The soft-start block supports the precharged output capacitor.

Figure 6. Soft-start phase with precharged C_{OUT}



During normal operation a new soft-start cycle takes place in case of:

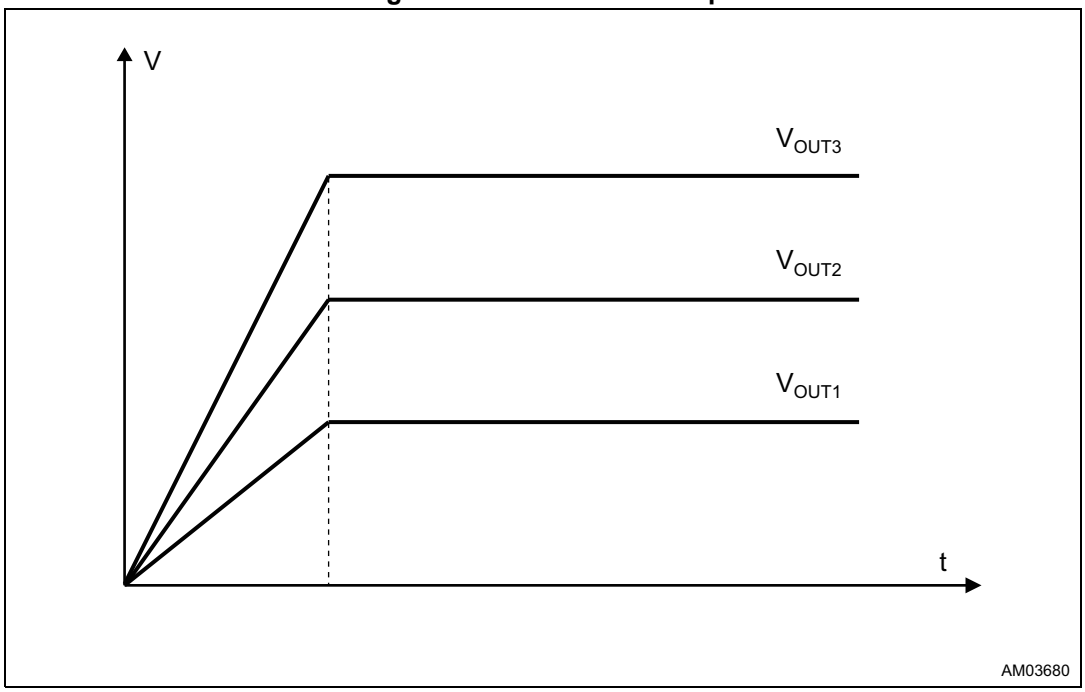
- Thermal shutdown event
- UVLO event
- The device is driven in $\overline{INH}$ mode

The soft-start capacitor is discharged with a 0.6 mA typ. current capability for 1 msec time max. For complete and proper capacitor discharge in case of fault condition, a maximum C_{SS} = 67 nF value is suggested.

5.3.1 Ratiometric startup

The ratiometric startup is implemented sharing the same soft-start capacitor for a set of the R6986 device.

Figure 7. Ratiometric startup



As a consequence all the internal current generators charge in parallel the external capacitor. The capacitor value is dimensioned accordingly with *Equation 2*:

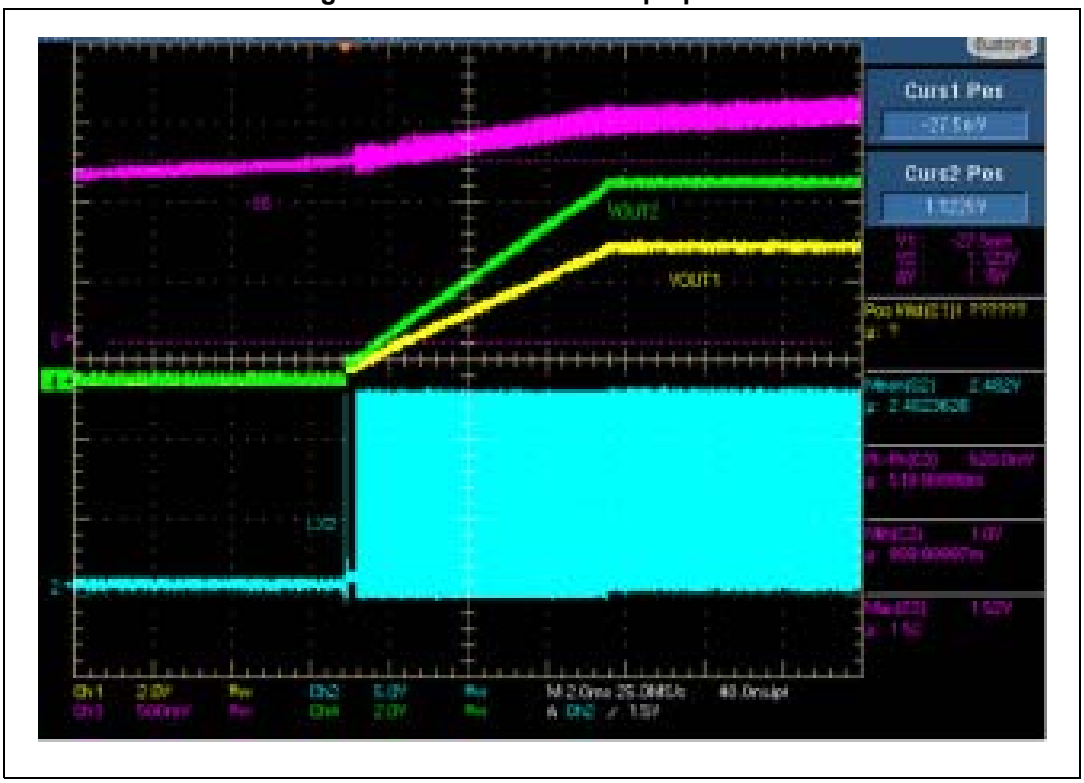
Equation 2

$$C_{SS} = n_{A6986} \bullet SS_{GAIN} \bullet \frac{I_{SSCH} \bullet T_{SS}}{V_{FB}} = n_{R6986} \bullet 3 \bullet \frac{4\mu A \bullet T_{SS}}{0.85V}$$

where n_{R6986} represents the number of devices connected in parallel.

For better tracking of the different output voltages the synchronization of the set of regulators is suggested.

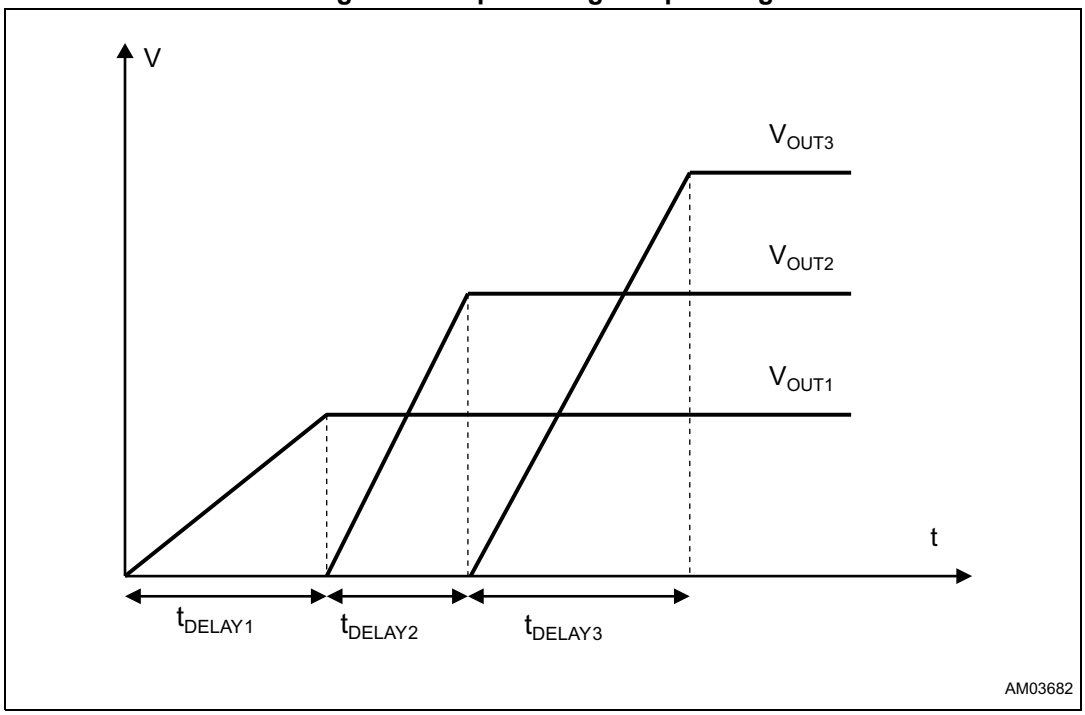
Figure 8. Ratiometric startup operation



5.3.2 Output voltage sequencing

The R6986 device implements sequencing connecting the RST pin of the master device to the SS/$\overline{INH}$ of the slave. The slave is inhibited as long as the master output voltage is outside regulation so implementing the sequencing (see *Figure 9*).

Figure 9. Output voltage sequencing



High flexibility is achieved thanks to the programmable RST thresholds (see *Table 7: LNM / LCM selection on page 12*) and programmable delay time. To minimize the component count the DELAY pin capacitor can be also omitted so the pin works as a normal power good.

5.4 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (0.85 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage.

Table 8. Uncompensated error amplifier characteristics

Description	Values
Transconductance	155 µS
Low frequency gain	100 dB

The error amplifier output is compared with the inductor current sense information to perform PWM control. The error amplifier also determines the burst operation at light load when the LCM is active.

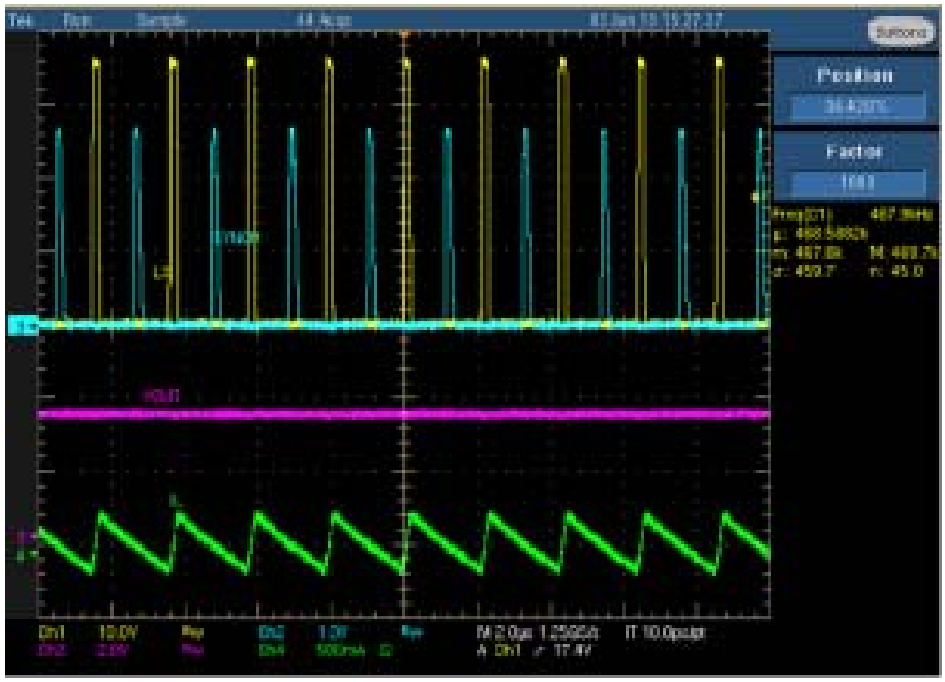
5.5 Light load operation

The MLF pinstrapping during the power-up phase determines the light load operation (refer to *Table 7: LNM / LCM selection on page 12*).

5.5.1 Low noise mode (LNM)

The low noise mode implements a forced PWM operation over the different loading conditions. The LNM features a constant switching frequency to minimize the noise in the final application and a constant voltage ripple at fixed V_{IN}. The regulator in steady loading condition never skip pulses and it operates in continuous conduction mode (CCM) over the different loading conditions.

Figure 10. Low noise mode operation



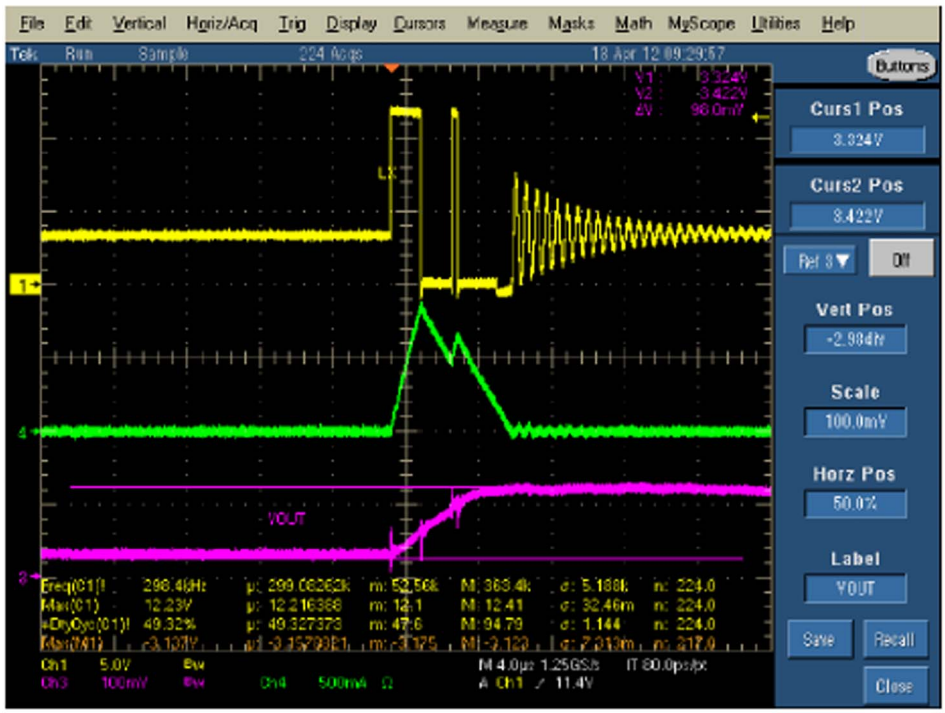
5.5.2 Low consumption mode (LCM)

The low consumption mode maximizes the efficiency at light load. The regulator prevents the switching activity whenever the switch peak current request is lower than the I_{SKIP} threshold (700 mA typical). As a consequence the R6986 device works in bursts and it minimizes the quiescent current request in the meantime between the switching operation.

In order to minimize the regulator quiescent current request from the input voltage, the V_{BIAS} pin can be connected to an external voltage source in the range 3 V < V_{BIAS} < 5.5 V (see *Section 5.1: Power supply and voltage reference on page 15*).

In case the V_{BIAS} pin is connected to the regulated output voltage (VOUT), the total current drawn from the input voltage can be calculated as:

Figure 11. LCM operation at zero load



Given the energy stored in the inductor during a burst, the voltage ripple depends on the capacitor value:

Equation 3

$$V_{OUT\ RIPPLE} = \frac{\Delta Q_{IL}}{C_{OUT}} = \frac{\int_0^{T_{BURST}} (i_L(t) \cdot dt)}{C_{OUT}}$$

Figure 12. LCM operation over loading condition (part 1)

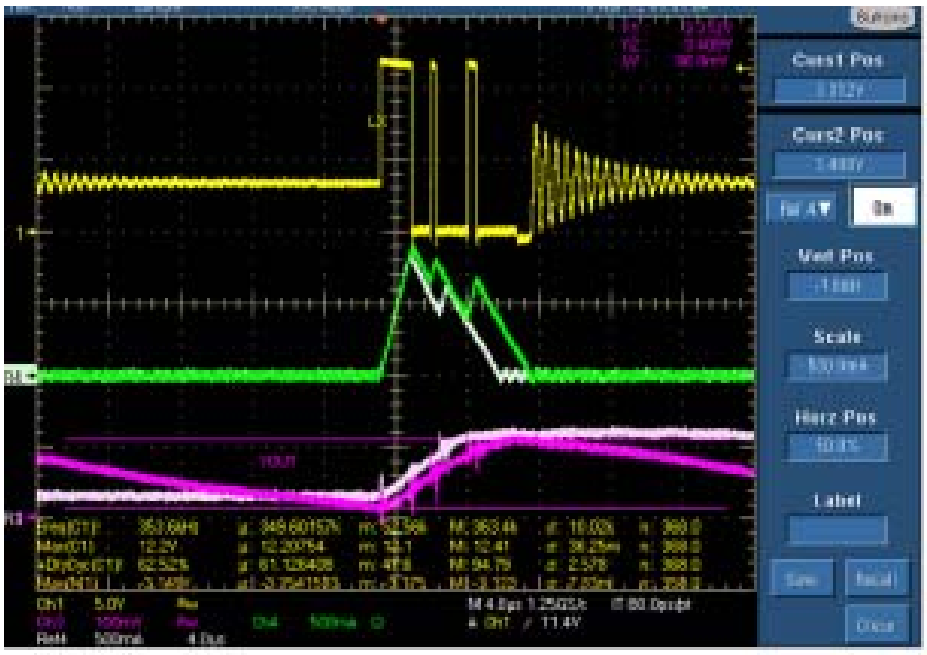


Figure 13. LCM operation over loading condition (part 2)

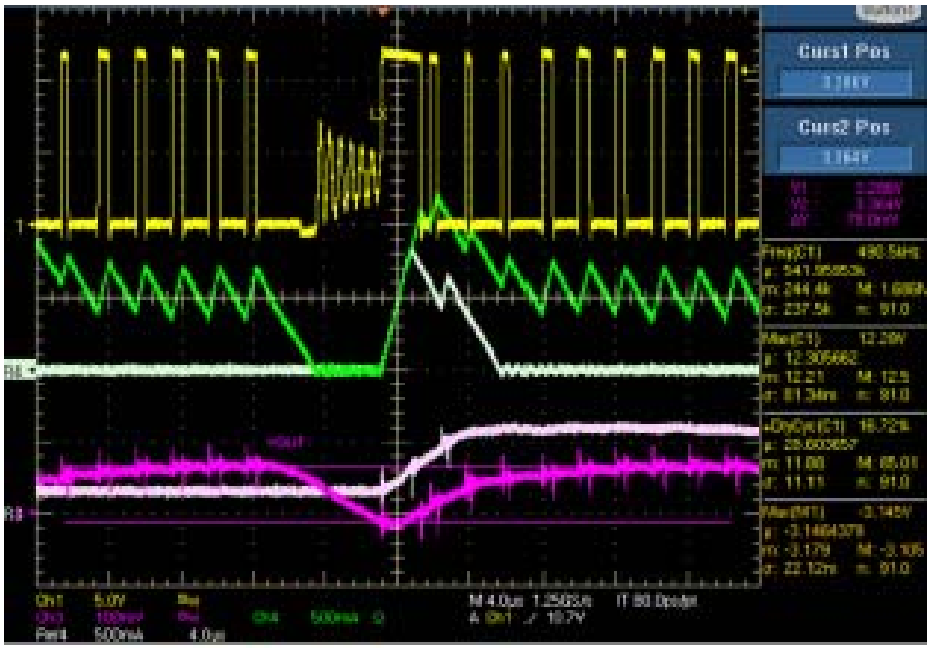
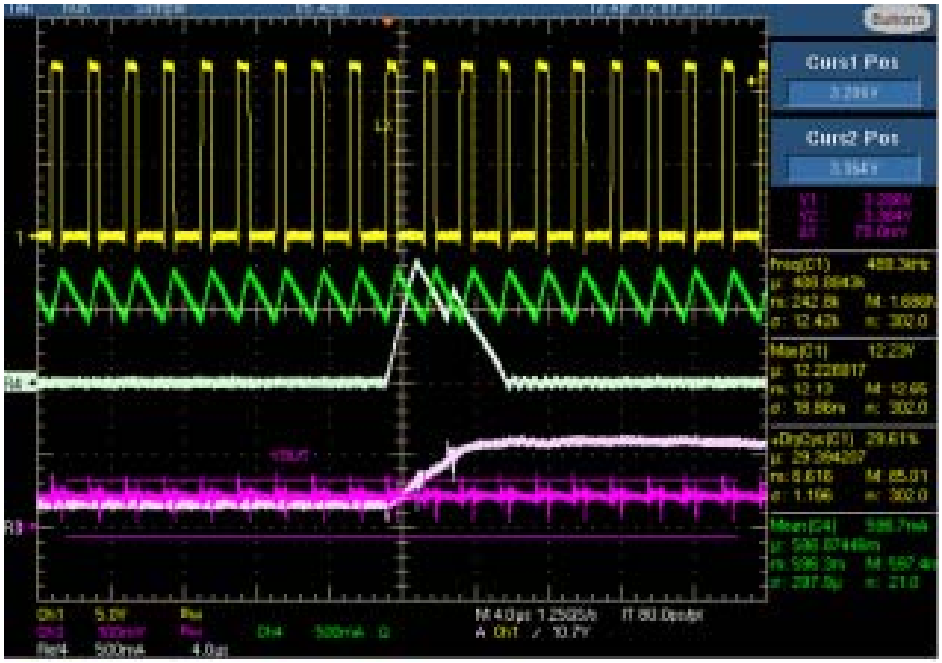


Figure 14. The regulator works in CCM



5.6 Switchover feature

The switchover maximizes the efficiency at light load that is crucial for LCM applications.

5.6.1 LCM

The LCM operation satisfies the high efficiency requirements of the battery powered applications. In order to minimize the regulator quiescent current request from the input voltage, the V_{BIAS} pin can be connected to an external voltage source in the range $3\ V < V_{BIAS} < 5.5\ V$ (see *Section 5.1: Power supply and voltage reference on page 15*).

In case the V_{BIAS} pin is connected to the regulated output voltage (V_{OUT}), the total current drawn from the input voltage can be calculated as:

Equation 4

$$I_{QVIN} = I_{QOPVIN} + \frac{1}{\eta_{R6986}} \bullet \frac{V_{BIAS}}{V_{IN}} \bullet I_{QOPVBIAS}$$

where *IQ OP V_{IN}*, *IQ OP V_{BIAS}* are defined in *Table 5: Electrical characteristics on page 8* and η_{R6986} is the efficiency of the conversion in the working point.

5.6.2 LNM

Equation 4 is also valid when the device works in LNM and it can increase the efficiency at medium load since the regulator always operates in continuous conduction mode.

5.7 Overcurrent protection

The current protection circuitry features a constant current protection, so the device limits the maximum peak current (see *Table 5: Electrical characteristics on page 8*) in overcurrent condition.

The R6986 device implements a pulse by pulse current sensing on both power elements (high-side and low-side switches) for effective current protection over the duty cycle range. The high-side current sensing is called “peak” the low-side sensing “valley”.

The internal noise generated during the switching activity makes the current sensing circuitry ineffective for a minimum conduction time of the power element. This time is called “masking time” because the information from the analog circuitry is masked by the logic to prevent an erroneous detection of the overcurrent event. As a consequence, the peak current protection is disabled for a masking time after the high-side switch is turned on, the valley for a masking time after the low-side switch is turned on. In other words, the peak current protection can be ineffective at extremely low duty cycles, the valley current protection at extremely high duty cycles.

The R6986 device assures an effective overcurrent protection sensing the current flowing in both power elements. In case one of the two current sensing circuitry is ineffective because of the masking time, the device is protected sensing the current on the opposite switch. Thus, the combination of the “peak” and “valley” current limits assure the effectiveness of the overcurrent protection even in extreme duty cycle conditions.

The valley current threshold is designed higher than the peak to guarantee a proper operation. In case the current diverges because of the high-side masking time, the low-side power element is turned on until the switch current level drops below the valley current sense threshold. The low-side operation is able to prevent the high-side turn on, so the device can skip pulses decreasing the swathing frequency.

Figure 15. Valley current sense operation in overcurrent condition

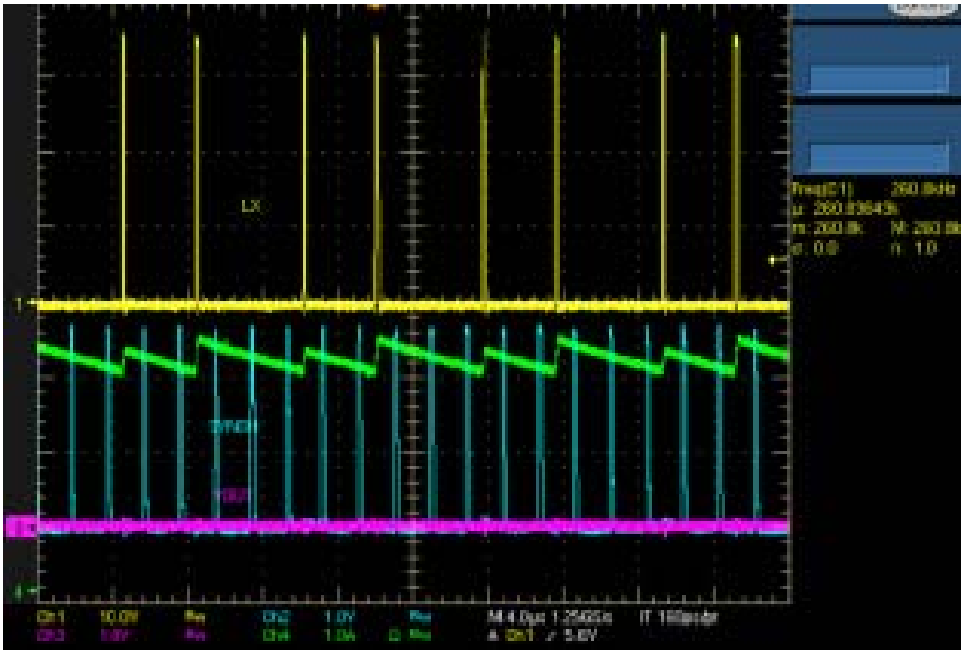


Figure 15 shows the switching frequency reduction during the valley current sense operation in case of extremely low duty cycle (V_{IN} 38 V, f_{SW} = 500 kHz short-circuit condition).

In worst case scenario (like *Figure 15*) of the overcurrent protection the switch current is limited to:

Equation 5

$$I_{MAX} = I_{VALLEYTH} + \frac{V_{IN} - V_{OUT}}{L} \bullet T_{MASKHS}$$

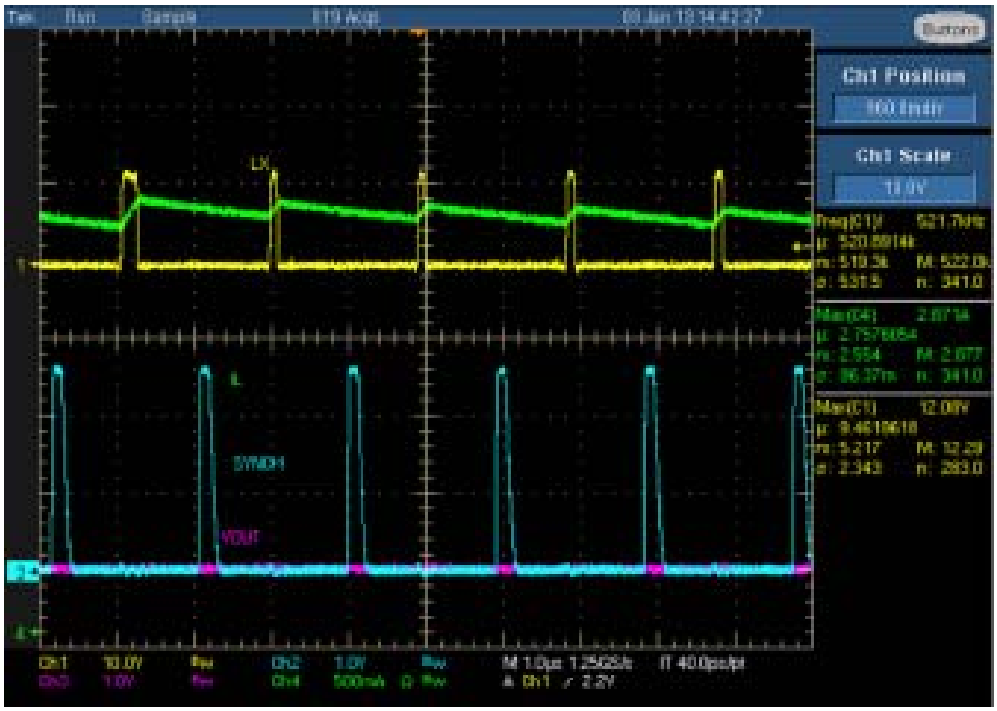
where I_{VALLEY_TH} is the current threshold of the valley sensing circuitry (see *Table 5: Electrical characteristics on page 8*) and T_{MASK_HS} is the masking time of the high-side switch 100 nsec. typ.).

In most of the overcurrent conditions the conduction time of the high-side switch is higher than the masking time and so the peak current protection limits the switch current.

Equation 6

$$I_{MAX} = I_{PEAK\_TH}$$

Figure 16. Peak current sense operation in overcurrent condition



The DC current flowing in the load in overcurrent condition is:

Equation 7

$$I_{DCOC}(V_{OUT}) = I_{MAX} - \frac{I_{RIPPLE}(V_{OUT})}{2} = I_{MAX} - \left(\frac{V_{IN} - V_{OUT}}{2 \bullet L} \bullet T_{ON}\right)$$

OCP and switchover feature

Output capacitor discharging the current flowing to ground during heavy short-circuit events is only limited by parasitic elements like the output capacitor ESR and short-circuit impedance.

Due to parasitic inductance of the short-circuit impedance, negative output voltage oscillations can be generated with huge discharging current levels (see *Figure 17*).

Figure 17. Output voltage oscillations during heavy short-circuit

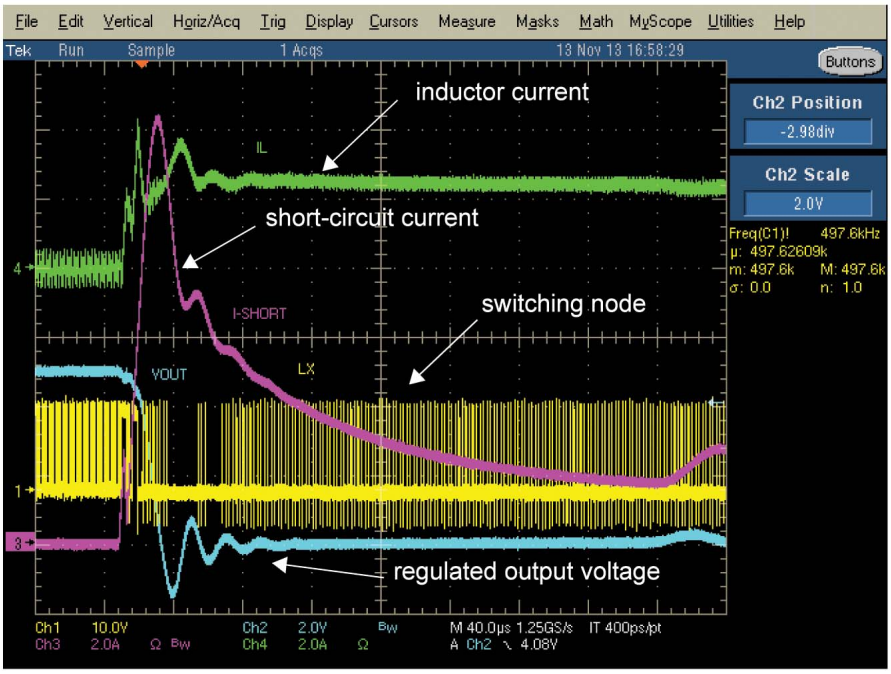
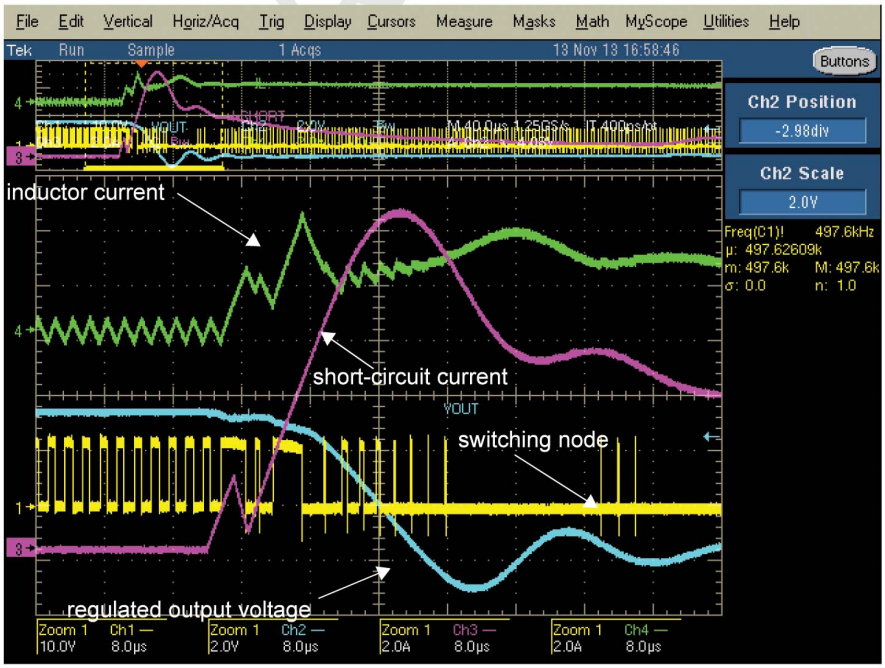


Figure 18. Zoomed waveform

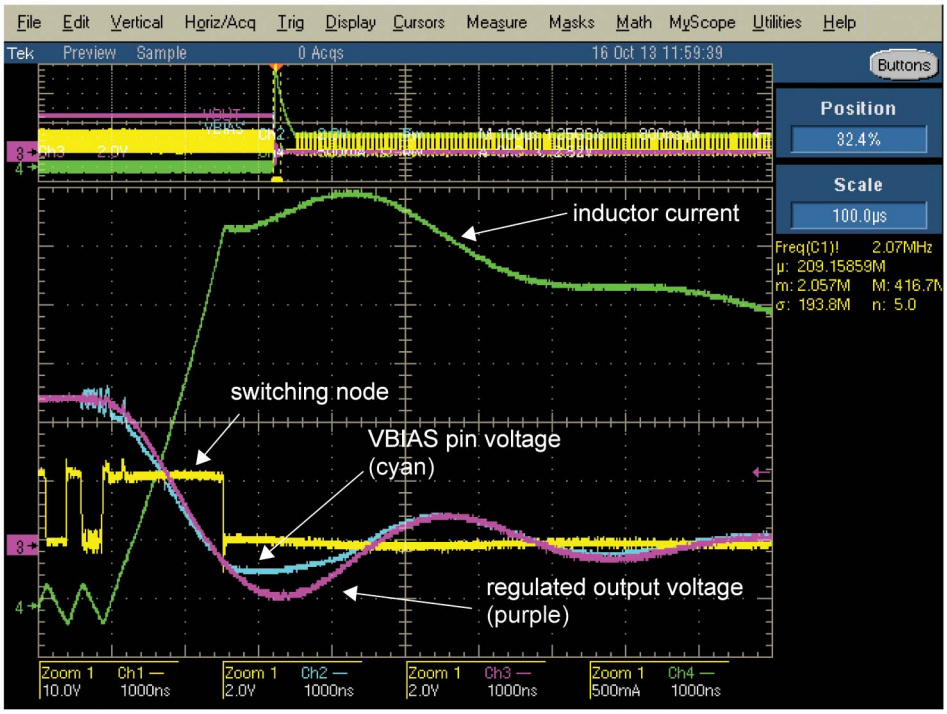


The V_{BIAS} pin absolute maximum ratings (see *Table 2: Absolute maximum ratings on page 6*) must be satisfied over the different dynamic conditions.

If V_{BIAS} is connected to GND there are no issues (see *Figure 17* and *Figure 18*).

A small resistor value (few ohms) in series with V_{BIAS} can help to limit the pin negative voltage (see *Figure 19*) during heavy short-circuit events if it is connected to the regulated output voltage.

Figure 19. V_{BIAS} in heavy short-circuit event



5.8 Overvoltage protection

The overvoltage protection monitors the FB pin and enables the low-side MOSFET to discharge the output capacitor if the output voltage is 20% over the nominal value.

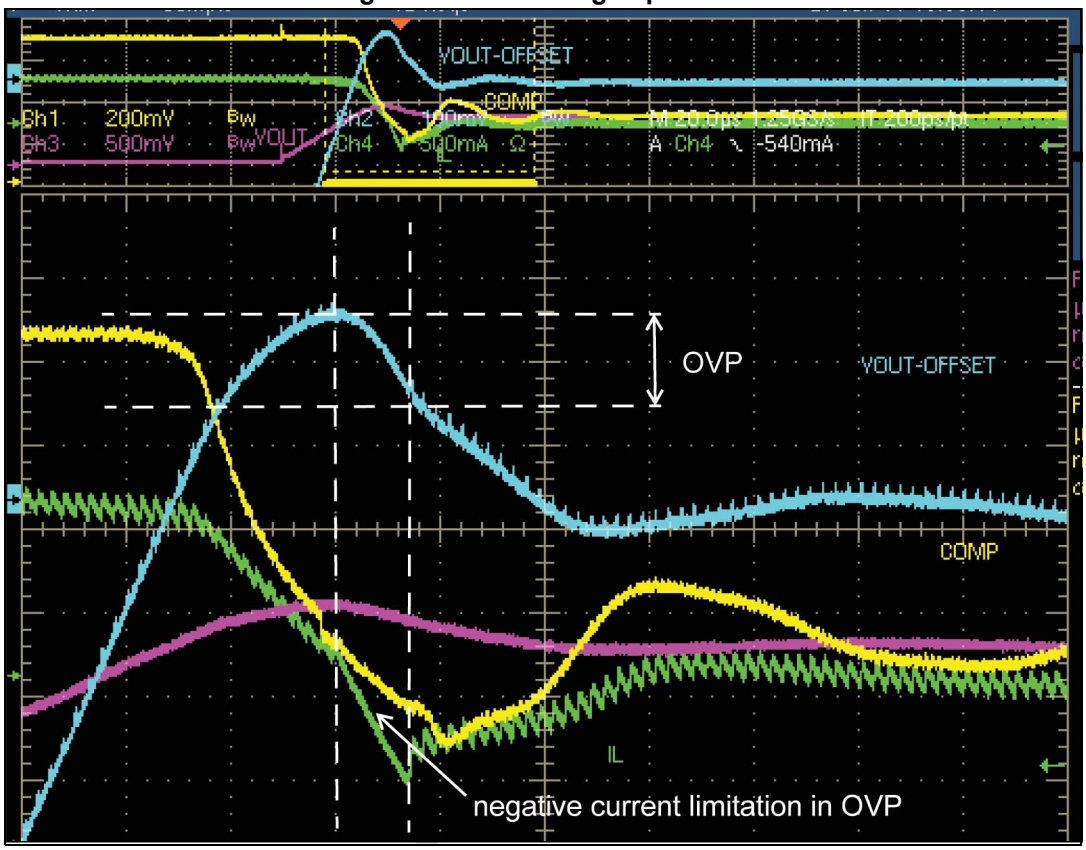
This is a second level protection and should never be triggered in normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance determined by the compensation network should guarantee an output voltage regulation within the overvoltage threshold even during the worst case scenario in term of load transitions.

The protection is reliable and also able to operate even during normal load transitions for a system whose dynamic performance is not in line with the load dynamic request. As a consequence the output voltage regulation would be affected.

Figure 20 shows the overvoltage operation during a negative steep load transient for a system designed with huge inductor value and small output capacitor. The inductor value limits the switch current slew rate and the extra charge flowing into the small capacitor value generates an overvoltage event. This can be considered as an example for a system with dynamic performance not in line with the load request.

The R6986 device implements a 1 A typ. negative current limitation to limit the maximum reversed switch current during the overvoltage operation.

Figure 20. Overvoltage operation

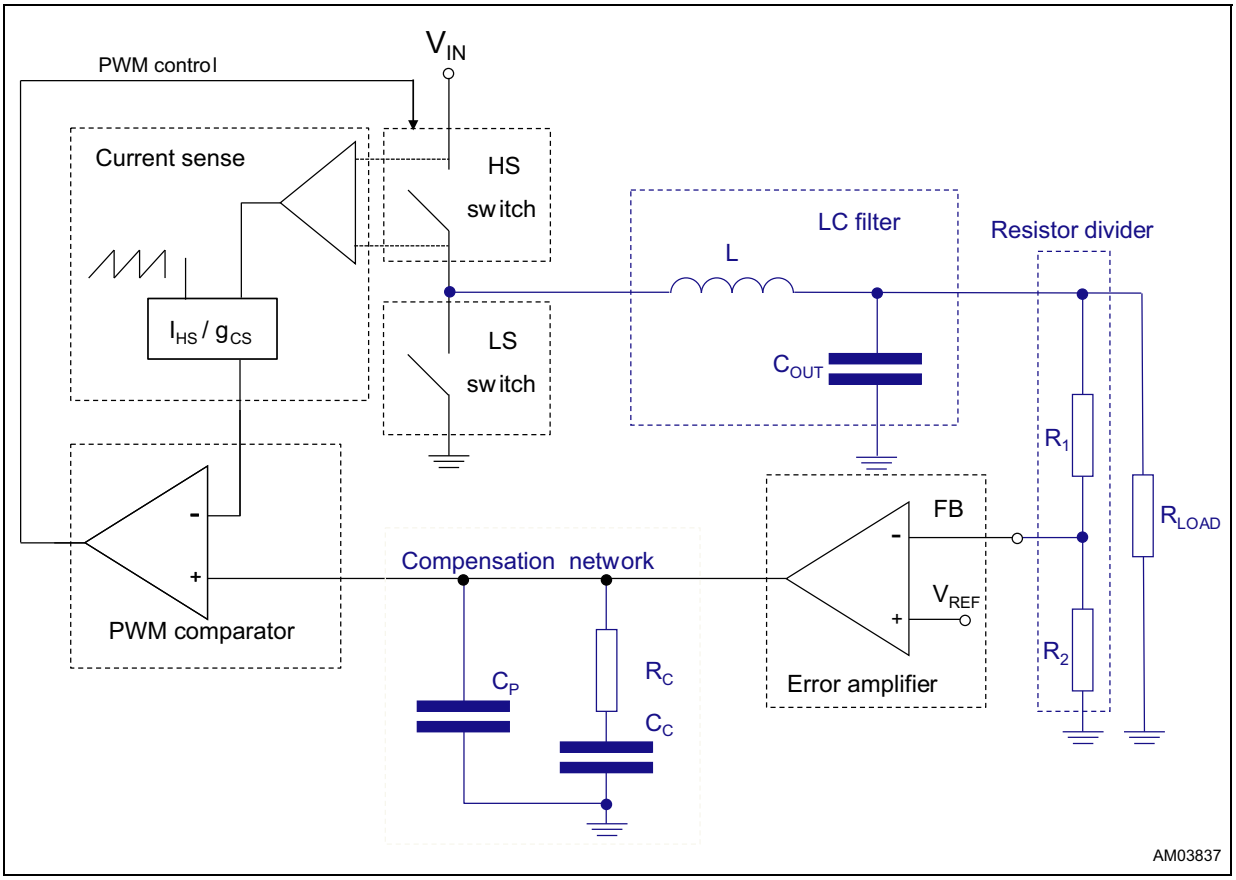


5.9 Thermal shutdown

The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold (165 °C typical). The thermal sensing element is close to the power elements, ensuring fast and accurate temperature detection. A hysteresis of approximately 30 °C prevents the device from turning ON and OFF continuously. When the thermal protection runs away a new soft-start cycle will take place.

6 Closing the loop

Figure 21. Block diagram of the loop



6.1 $G_{CO}(s)$ control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as:

Equation 8

$$G_{CO(s)} = \frac{R_{LOAD}}{R_i} \bullet \frac{1}{1 + \frac{R_{LOAD} \bullet T_{SW}}{L} \bullet [m_C \bullet (1 - D) - 0.5]} \bullet \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \bullet F_H(s)$$

where R_{LOAD} represents the load resistance, R_i the equivalent sensing resistor of the current sense circuitry, ω_p the single pole introduced by the the power stage and ω_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

Equation 9

$$\omega_z = \frac{1}{ESR \bullet C_{OUT}}$$

Equation 10

$$\omega_p = \frac{1}{R_{LOAD} \bullet C_{OUT}} + \frac{m_c \bullet (1 - D) - 0.5}{L \bullet C_{OUT} \bullet f_{SW}}$$

where:

Equation 11

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = V_{PP} \cdot g_{CS} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \end{cases}$$

S_n represents the on time slope of the sensed inductor current, S_e the on time slope of the external ramp (V_{PP} peak-to-peak amplitude) that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

S_e can be calculated from the parameter $V_{PP} \cdot g_{CS}$ given in *Table 5 on page 8*.

The sampling effect contribution $F_H(s)$ is:

Equation 12

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \bullet Q_p} + \frac{s^2}{\omega_n^2}}$$

where:

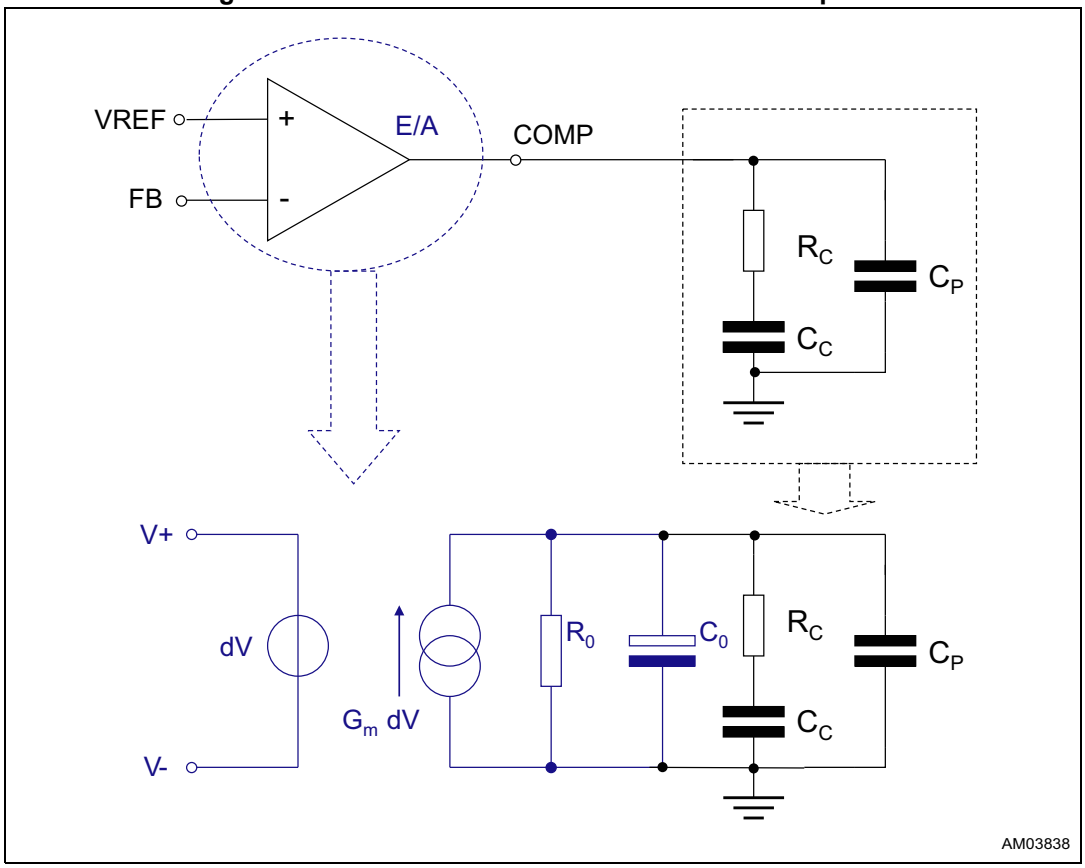
Equation 13

$$Q_p = \frac{1}{\pi \bullet [m_c \bullet (1 - D) - 0.5]}$$

6.2 Error amplifier compensation network

The typical compensation network required to stabilize the system is shown in *Figure 22*.

Figure 22. Transconductance embedded error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability but it is useful to reduce the noise at the output of the error amplifier.

The transfer function of the error amplifier and its compensation network is:

Equation 14

$$A_0(s) = \frac{A_{V0} \bullet (1 + s \bullet R_c \bullet C_c)}{s^2 \bullet R_0 \bullet (C_0 + C_p) \bullet R_c \bullet C_c + s \bullet (R_0 \bullet C_c + R_0 \bullet (C_0 + C_p) + R_c \bullet C_c) + 1}$$

Where $A_{vo} = G_m \cdot R_o$

The poles of this transfer function are (if $C_c >> C_0 + C_P$):

Equation 15

$$f_{PLF} = \frac{1}{2 \bullet \pi \bullet R_0 \bullet C_c}$$

Equation 16

whereas the zero is defined as:

$$f_{PHF} = \frac{1}{2 \bullet \pi \bullet R_0 \bullet (C_0 + C_p)}$$

Equation 17

$$f_Z = \frac{1}{2 \bullet \pi \bullet R_c \bullet C_c}$$

6.3 Voltage divider

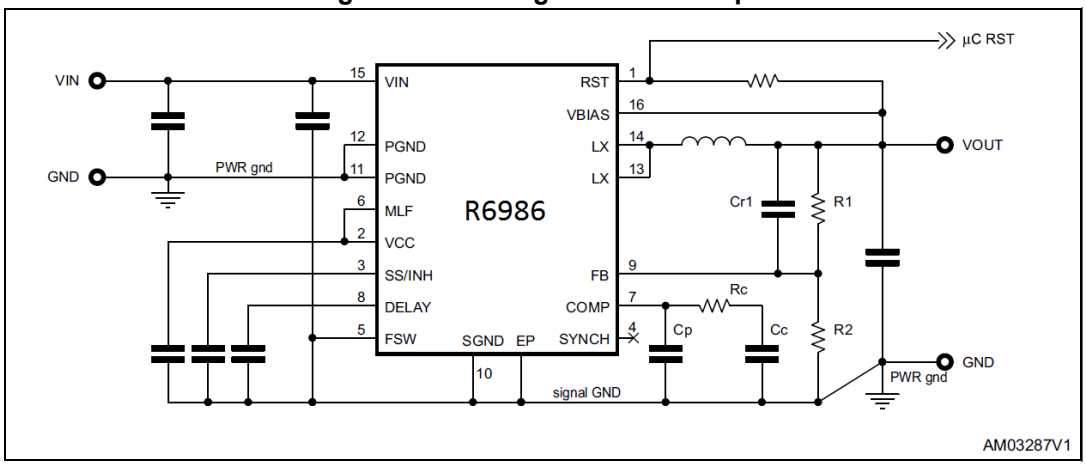
The contribution of a simple voltage divider is:

Equation 18

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2}$$

A small signal capacitor in parallel to the upper resistor (see *Figure 23*) of the voltage divider implements a leading network ($f_{zero} < f_{pole}$), sometimes necessary to improve the system phase margin:

Figure 23. Leading network example



Laplace transformer of the leading network:

Equation 19

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} \bullet \frac{(1 + s + R_1 \bullet C_{R1})}{\left(1 + s \bullet \frac{R_1 \bullet R_2}{R_1 + R_2} \bullet C_{R1}\right)}$$

where:

Equation 20

$$f_Z = \frac{1}{2 \bullet \pi \bullet R_1 \bullet C_{R1}}$$

$$f_p = \frac{1}{2 \bullet \pi \bullet \frac{R_1 \bullet R_2}{R_1 + R_2} \bullet C_{R1}}$$

$$f_Z < f_p$$

6.4 Total loop gain

In summary, the open loop gain can be expressed as:

Equation 21

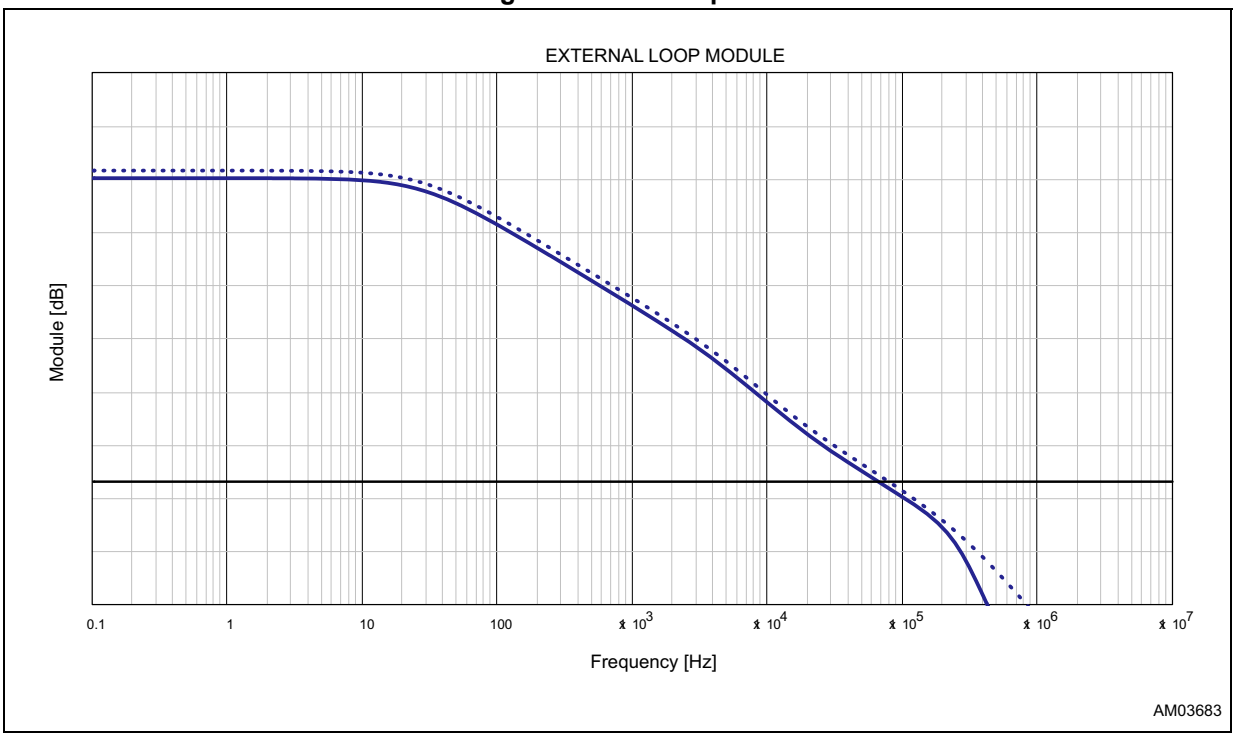
$$G(s) = G_{DIV}(s) \cdot G_{CO}(s) \cdot A_0(s)$$

Example 1

$$V_{IN} = 12\ V,\ V_{OUT} = 3.3\ V,\ R_{OUT} = 2.2\ \Omega$$

Selecting L = 6.8 µH, C_{OUT} = 15 µF and ESR = 1 mΩ, R_C= 68 kΩ, C_C= 180 pF, C_P = 6.8 pF (please refer to *Example 2*), the gain and phase bode diagrams are plotted respectively in *Figure 24* and *Figure 25*.

Figure 24. Module plot

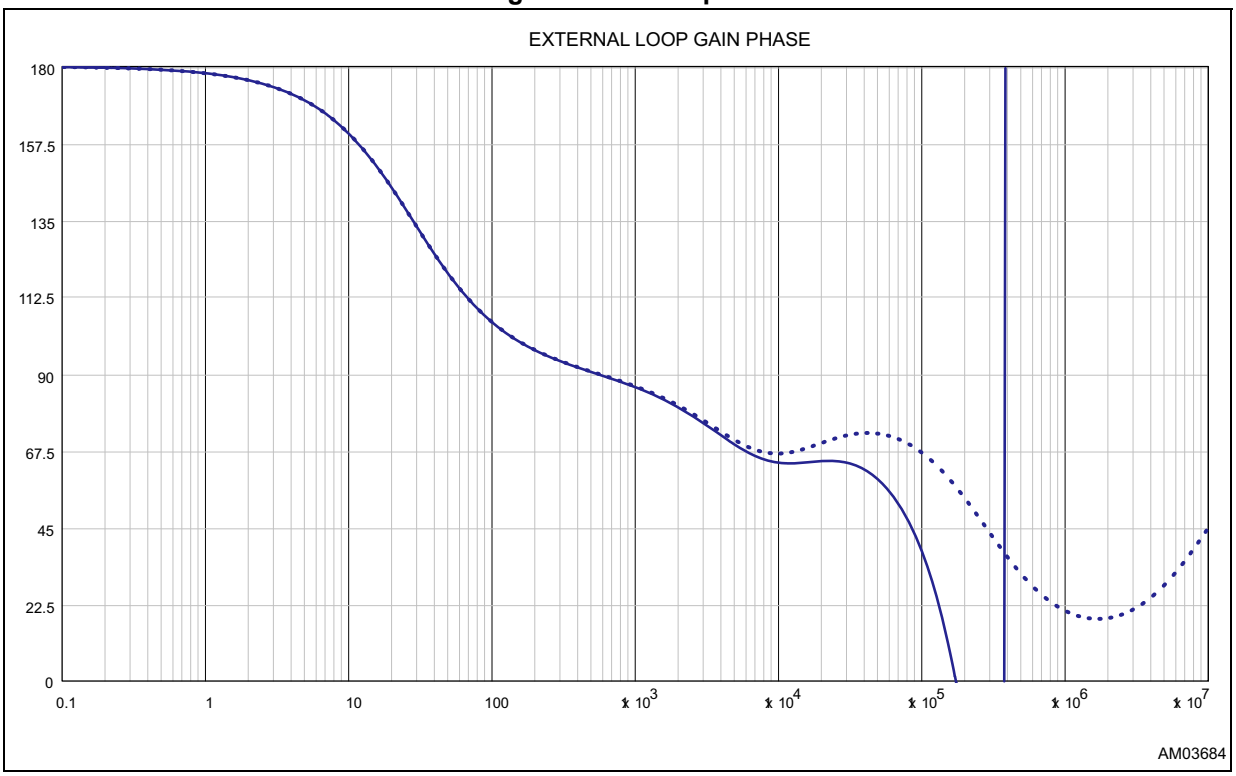


Equation 22

$$BW = 67kHz$$

$$\text{phase margin} = 53^0$$

Figure 25. Phase plot



The blue solid trace represents the transfer function including the sampling effect term (see *Equation 12 on page 33*), the dotted blue trace neglects the contribution.

6.5 Compensation network design

The maximum bandwidth of the system can be designed up to $f_{SW}/6$ to guarantee a valid small signal model.

Equation 23

$$BW = \frac{f_{SW}}{6}$$

Equation 24

$$R_C = \frac{2 \cdot \pi \cdot BW \cdot C_{OUT} \cdot V_{OUT}}{0.85V \cdot g_{CS} \cdot g_{m\,TYP}}$$

where:

Equation 25

$$f_{POLE} = \frac{\omega_p}{2 \cdot \pi}$$

ω_p is defined by *Equation 10 on page 33*, g_{CS} represents the current sense transconductance (see *Table 5: Electrical characteristics on page 8*) and $g_{m\ TYP}$ the error amplifier transconductance.

Equation 26

$$C_C = \frac{5}{2 \cdot \pi \cdot R_C \cdot BW}$$

Example 2

Considering V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 6.8 µH, C_{OUT} = 15 µF, f_{SW} = 500 kHz.

The maximum system bandwidth is 80 kHz. Assuming to design the compensation network to achieve a system bandwidth of 70 kHz:

Equation 27

$$f_{POLE} = 6kHz$$

Equation 28

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT}} = 2.2\Omega$$

so accordingly with *Equation 24* and *Equation 26*:

Equation 29

$$R_C = 68k\Omega$$

Equation 30

$$C_C = 168pF \approx 180pF$$

7 Application notes

7.1 Output voltage adjustment

The error amplifier reference voltage is 0.85 V typical.

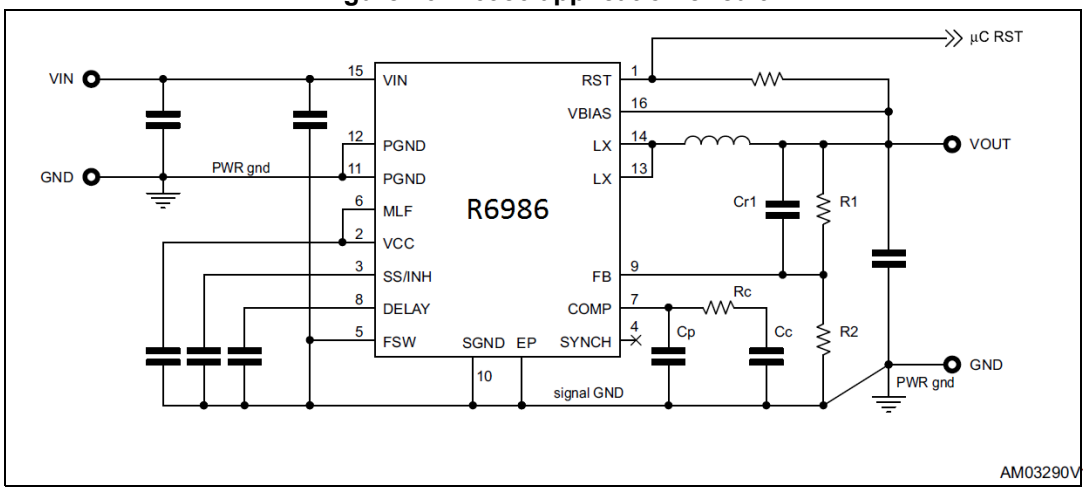
The output voltage is adjusted accordingly with *Equation 31* (see *Figure 26*):

Equation 31

$$V_{OUT} = 0.85 \bullet \left(1 + \frac{R_1}{R_2}\right)$$

C_{r1} capacitor is sometimes useful to increase the small signal phase margin (please refer to *Section 6.5: Compensation network design*).

Figure 26. R6986 application circuit



7.2 Switching frequency

A resistor connected to the FSW pin features the selection of the switching frequency. The pinstrapping is performed at power-up, before the soft-start takes place. The FSW pin is pinstrapped and then driven floating in order to minimize the quiescent current from VIN.

Please refer to *Table 6: f_{SW} selection on page 11* to identify the pull-up / pull-down resistor value. f_{SW} = 250 kHz / f_{SW} = 500 kHz preferred codifications don't require any external resistor.

7.3 MLF pin

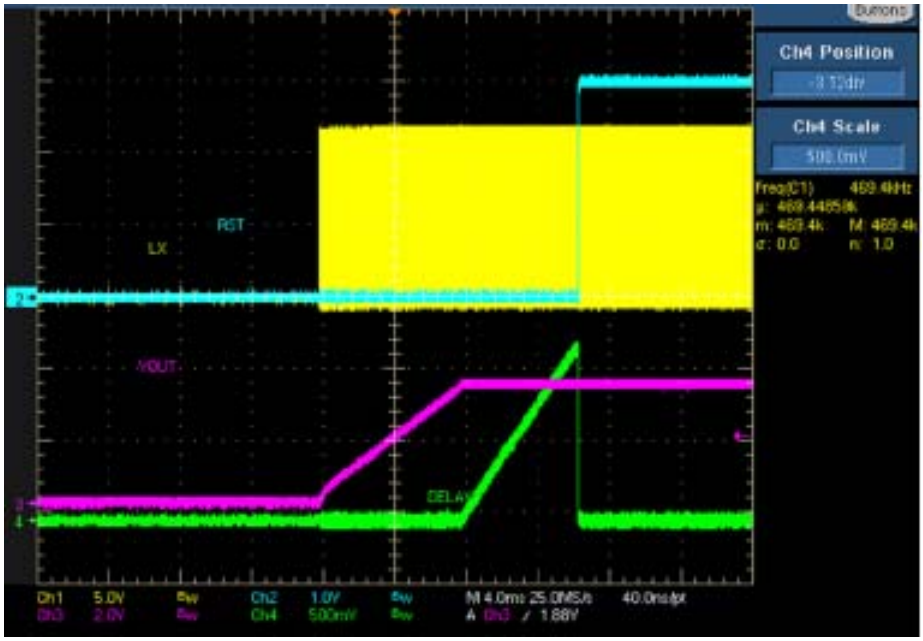
A resistor connected to the MLF pin features the selection of the between low noise mode / low consumption mode and the different RST thresholds. The pinstrapping is performed at power-up, before the soft-start takes place. The FSW pin is pinstrapped and then driven floating in order to minimize the quiescent current from VIN.

Please refer to *Table 7: LNM / LCM selection on page 12* to identify the pull-up / pull-down resistor value. (LNM, RST threshold 93%) / (LCM, RST threshold 93%) preferred codifications don't require any external resistor.

7.4 Voltage supervisor

The embedded voltage supervisor (composed of the RST and the DELAY pins) monitors the regulated output voltage and keeps the RST open collector output in low impedance as long as the V_{OUT} is out of regulation. In order to ensure a proper reset of digital devices with a valid power supply, the device can delay the RST assertion with a programmable time.

Figure 27. Voltage supervisor operation



The comparator monitoring the FB voltage has four different programmable thresholds (80%, 87%, 93%, 96% nominal output voltage) for high flexibility (see *Section 7.3: MLF pin* and *Table 7: LNM / LCM selection on page 12*).

When the RST comparator detects the output voltage is in regulation, a 2 µA internal current source starts to charge an external capacitor to implement a voltage ramp on the DELAY pin. The RST open collector is then released as soon as V_{DELAY} = 1.234 V (see *Figure 27*).

The CDELAY is dimensioned accordingly with *Equation 32*:

Equation 32

$$C_{DELAY} = \frac{I_{SSCH} \bullet T_{DELAY}}{V_{DELAY}} = \frac{2\mu A \bullet T_{DELAY}}{1.234V}$$

The maximum suggested capacitor value is 270 nF.

7.5 Synchronization (LNM)

Beating frequency noise is an issue when multiple switching regulators populate the same application board. The R6986 synchronization circuitry features the same switching frequency for a set of regulators simply connecting their SYNCH pin together, so preventing beating noise. The master device provides the synchronization signal to the others since the SYNCH pin is I/O able to deliver or recognize a frequency signal.

For proper synchronization of multiple regulators, all of them have to be configured with the same switching frequency (see *Table 6 on page 11*), so the same resistor connected at the FSW pin.

In order to minimize the RMS current flowing through the input filter, the R6986 device provides a phase shift of 180° between the master and the SLAVES. If more than two devices are synchronized, all slaves will have a common 180° phase shift with respect to the master.

Considering two synchronized R6986 which regulates the same output voltage (i.e.: operating with the same duty cycle), the input filter RMS current is optimized and is calculated as:

Equation 33

$$I_{RMS} = \begin{cases} \frac{I_{OUT}}{2} \cdot \sqrt{2D \cdot (1 - 2D)} & \text{if } D < 0.5 \\ \frac{I_{OUT}}{2} \cdot \sqrt{(2D - 1) \cdot (2 - 2D)} & \text{if } D > 0.5 \end{cases}$$

Figure 28 shows two regulators not synchronized.

Figure 28. Two regulators not synchronized

Figure 29 shows the same regulators working synchronized. The MASTER regulator (LX2 trace) delivers the synchronization signal (SYNCH1, SYNCH2 pins are connected together) to the SLAVE device (LX1). The SLAVE regulator works in phase with the synchronization signal which is out of phase with the MASTER switching operation.

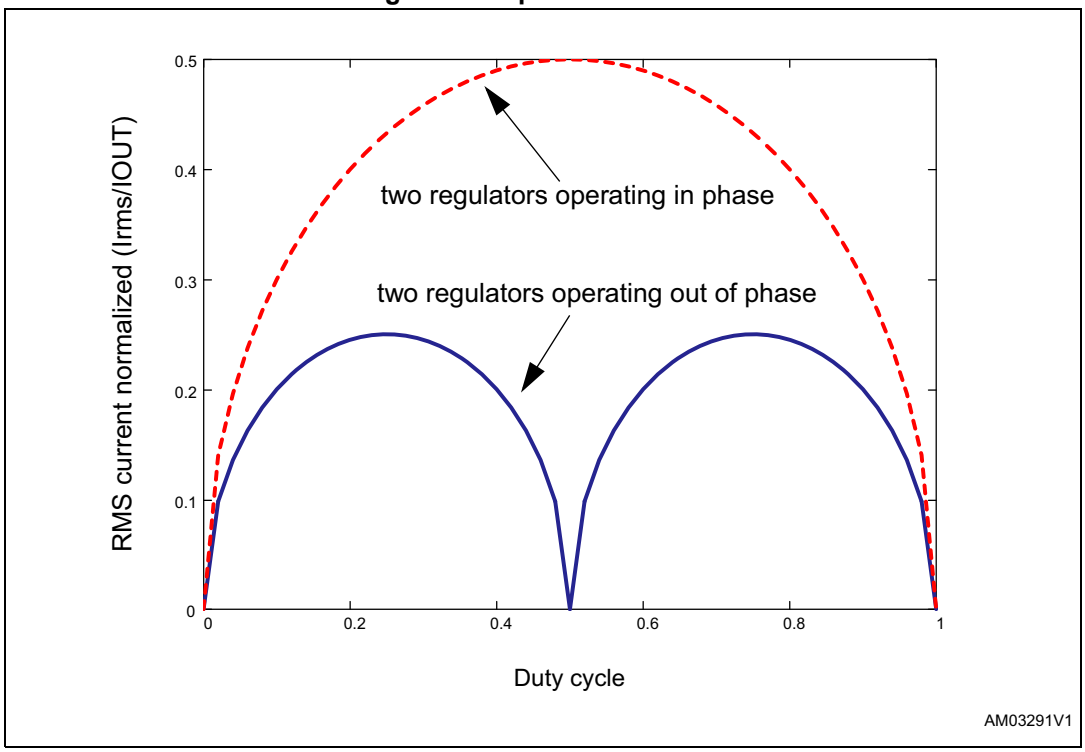
Figure 29. Two regulators synchronized

Multiple R6986 can be synchronized to an external frequency signal fed to the SYNCH pin. In this case the set is phased to the reference and all the devices will work with 0° phase shift.

Since the slope compensation contribution, that is required to prevent subharmonic oscillations in peak current mode architecture, depends on the switching frequency, it is important to select the same switching frequency for all regulators (all of them operate as SLAVE) one step lower than the reference signal (please refer to *Table 6: f_{SW} selection on page 11*). As a consequence, all the regulators have the same resistor connected to the FSW pin.

The graphical representation of the input RMS current of the input filter in the case of two devices with 0° phase shift (synchronized to an external signal) or 180° phase shift (synchronized connecting their SYNCH pins) regulating the same output voltage is provided in *Figure 30*. To dimension the proper input capacitor please refer to *Section 7.6.1: Input capacitor selection*.

Figure 30. Input RMS current



7.6 Design of the power components

7.6.1 Input capacitor selection

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity a pulsed current flows into the input capacitor and so its RMS current capability must be selected accordingly with the application conditions. Internal losses of the input filter depends on the ESR value so usually low ESR capacitors (like multilayer ceramic capacitors) have higher RMS current capability. On the other hand, given the RMS current value, lower ESR input filter has lower losses and so contributes to higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

Equation 34

$$I_{RMS} = I_{OUT} \bullet \sqrt{\left(1 - \frac{D}{\eta}\right) \bullet \frac{D}{\eta}}$$

Where I_{OUT} is the maximum DC output current, D is the duty cycles, η is the efficiency. This function has a maximum at D = 0.5 and, considering η = 1, it is equal to Io/2.

In a specific application the range of possible duty cycles has to be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

Equation 35

$$D_{MAX} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INMIN} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}}$$

Equation 36

$$D_{MIN} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INMAX} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}}$$

Where ΔV_{HIGH_SIDE} and ΔV_{LOW_SIDE} are the voltage drops across the embedded switches. The peak to peak voltage across the input filter can be calculated as:

Equation 37

$$V_{PP} = \frac{I_{OUT}}{C_{IN} \bullet f_{SW}} \bullet \left(1 - \frac{D}{\eta}\right) \bullet \frac{D}{\eta} + ESR \bullet (I_{OUT} + \Delta I_L)$$

In case of negligible ESR (MLCC capacitor) the equation of CIN as a function of the target VPP can be written as follows:

Equation 38

$$C_{IN} = \frac{I_{OUT}}{V_{PP} \bullet f_{SW}} \bullet \left(1 - \frac{D}{\eta}\right) \bullet \frac{D}{\eta}$$

Considering $\eta = 1$ this function has its maximum in D = 0.5:

Equation 39

$$C_{INMIN} = \frac{I_{OUT}}{4 \bullet V_{PPMAX} \bullet f_{SW}}$$

Typically C_{IN} is dimensioned to keep the maximum peak-peak voltage across the input filter in the order of 5% V_{IN_MAX}.

Table 9. Input capacitors

Manufacturer	Series	Size	Cap value (µF)	Rated voltage (V)
TDK	C3225X7S1H106M	1210	10	50
	C3216X5R1H106M	1206		
Taiyo Yuden	UMK325BJ106MM-T	1210		

7.6.2 Inductor selection

The inductor current ripple flowing into the output capacitor determines the output voltage ripple (please refer to *Section 7.6.3*). Usually the inductor value is selected in order to keep the current ripple lower than 20% - 40% of the output current over the input voltage range. The inductance value can be calculated by *Equation 40*:

Equation 40

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \bullet T_{ON} = \frac{V_{OUT}}{L} \bullet T_{OFF}$$

Where T_{ON} and T_{OFF} are the on and off time of the internal power switch. The maximum current ripple, at fixed $V_{OUT,}$ is obtained at maximum T_{OFF} that is at minimum duty cycle (see *Section 7.6.1: Input capacitor selection* to calculate minimum duty). So fixing ΔI_L = 20% to 40% of the maximum output current, the minimum inductance value can be calculated:

Equation 41

$$L_{MIN} = \frac{V_{OUT}}{\Delta I_{LMAX}} \bullet \frac{1 - D_{MIN}}{F_{SW}}$$

where f_{SW} is the switching frequency $1/(T_{ON} + T_{OFF})$.

For example for V_{OUT} = 3.3 V, V_{IN} = 12 V, I_O = 2 A and F_{SW} = 500 kHz the minimum inductance value to have ΔI_L = 30% of IO is about 8.2 µH.

The peak current through the inductor is given by:

Equation 42

$$I_{L,PK} = I_{OUT} + \frac{\Delta I_L}{2}$$

So if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher is the inductor value, the higher is the average output current that can be delivered, without reaching the current limit.

In *Table 10* some inductor part numbers are listed.

Table 10. Inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	XAL50xx	2.2 to 22	6.5 to 2.7
	XAL60xx	2.2 to 22	12.5 to 4

7.6.3 Output capacitor selection

The triangular shape current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, that depends on the capacitor value and the equivalent resistive component (ESR). As a consequence the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

The voltage ripple equation can be calculated as:

Equation 43

$$\Delta V_{OUT} = ESR \bullet \Delta I_{LMAX} + \frac{\Delta I_{LMAX}}{8 \bullet C_{OUT} \bullet f_{SW}}$$

Usually the resistive component of the ripple can be neglected if the selected output capacitor is a multi layer ceramic capacitor (MLCC).

The output capacitor is important also for loop stability: it determines the main pole and the zero due to its ESR. (see *Section 6: Closing the loop on page 32* to consider its effect in the system stability).

For example with V_{OUT} = 3.3 V, V_{IN} = 12 V, ΔI_L = 0.6 A, f_{SW} = 500 kHz (resulting by the inductor value) and C_{OUT} = 10 µF MLCC:

Equation 44

$$\frac{\Delta V_{OUT}}{V_{OUT}} \cong \frac{1}{V_{OUT}} \bullet \frac{\Delta I_{LMAX}}{C_{OUT} \bullet f_{SW}} = \left(\frac{1}{33} \bullet \frac{0,6}{8 \bullet 10\mu F \bullet 500kHz}\right) = \frac{15mV}{3.3} = 0.45\%$$

The output capacitor value has a key role to sustain the output voltage during a steep load transient. When the load transient slew rate exceeds the system bandwidth, the output capacitor provides the current to the load. In case the final application specifies high slew rate load transient, the system bandwidth must be maximized and the output capacitor has to sustain the output voltage for time response shorter than the loop response time.

In *Table 11* some capacitor series are listed.

Table 11. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
MURATA	GRM32	22 to 100	6.3 to 25	< 5
	GRM31	10 to 47	6.3 to 25	< 5
PANASONIC	ECJ	10 to 22	6.3	< 5
	EEFCD	10 to 68	6.3	15 to 55
SANYO	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	< 5

8 Efficiency curves

Figure 31. Efficiency curves over f_{sw}: V_{IN} = 13.5 V - V_{OUT} = 3.3 V

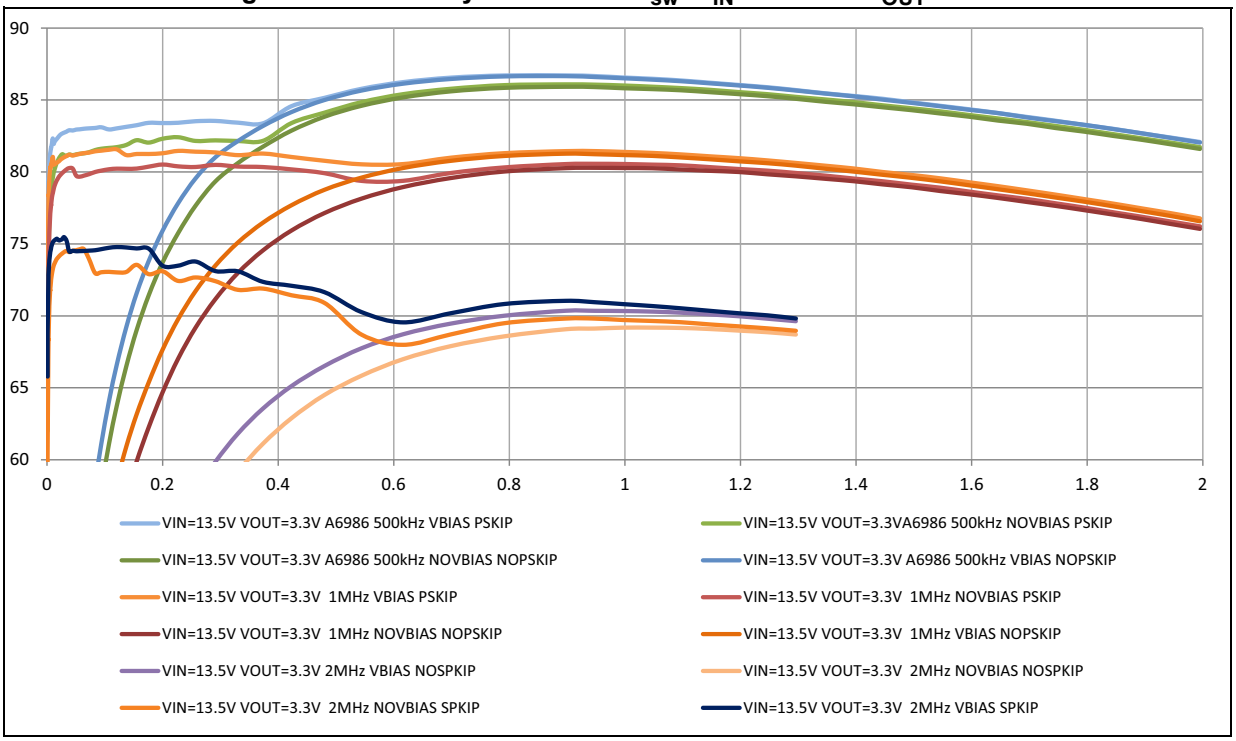


Figure 32. Efficiency curves over f_{sw}: V_{IN} = 13.5 V - V_{OUT} = 3.3 V (log scale)

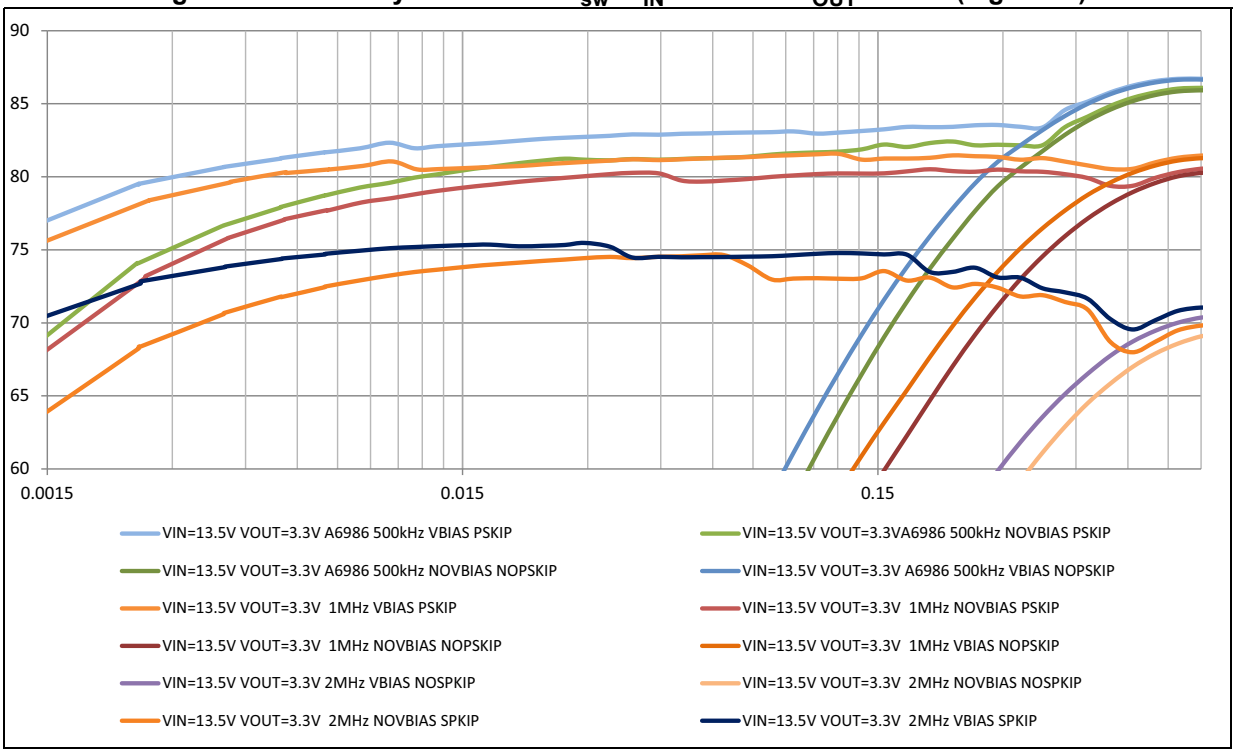


Figure 33. Efficiency curves over f_{sw}: V_{IN} = 13.5 V - V_{OUT} = 5 V

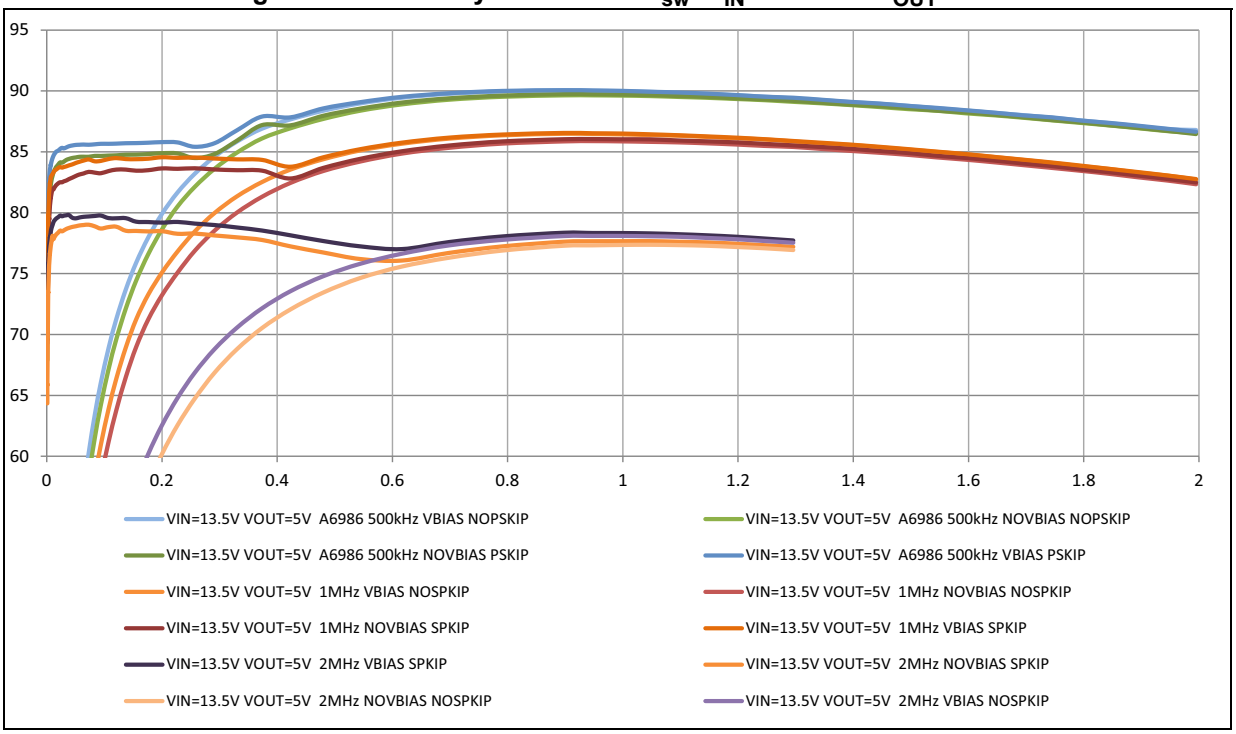


Figure 34. Efficiency curves over f_{sw}: V_{IN} = 13.5 V - V_{OUT} = 5 V (log scale)

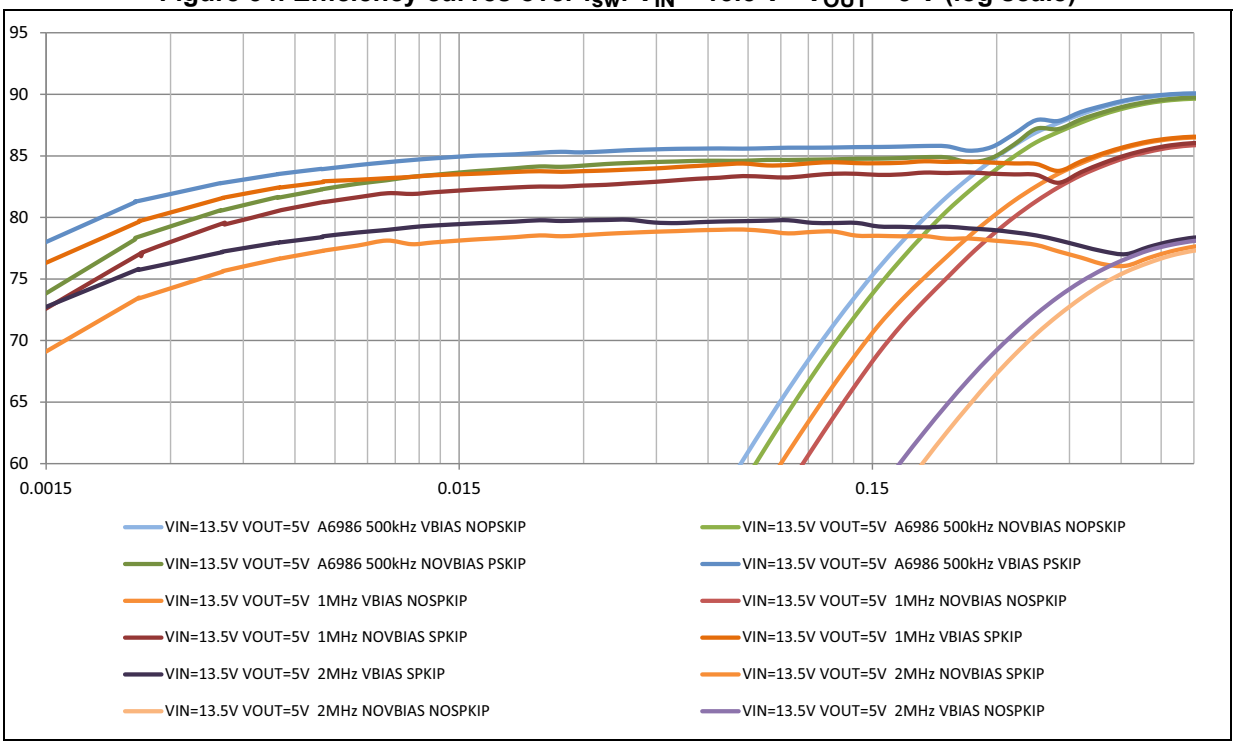


Figure 35. Efficiency curves over f_{sw}: V_{IN} = 24 V - V_{OUT} = 3.3 V

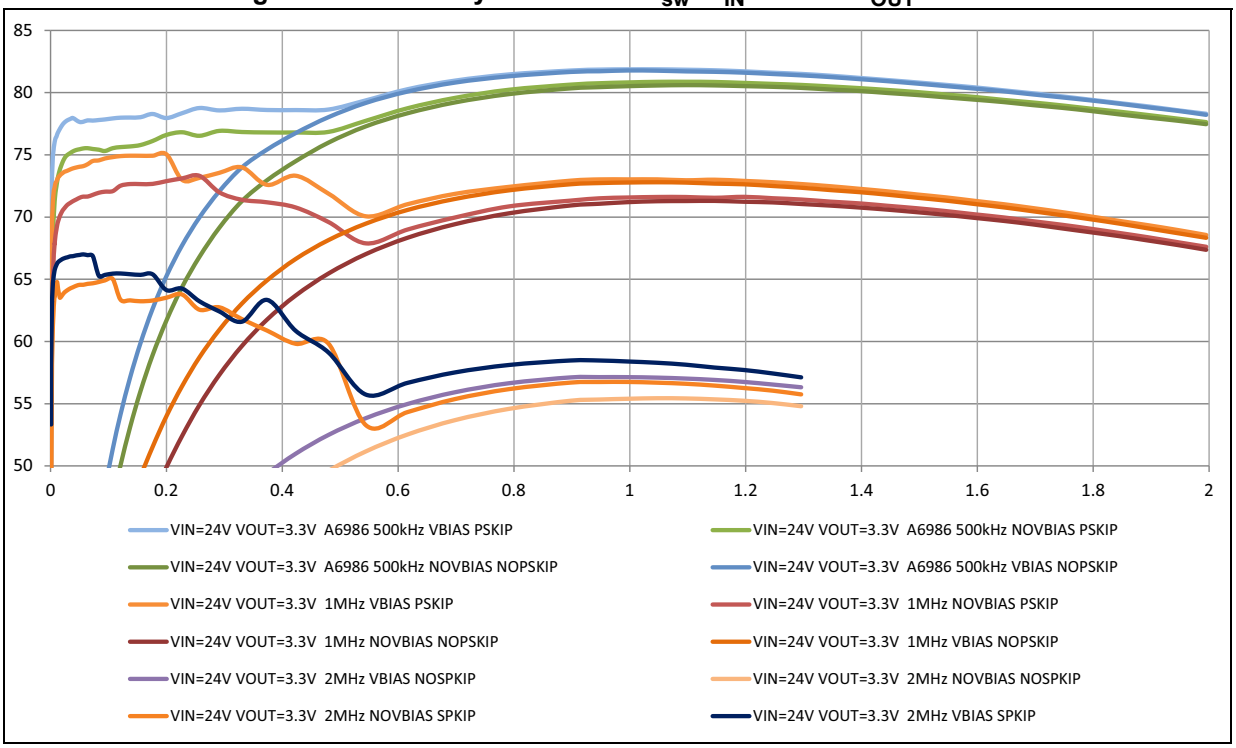


Figure 36. Efficiency curves over f_{sw}: V_{IN} = 24 V - V_{OUT} = 3.3 V (log scale)

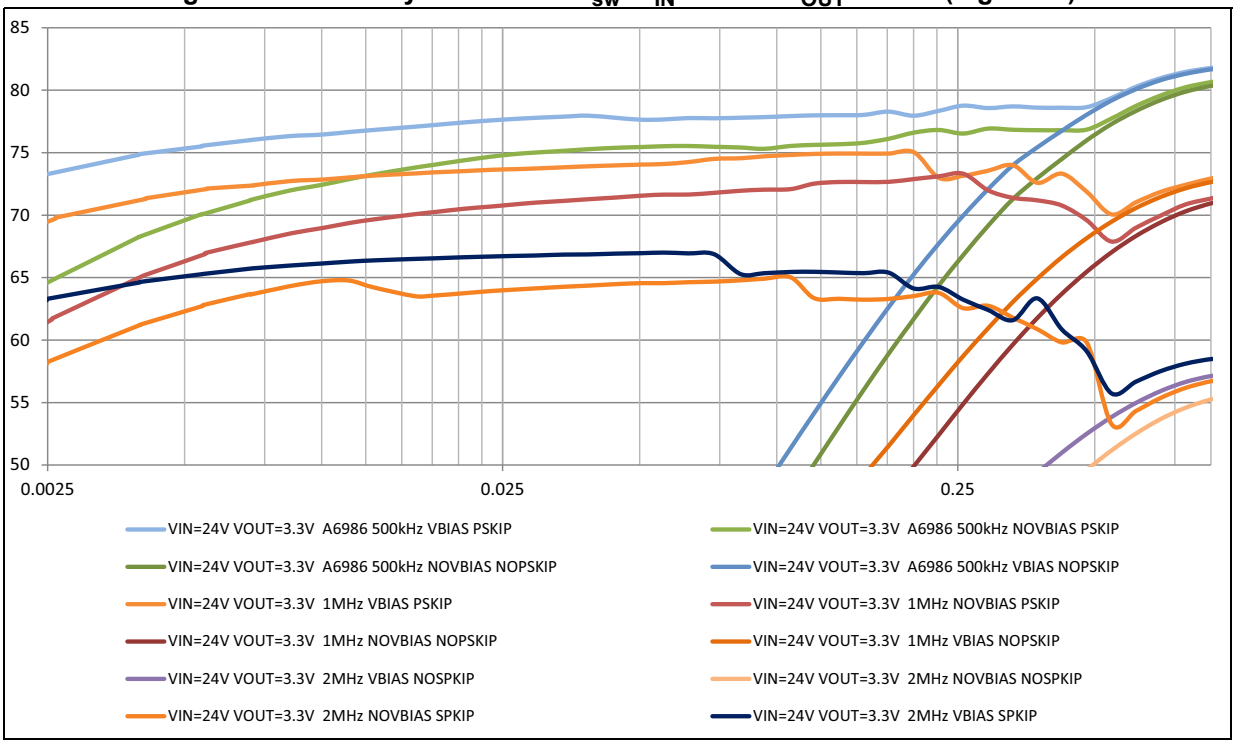


Figure 37. Efficiency curves over f_{sw}: V_{IN} = 24 V - V_{OUT} = 5 V

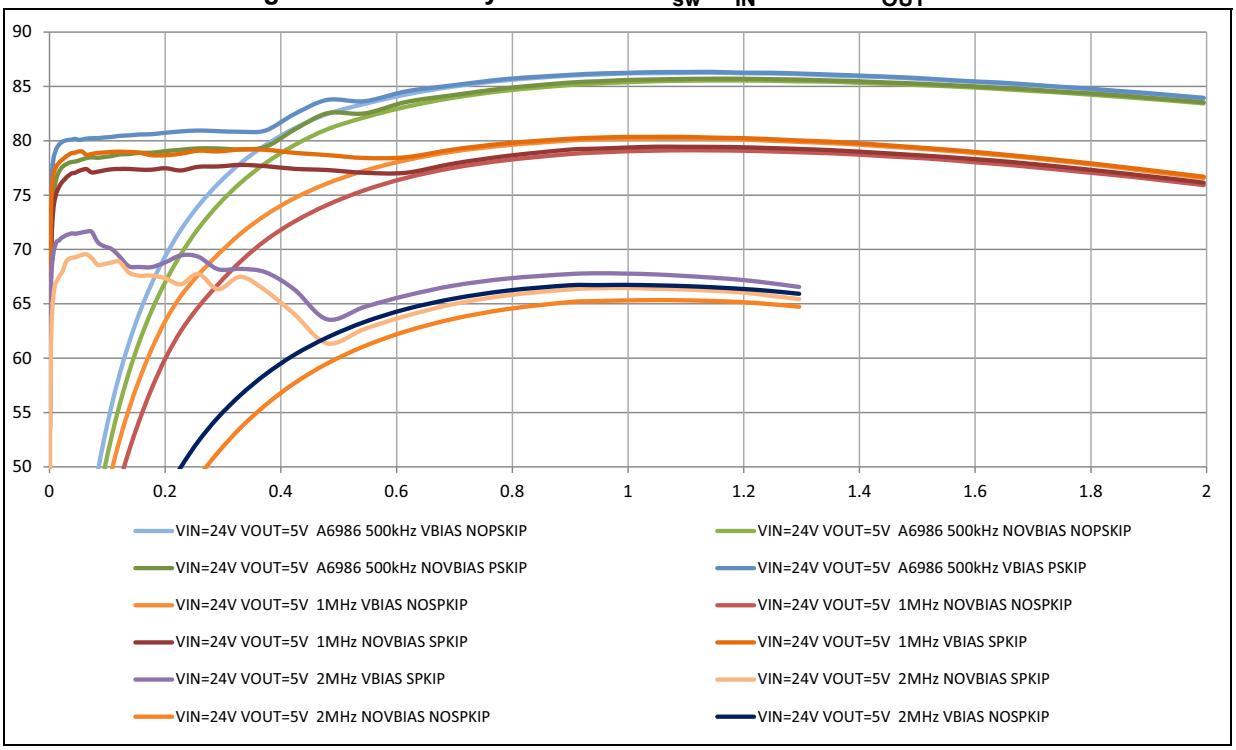


Figure 38. Efficiency curves over f_{sw}: V_{IN} = 24 V - V_{OUT} = 5 V (log scale)

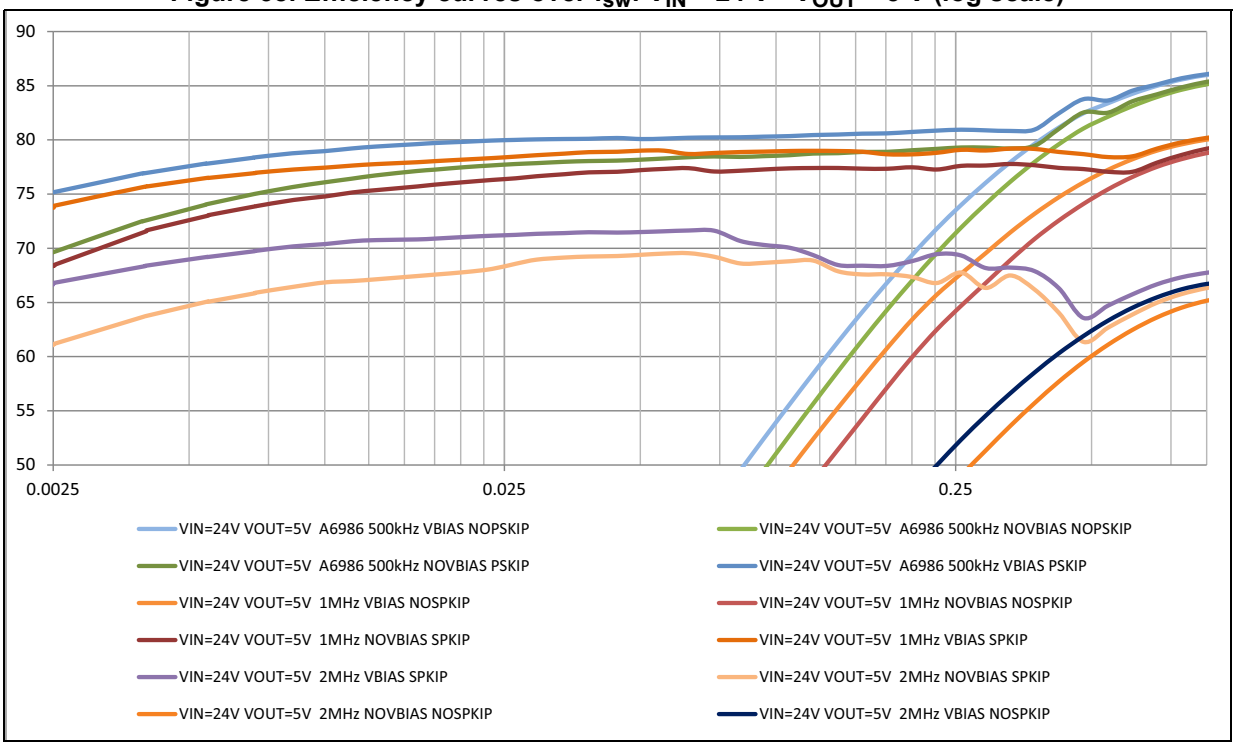


Figure 39. Efficiency curves: f_{sw} = 500kHz - V_{IN} = 24 V - V_{OUT} = 3.3 V

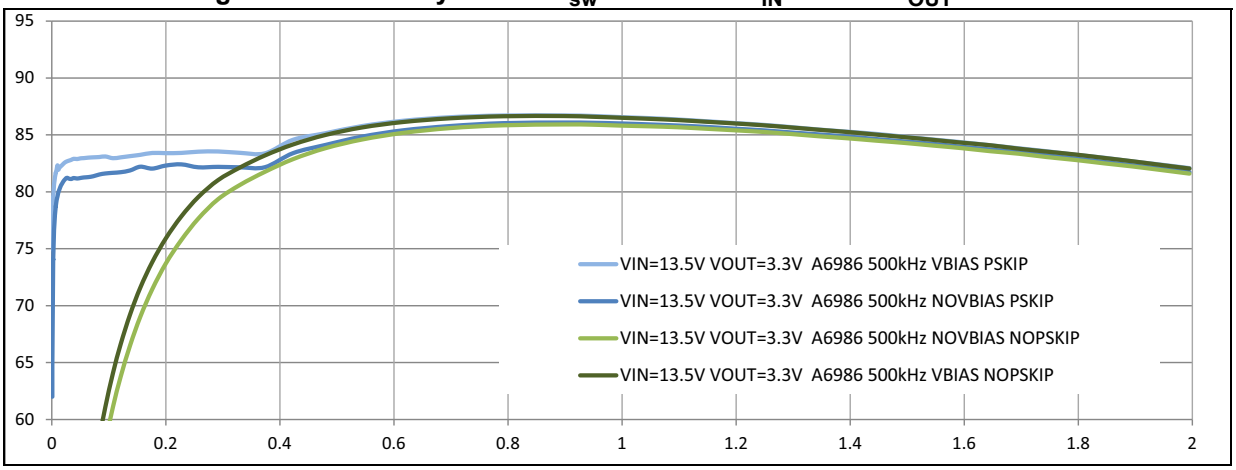


Figure 40. Efficiency curves: f_{sw} = 500 kHz - V_{IN} = 13.5 V - V_{OUT} = 3.3 V (log scale)

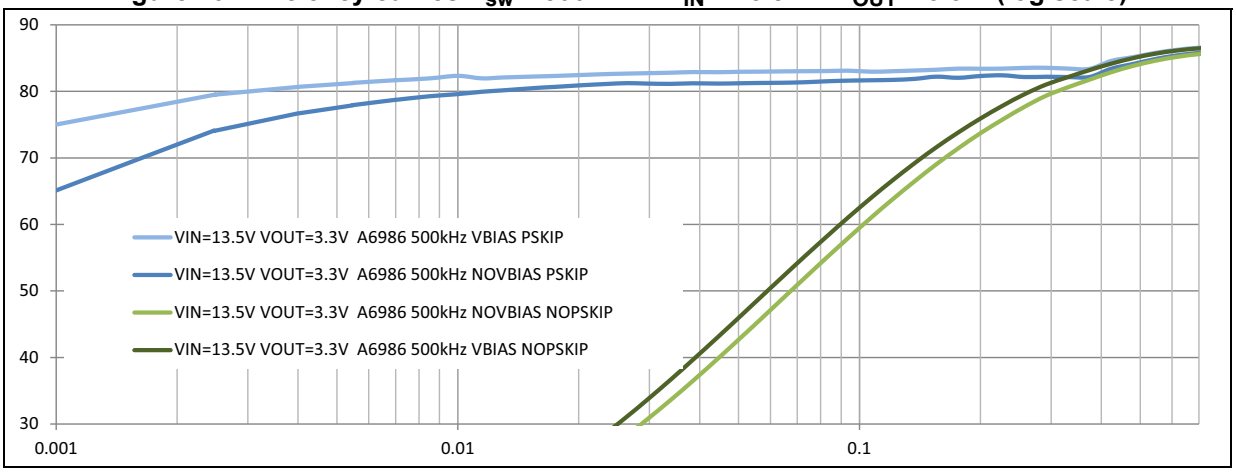


Figure 41. Efficiency curves: f_{sw} = 500 kHz - V_{IN} = 13.5 V - V_{OUT} = 5 V

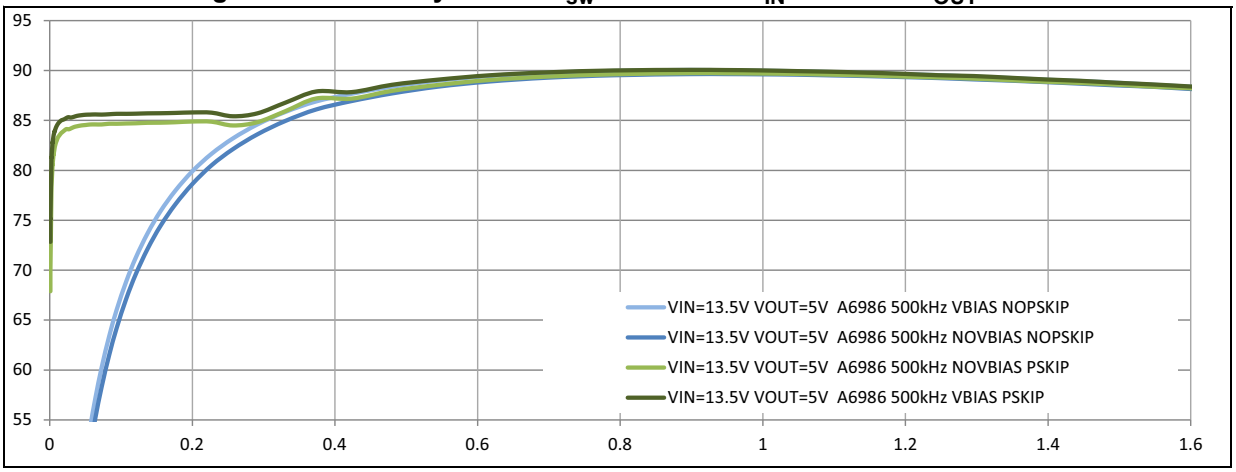


Figure 42. Efficiency curves: f_{sw} = 500 kHz - V_{IN} = 13.5 V - V_{OUT} = 5 V (log scale)

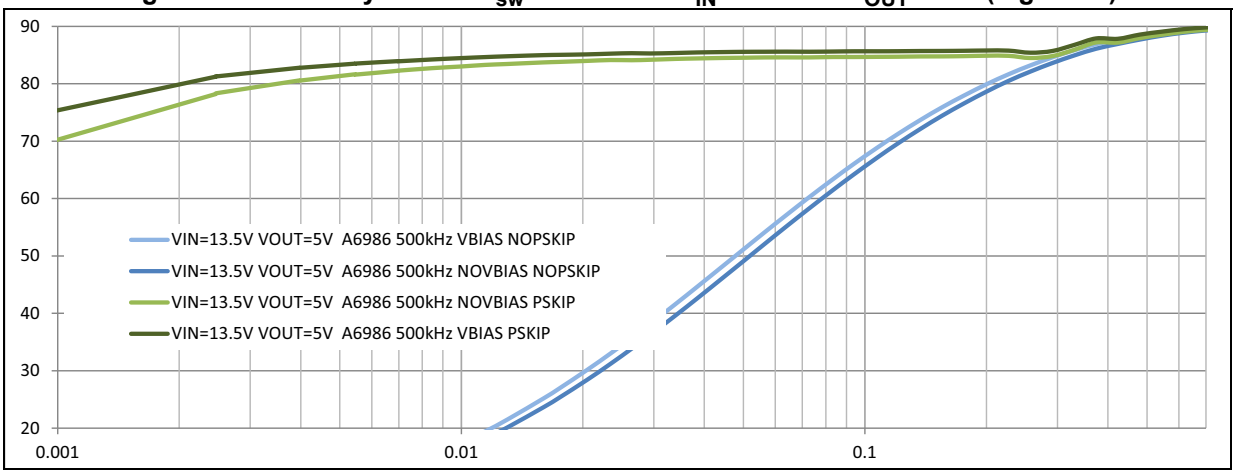


Figure 43. Efficiency curves: f_{sw} = 500 kHz - V_{IN} = 24 V - V_{OUT} = 3.3 V

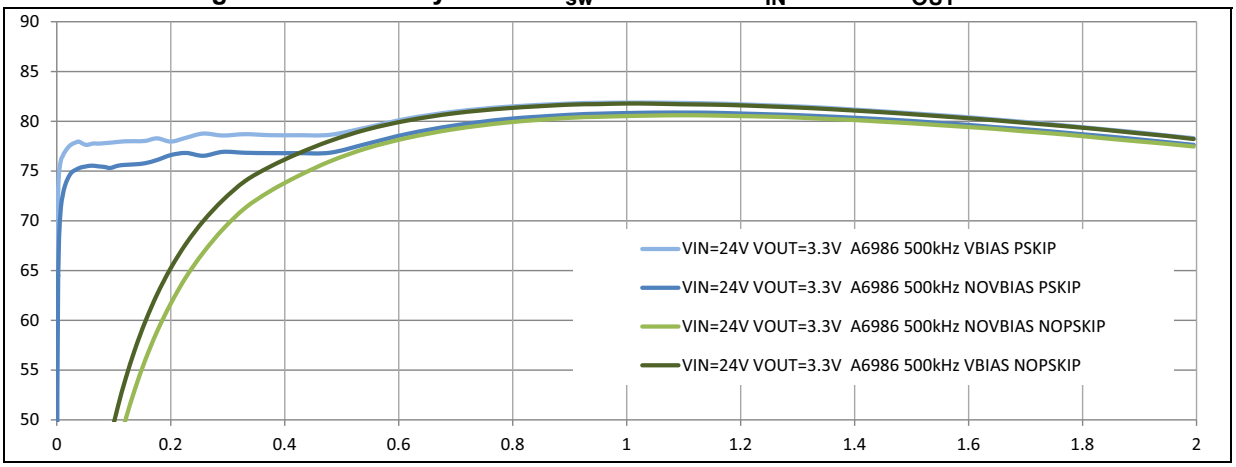


Figure 44. Efficiency curves: f_{sw} = 500 kHz - V_{IN} = 24 V - V_{OUT} = 3.3 V (log scale)

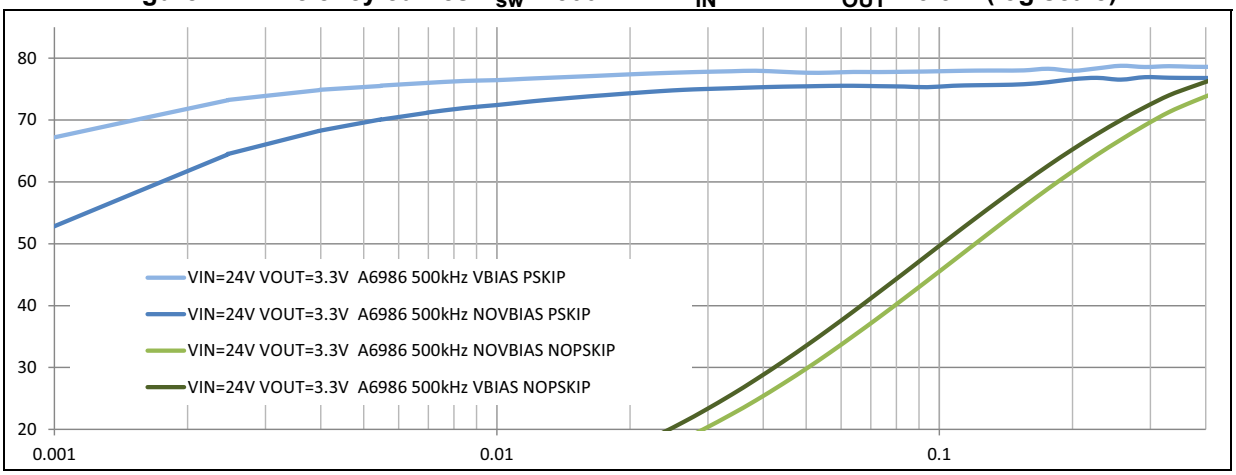


Figure 45. Efficiency curves: f_{sw} = 500 kHz - V_{IN} = 24 V - V_{OUT} = 5 V (log scale)

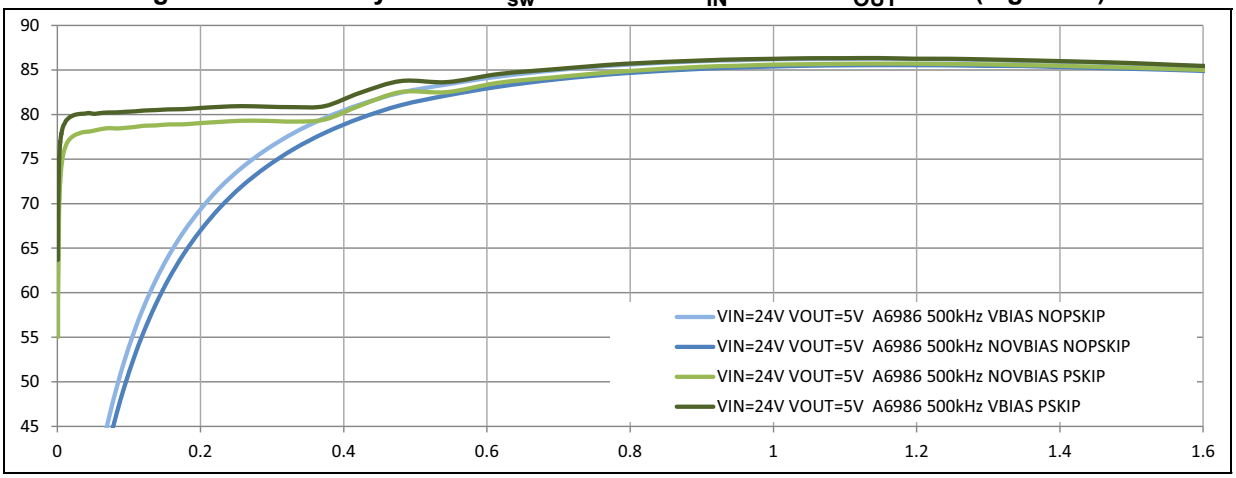
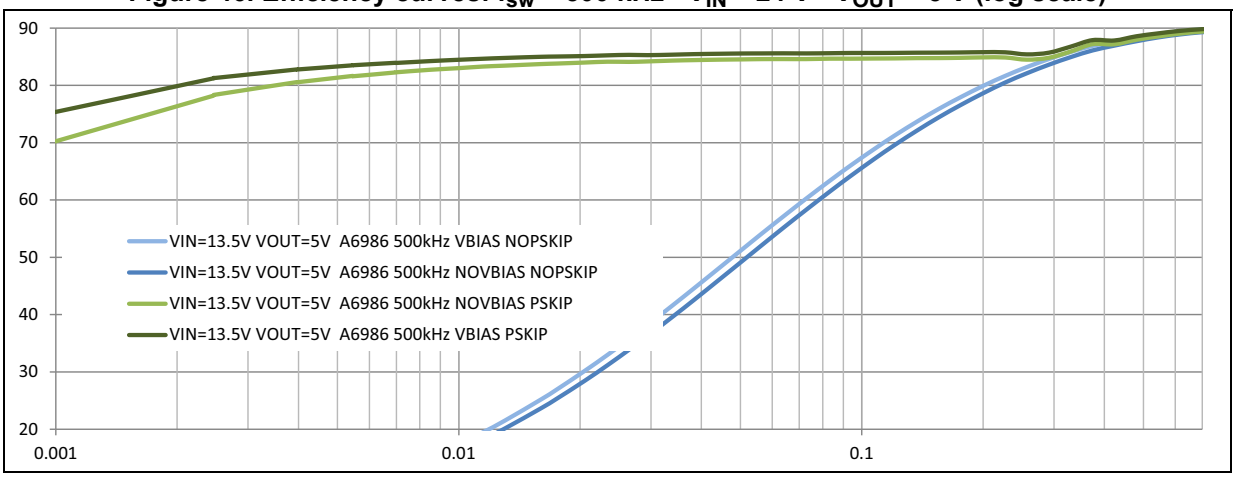


Figure 46. Efficiency curves: f_{sw} = 500 kHz - V_{IN} = 24 V - V_{OUT} = 5 V (log scale)



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 47. HTSSOP16 package outline

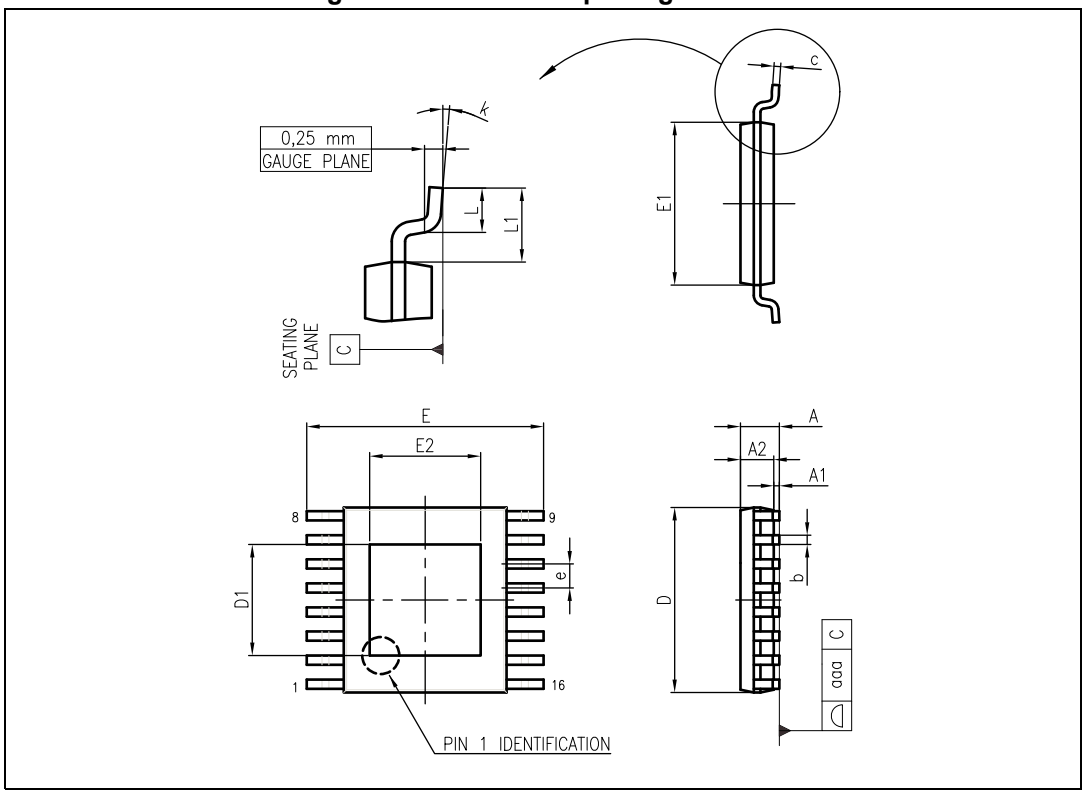


Table 12. HTSSOP16 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
D1	2.8	3	3.2
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.8	3	3.2
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0.00		8.00
aaa			0.10

10 Order codes

Table 13. Order codes

Part numbers	Package	Packaging
R6986	HTSSOP16	Tube
R6986TR		Tape and reel

11 Revision history

Table 14. Document revision history

Date	Revision	Changes
06-Oct-2014	1	Initial release.