RENESAS

HAT2175H

Silicon N Channel Power MOS FET Power Switching

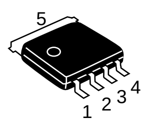
REJ03G0006-0300Z
Rev.3.00
Apr.14.2003

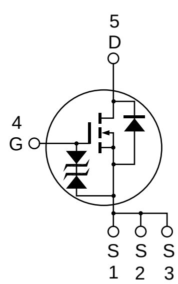
Features

- Capable of 8 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 33 mΩ typ. (at V_{GS} = 10 V)

Outline

LFPAK





1, 2, 3	Source
4	Gate
5	Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$ Note1	60	A
Body-drain diode reverse drain current	I_{DR}	15	A
Avalanche current	I_{AP} Note 2	15	A
Avalanche energy	E_{AR} Note 2	22.5	mJ
Channel dissipation	Pch Note3	15	W
Channel to Case Thermal Resistance	θch-C	8.34	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. Tc = 25°C

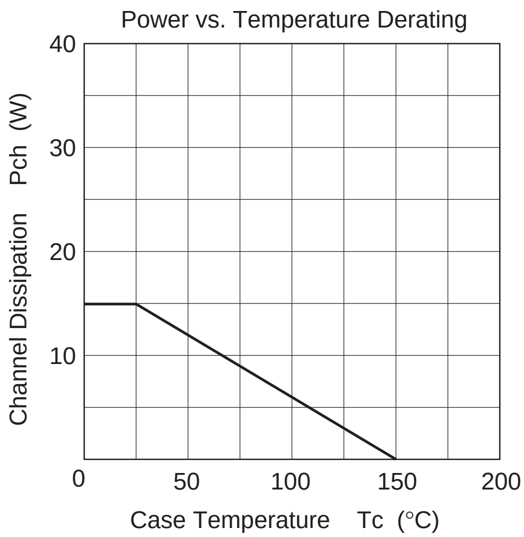
Electrical Characteristics

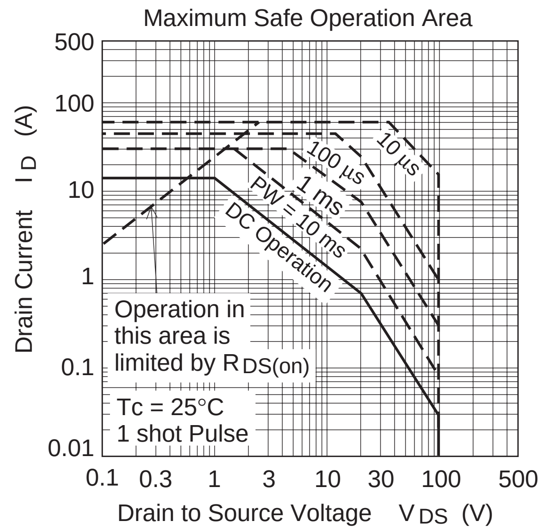
(Ta = 25°C)

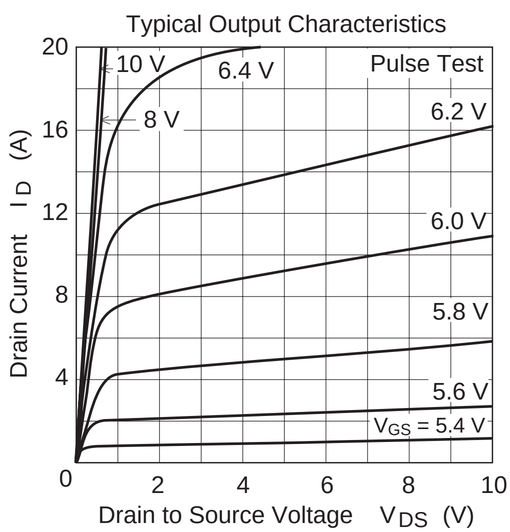
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	± 10	μA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	1	μA	V_{DS} = 100 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	4.0	—	6.0	V	V_{DS} = 10 V, I_D = 20mA
Static drain to source on state resistance	$R_{DS(on)}$	—	33	42	mΩ	I_D = 7.5 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	34	46	mΩ	I_D = 7.5 A, V_{GS} = 8 V Note4
Forward transfer admittance	$\|y_{fs}\|$	15	25	—	S	I_D = 7.5 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	1445	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	185	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	61	—	pF	f = 1 MHz
Gate Resistance	Rg	—	0.55	—	Ω	
Total gate charge	Qg	—	21	—	nc	V_{DD} = 50 V
Gate to source charge	Qgs	—	8	—	nc	V_{GS} = 10 V
Gate to drain charge	Qgd	—	4.5	—	nc	I_D = 15 A
Turn-on delay time	$t_{d(on)}$	—	17	—	ns	V_{GS} = 10 V, I_D = 7.5 A
Rise time	t_r	—	8.2	—	ns	$V_{DD} \cong$ 30 V
Turn-off delay time	$t_{d(off)}$	—	28	—	ns	R_L = 4 Ω
Fall time	t_f	—	4.7	—	ns	Rg = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	0.84	1.10	V	IF = 15 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	45	—	ns	IF = 15 A, V_{GS} = 0 diF/ dt = 100 A/ μs

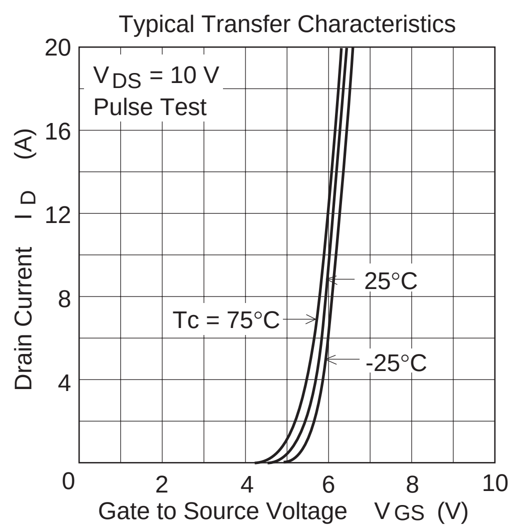
Notes: 4. Pulse test

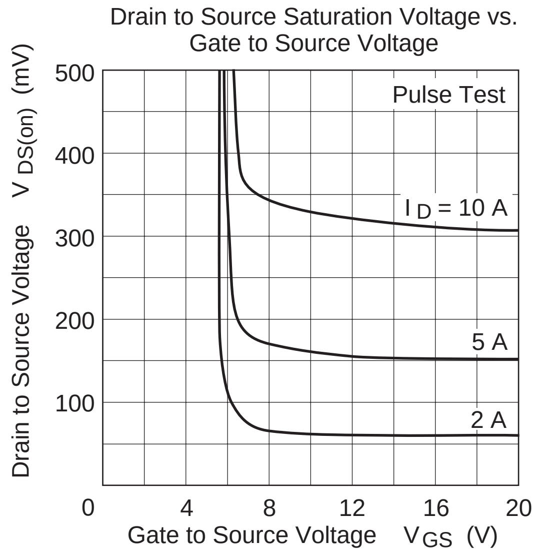
Main Characteristics

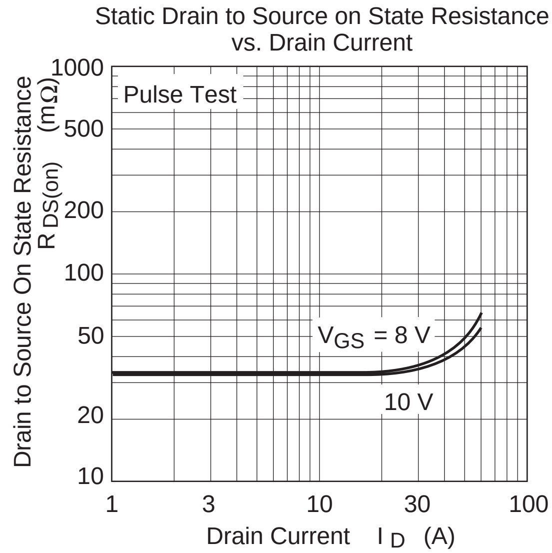


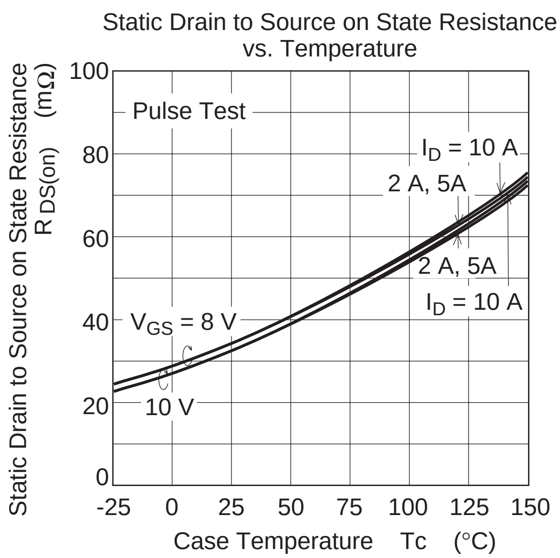


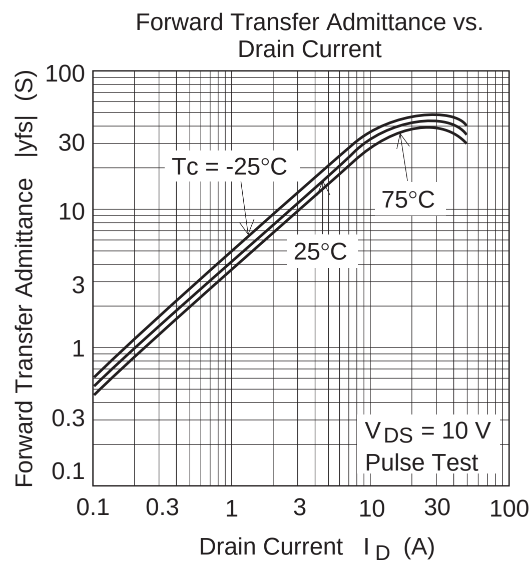




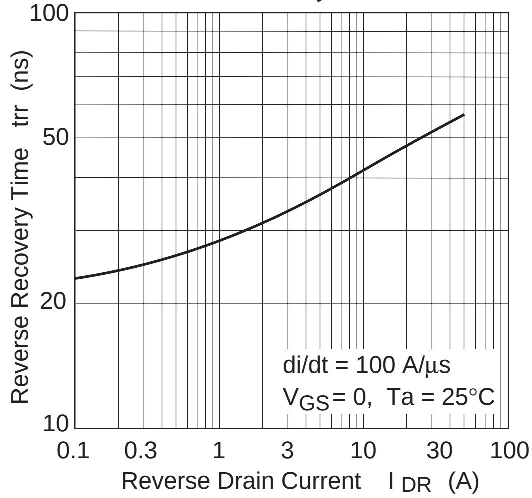

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 10 A
5 A
2 A
Drain to Source Voltage V DS(on) (mV)
Gate to Source Voltage V GS (V)
0 4 8 12 16 20
100 200 300 400 500


Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = 8 V
10 V
Drain to Source On State Resistance R DS(on) (mΩ)
Drain Current I D (A)
1 3 10 30 100
10 20 50 100 200 500 1000

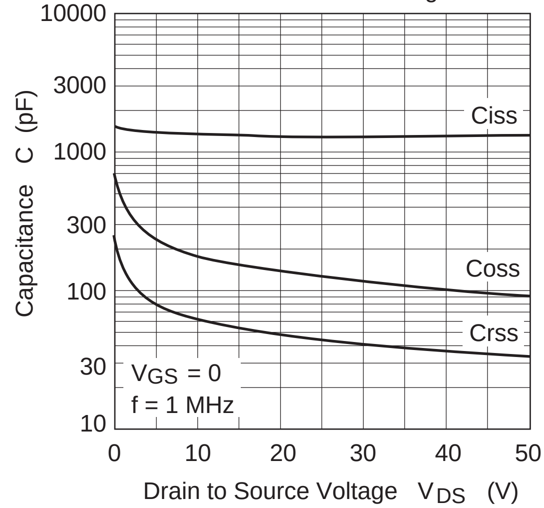

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = 10 A
2 A, 5A
2 A, 5A
I D = 10 A
V GS = 8 V
10 V
Static Drain to Source on State Resistance R DS(on) (mΩ)
Case Temperature Tc (°C)
-25 0 25 50 75 100 125 150
0 20 40 60 80 100


Forward Transfer Admittance vs.
Drain Current
Tc = -25°C
25°C
75°C
V DS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
Drain Current I D (A)
0.1 0.3 1 3 10 30 100
0.1 0.3 1 3 10 30 100

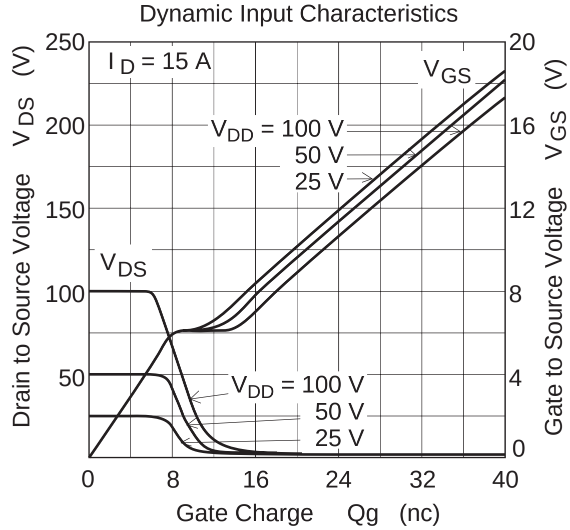
Body-Drain Diode Reverse Recovery Time



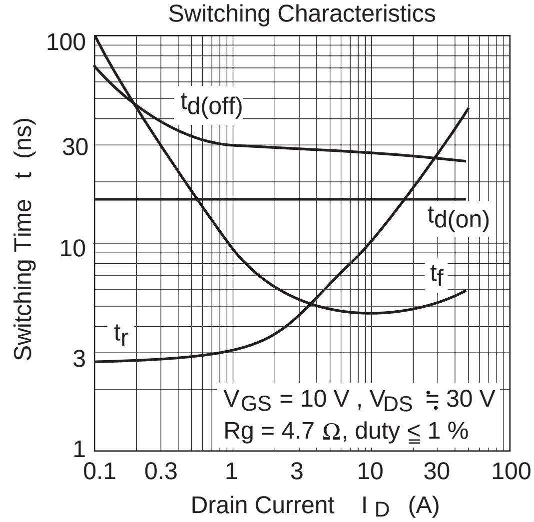
Typical Capacitance vs. Drain to Source Voltage

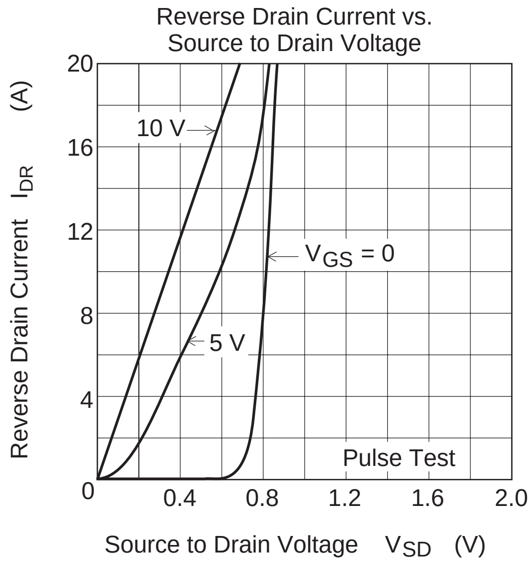


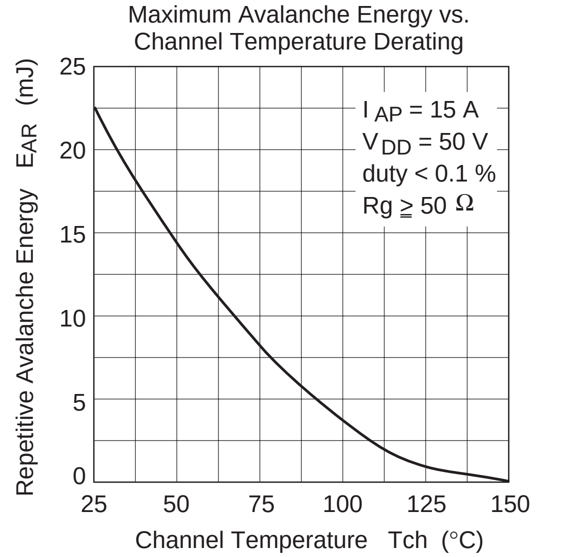
Dynamic Input Characteristics

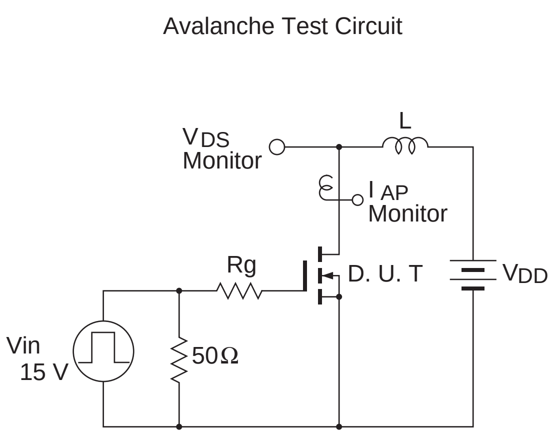


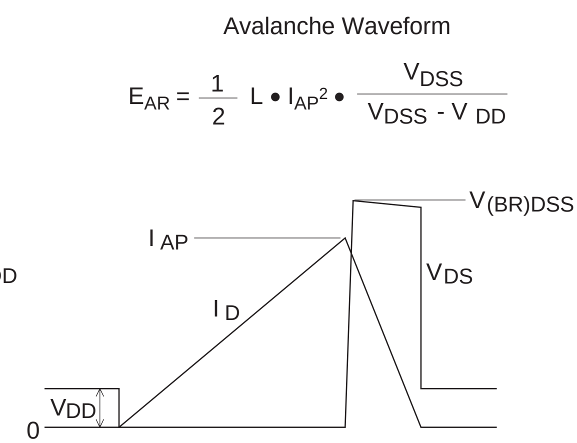
Switching Characteristics




Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
4
8
12
16
20
0.4
0.8
1.2
1.6
2.0
10 V
5 V
V_{GS} = 0
Pulse Test


Maximum Avalanche Energy vs.
Channel Temperature Derating
Repetitive Avalanche Energy E_{AR} (mJ)
Channel Temperature Tch (°C)
0
5
10
15
20
25
25
50
75
100
125
150
I_{AP} = 15 A
V_{DD} = 50 V
duty < 0.1 %
Rg ≧ 50 Ω


Avalanche Test Circuit
V_{DS} Monitor
L
I_{AP} Monitor
Rg
D. U. T
V_{DD}
Vin 15 V
50Ω


Avalanche Waveform
$E_{AR} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$
$V_{(BR)DSS}$
I_{AP}
V_{DS}
I_D
V_{DD}
0

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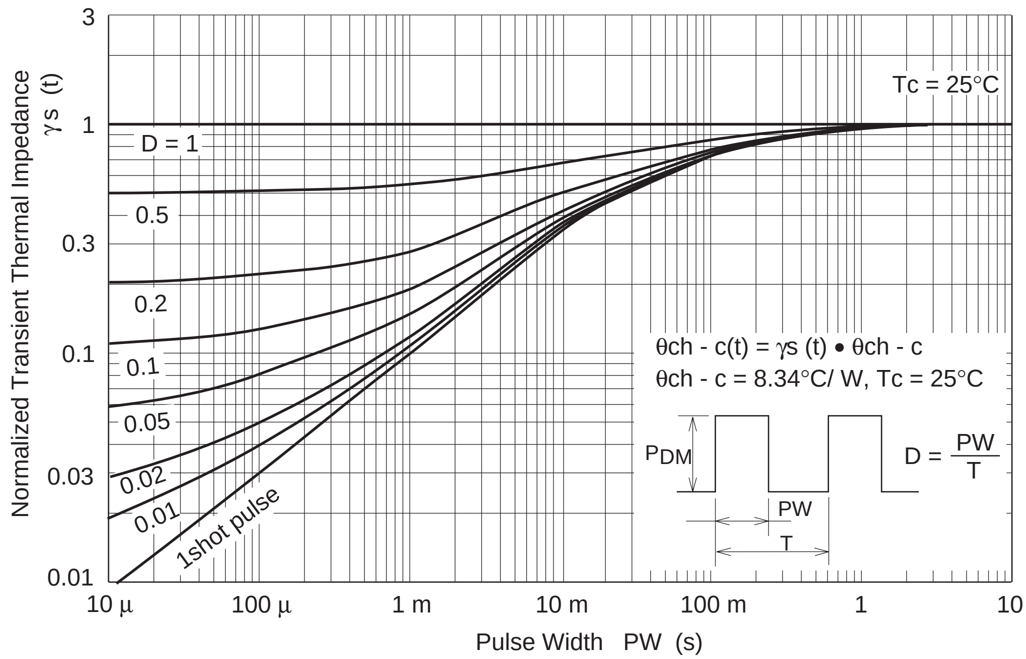
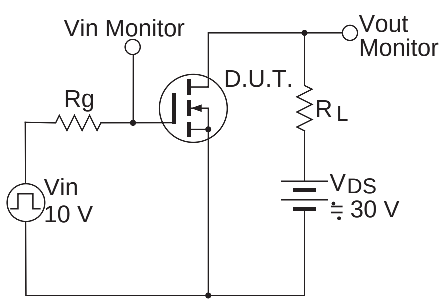
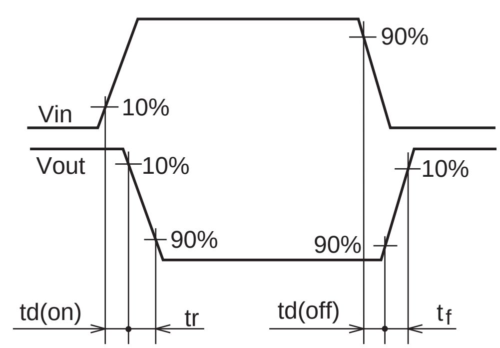
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

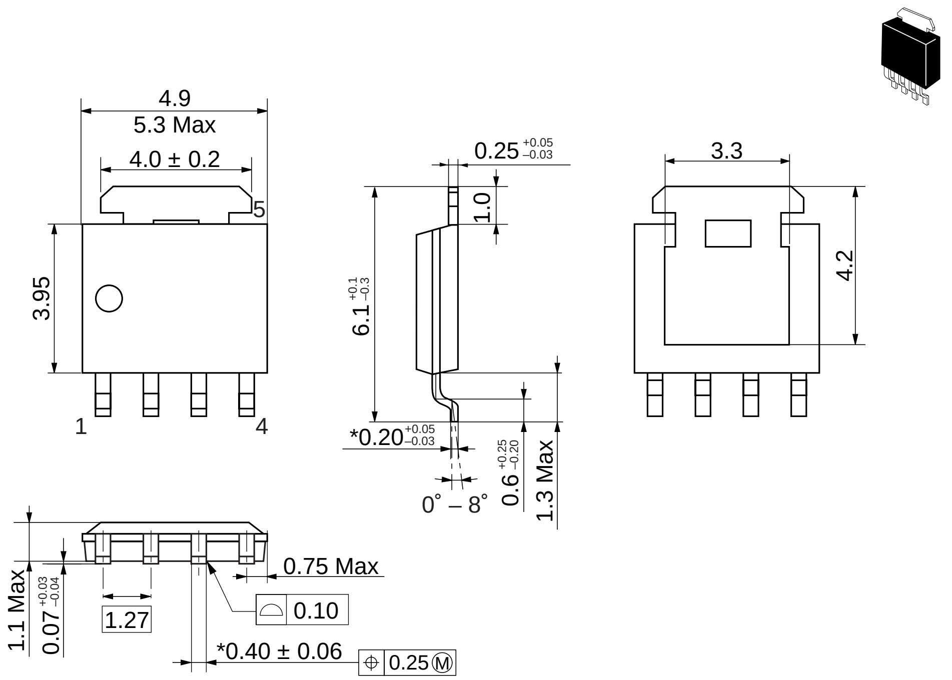


Switching Time Waveform



Package Dimensions

As of January, 2003
Unit: mm



Package Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

*Ni/Pd/Au plating