

HAT2175H

Silicon N Channel Power MOS FET Power Switching

REJ03G0006-0300Z

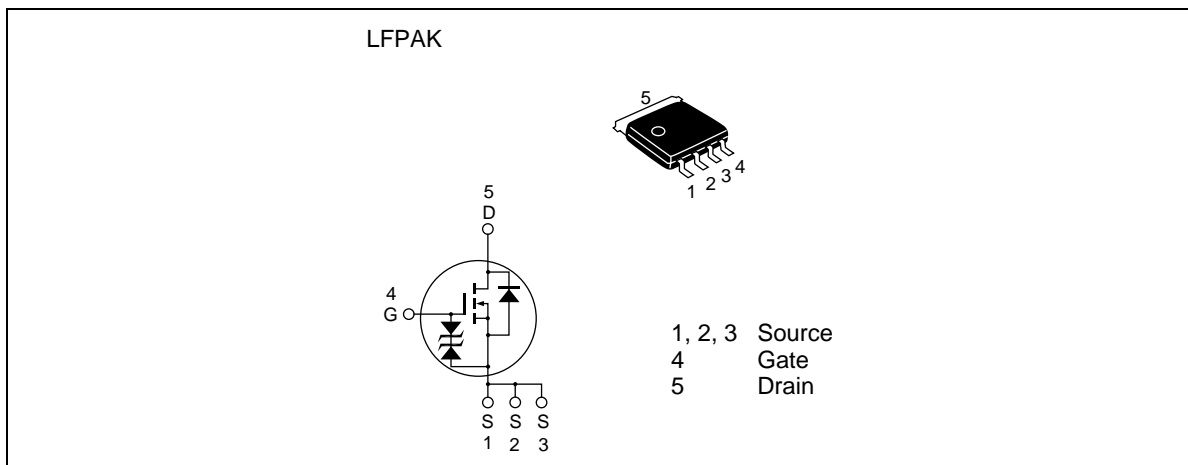
Rev.3.00

Apr.14.2003

Features

- Capable of 8 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 33 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	100	V
Gate to source voltage	V _{GSS}	± 20	V
Drain current	I _D	15	A
Drain peak current	I _{D(pulse)} ^{Note1}	60	A
Body-drain diode reverse drain current	I _{DR}	15	A
Avalanche current	I _{AP} ^{Note 2}	15	A
Avalanche energy	E _{AR} ^{Note 2}	22.5	mJ
Channel dissipation	P _{ch} ^{Note3}	15	W
Channel to Case Thermal Resistance	θ _{ch-C}	8.34	°C/W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at T_{ch} = 25°C, R_g ≥ 50 Ω
3. T_c = 25°C

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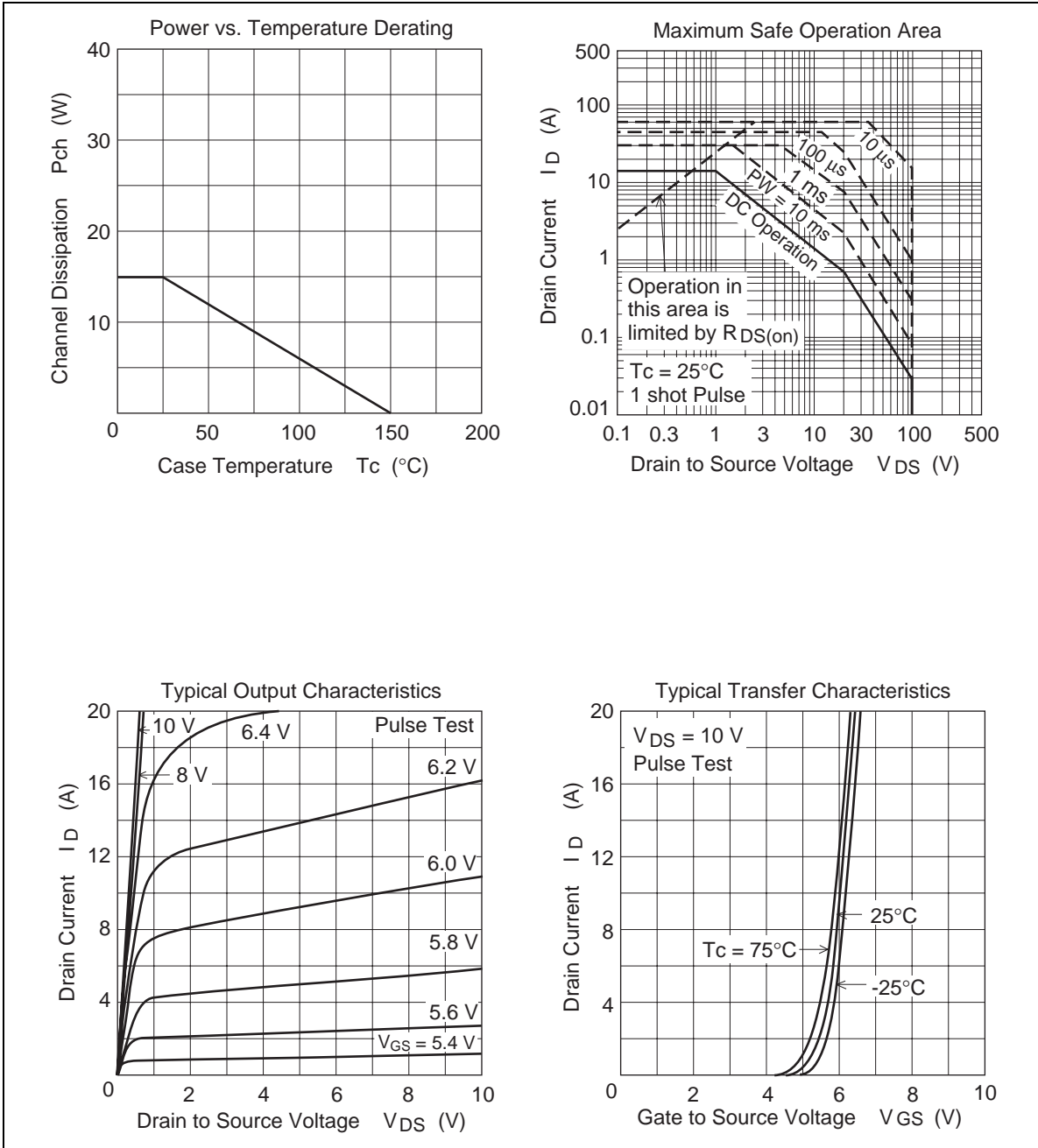
Electrical Characteristics

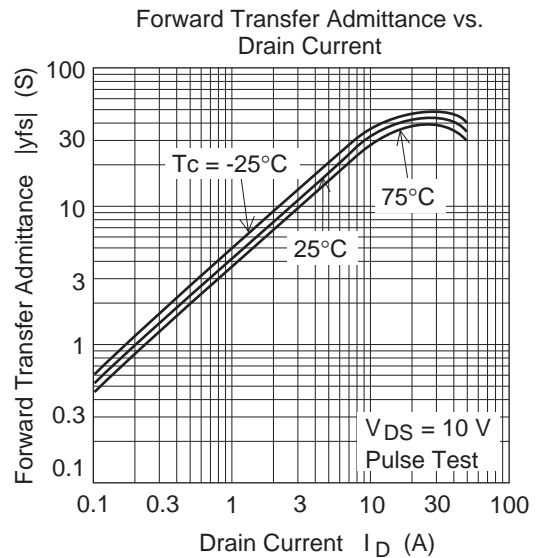
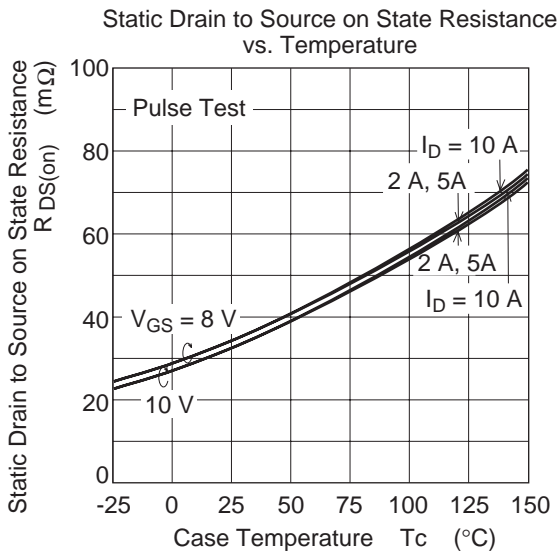
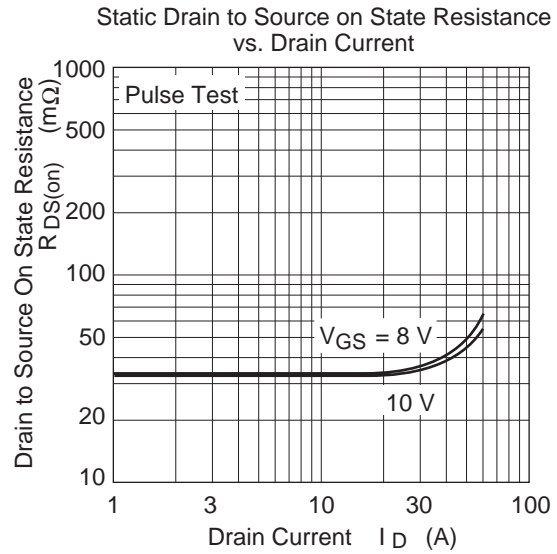
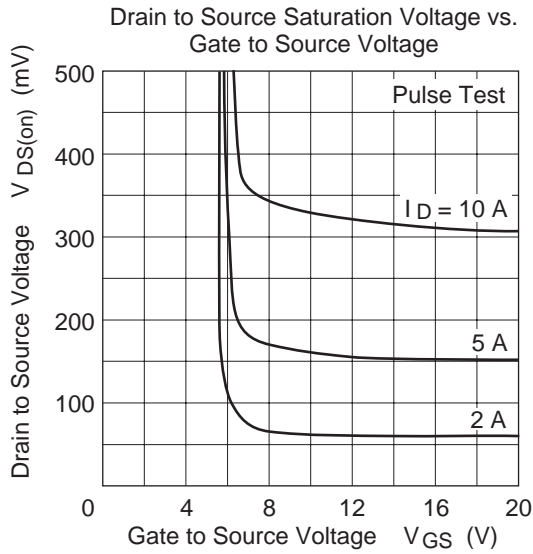
(T_a = 25°C)

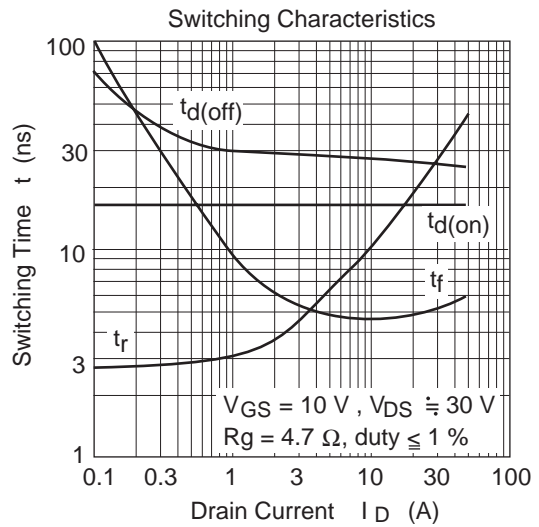
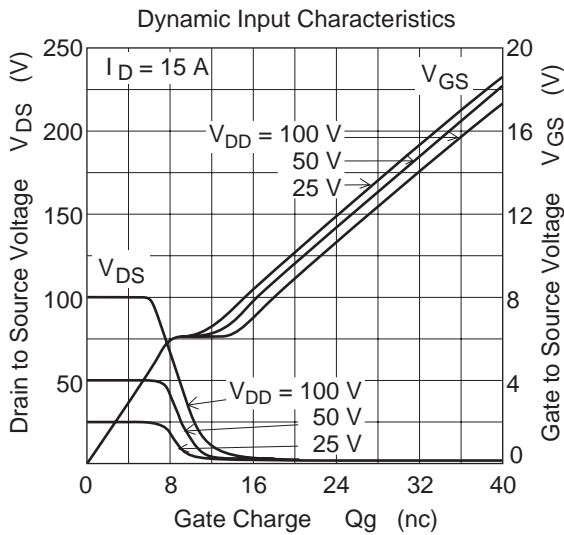
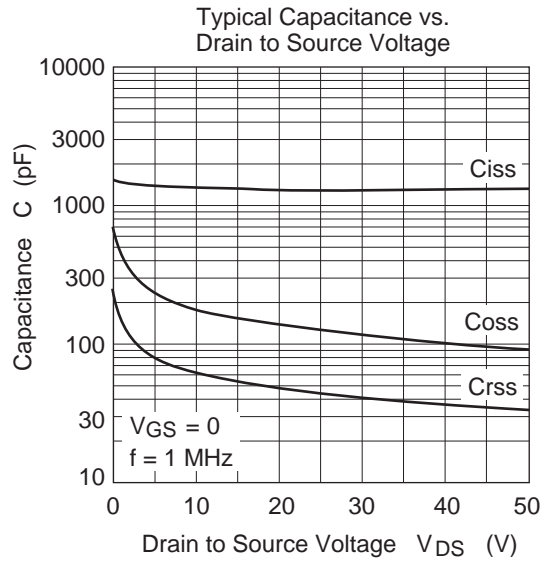
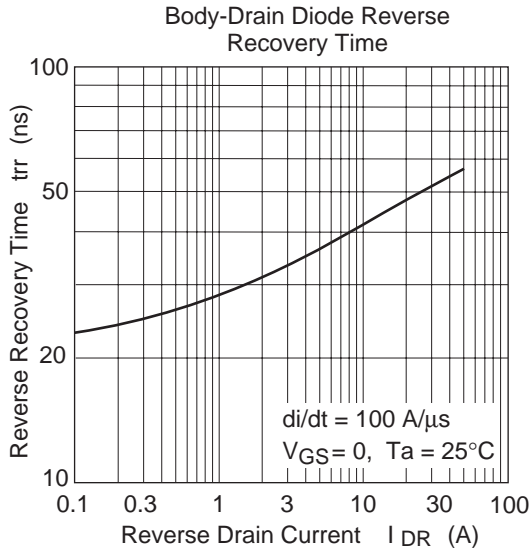
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	100	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	± 20	—	—	V	I _G = ±100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS}	—	—	± 10	μA	V _{GS} = ±16 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	1	μA	V _{DS} = 100 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	4.0	—	6.0	V	V _{DS} = 10 V, I _D = 20mA
Static drain to source on state resistance	R _{DS(on)}	—	33	42	mΩ	I _D = 7.5 A, V _{GS} = 10 V ^{Note4}
	R _{DS(on)}	—	34	46	mΩ	I _D = 7.5 A, V _{GS} = 8 V ^{Note4}
Forward transfer admittance	y _{fs}	15	25	—	S	I _D = 7.5 A, V _{DS} = 10 V ^{Note4}
Input capacitance	C _{iss}	—	1445	—	pF	V _{DS} = 10 V
Output capacitance	C _{oss}	—	185	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	61	—	pF	f = 1 MHz
Gate Resistance	R _g	—	0.55	—	Ω	
Total gate charge	Q _g	—	21	—	nc	V _{DD} = 50 V
Gate to source charge	Q _{gs}	—	8	—	nc	V _{GS} = 10 V
Gate to drain charge	Q _{gd}	—	4.5	—	nc	I _D = 15 A
Turn-on delay time	t _{d(on)}	—	17	—	ns	V _{GS} = 10 V, I _D = 7.5 A
Rise time	t _r	—	8.2	—	ns	V _{DD} ≅ 30 V
Turn-off delay time	t _{d(off)}	—	28	—	ns	R _L = 4 Ω
Fall time	t _f	—	4.7	—	ns	R _g = 4.7 Ω
Body–drain diode forward voltage	V _{DF}	—	0.84	1.10	V	I _F = 15 A, V _{GS} = 0 ^{Note4}
Body–drain diode reverse recovery time	t _{rr}	—	45	—	ns	I _F = 15 A, V _{GS} = 0 diF/ dt = 100 A/ μs

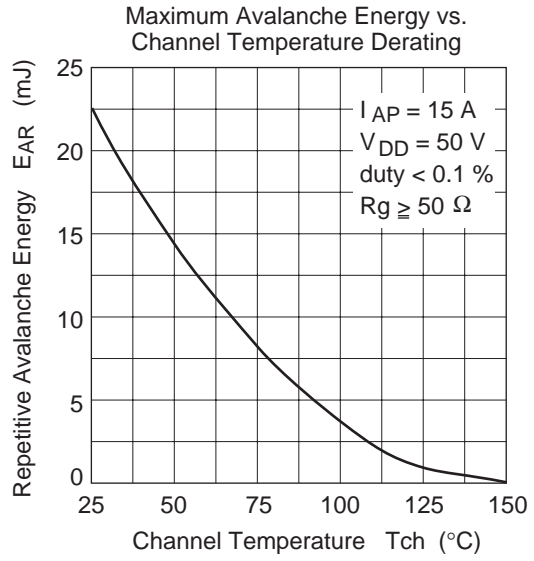
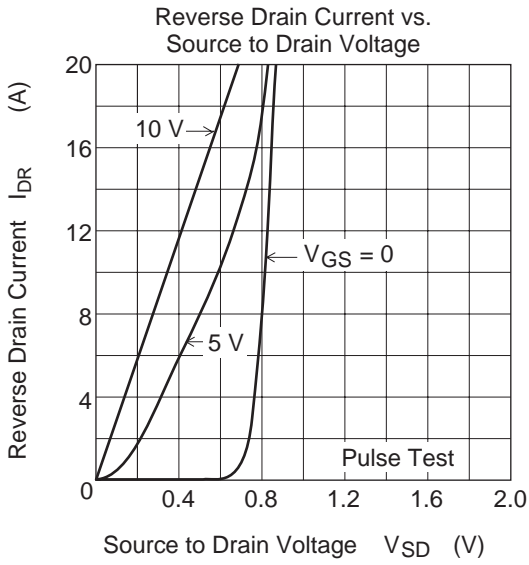
Notes: 4. Pulse test

Main Characteristics

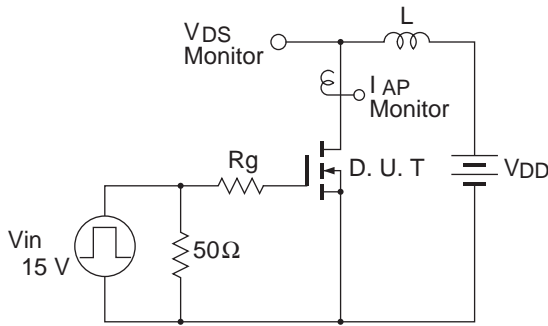






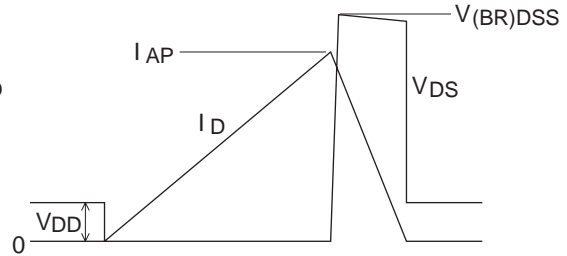


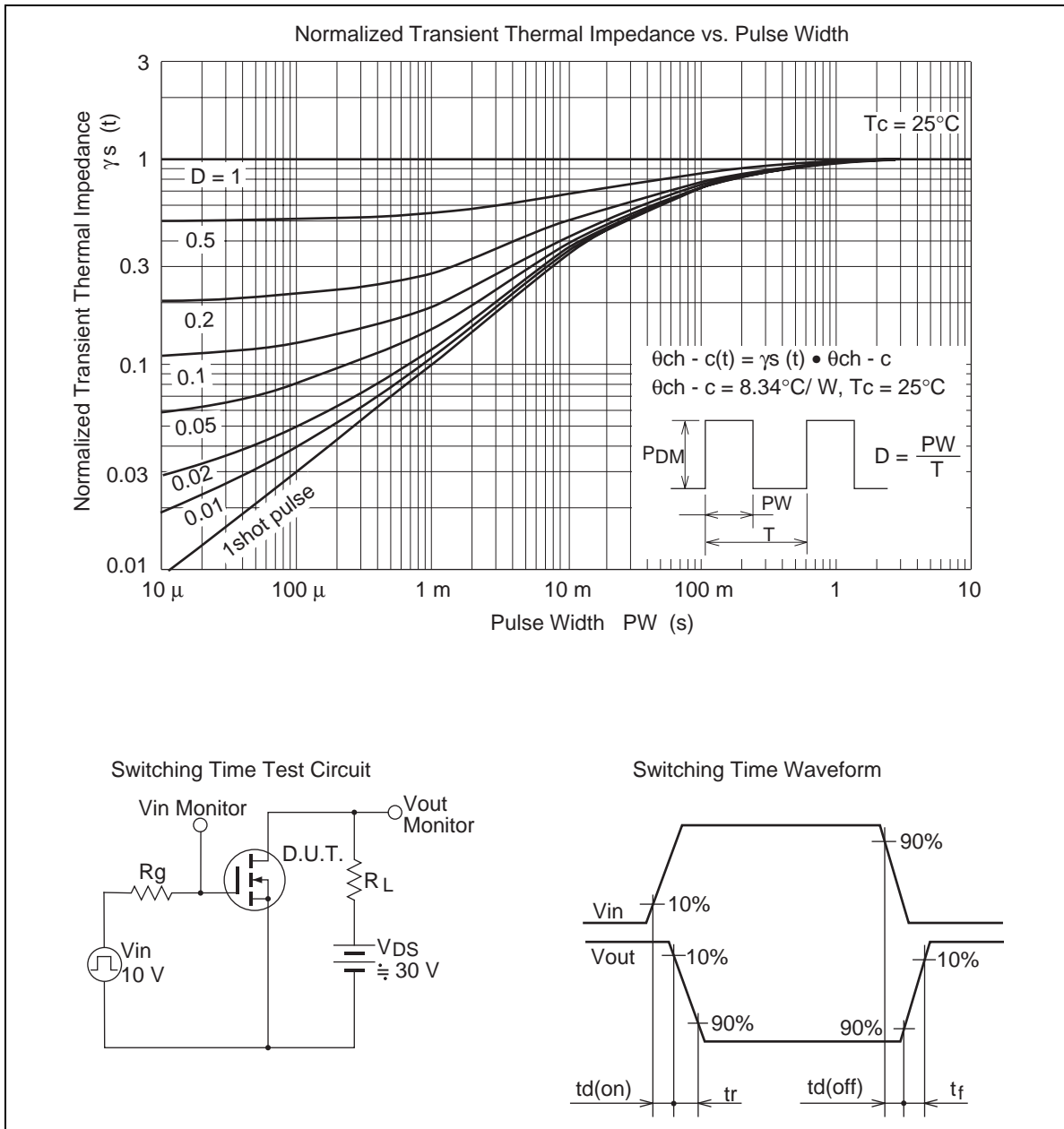
Avalanche Test Circuit



Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

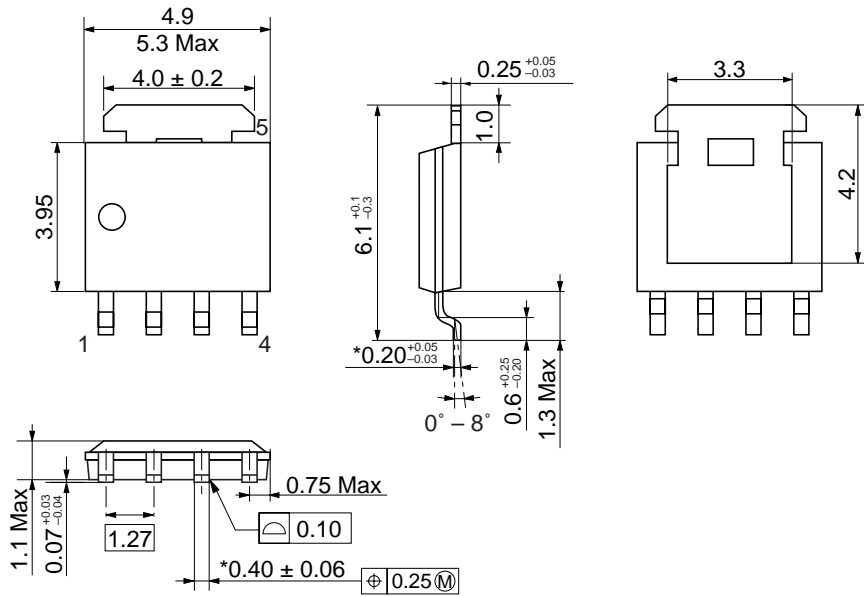
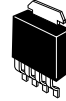




Package Dimensions

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

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Keep safety first in your circuit designs!

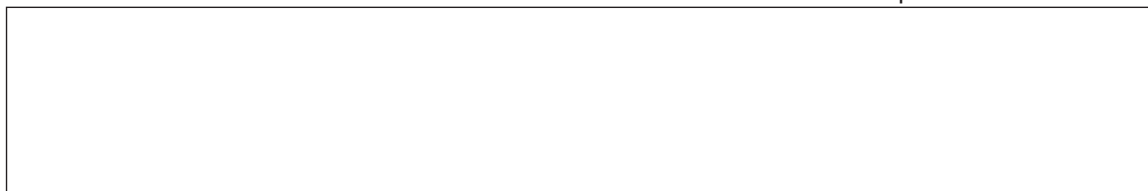
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