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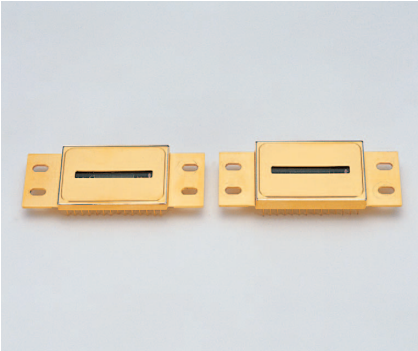
InGaAs linear image sensors



G9201 to G9204 series

Image sensor for DWDM wavelength monitor

The G9201 to G9204 series are InGaAs linear image sensors designed for WDM monitor detectors in optical communications. These linear image sensors contain a CMOS charge amplifier array, a CDS circuit, an offset compensation circuit, a shift register and a timing generator, along with an InGaAs photodiode array, and deliver high sensitivity and stable operation in the near infrared range. The package is hermetically sealed for high reliability and the light input window has an anti-reflective coating to improve the light detection efficiency.
The signal processing circuit on the CMOS chip allows selecting two conversion efficiencies (CE) by external voltage. A wide dynamic range can be obtained when the image sensor is operated at CE=16 nV/e^-, while a high gain can be obtained at CE=320 nV/e^-.

Features

- **Wide dynamic range**
- **Low noise and low dark current**
- **Two selectable conversion efficiencies**
- **Anti-saturation circuit**
- **CDS circuit*1**
- **Offset compensation circuit**
- **Simple operation (by built-in timing generator *2)**
- **High resolution: 25 µm pitch (512 ch)**
- **Low crosstalk**
- **256 ch: 1 video line**
  512 ch: 2 video lines

Applications

- **DWDM wavelength monitor**
- **Optical spectrum analyzer**

Options

- **InGaAs multichannel detector head C8061-01*3**
- **Multichannel detector head controller C7557-01*3**

*1: A major source of noise in charge amplifiers is the reset noise generated when the integration capacitance is reset. A CDS circuit greatly reduces this reset noise by holding the signal immediately after reset to find the noise differential.
*2: In conventional image sensor operation, external PLD (programmable logic device), etc. is used to input the required timing signals. However, the G9201 to G9204 series image sensors internally generate all timing signals on the CMOS chip just by supplying CLK and RESET pulses. This makes it simple to set the timings.
*3: The G9203-256D and G9204-512D are not available for the C7557-01.

Selection guide

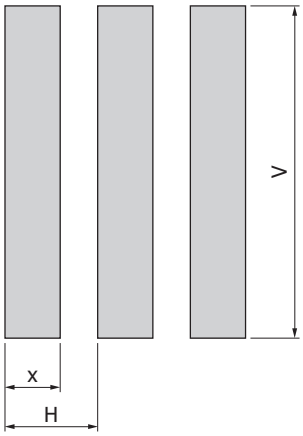
Type no.	Cooling	Image size (mm)	Number of total pixels	Number of effective pixels	Spectral response range (µm)	Defective pixels	Appilcable multichannel detector head
G9201-256S	One-stage TE-cooled	12.8 × 0.25	256	256	0.9 to 1.67 (-10 °C)	0	C8061-01
G9202-512S	One-stage TE-cooled		512	512	0.9 to 1.67 (-10 °C)		C8061-01
G9203-256D*4	Non-cooled	12.8 × 0.50	256	256	0.9 to 1.7 (25 °C)		-
G9203-256S	One-stage TE-cooled		256	256	0.9 to 1.67 (-10 °C)		C8061-01
G9204-512D*4	Non-cooled		512	512	0.9 to 1.7 (25 °C)		-
G9204-512S	One-stage TE-cooled		512	512	0.9 to 1.67 (-10 °C)		C8061-01

Structure

Type no.	Pixel size [µm (H) × µm (V)]	Pixel pitch (µm)	Package	Window material
G9201-256S	50 × 250	50	28-pin metal (refer to the dimensional outline)	Sapphire glass with anti-reflective coating
G9202-512S	25 × 250	25		
G9203-256D*4	50 × 500	50	22-pin ceramic	Borosilicate glass with anti-reflective coating
G9203-256S			28-pin metal (refer to the dimensional outline)	Sapphire glass with anti-reflective coating
G9204-512D*4	25 × 500	25	22-pin ceramic	Borosilicate glass with anti-reflective coating
G9204-512S			28-pin metal (refer to the dimensional outline)	Sapphire glass with anti-reflective coating

*4: For the G9203-256D and G9204-512D specifications, see the separate datasheet available from HAMAMATSU.

Details of photosensitive area (unit: mm)



Number of pixels	x	H	V
256	30	50	250
			500
512	10	25	250
			500

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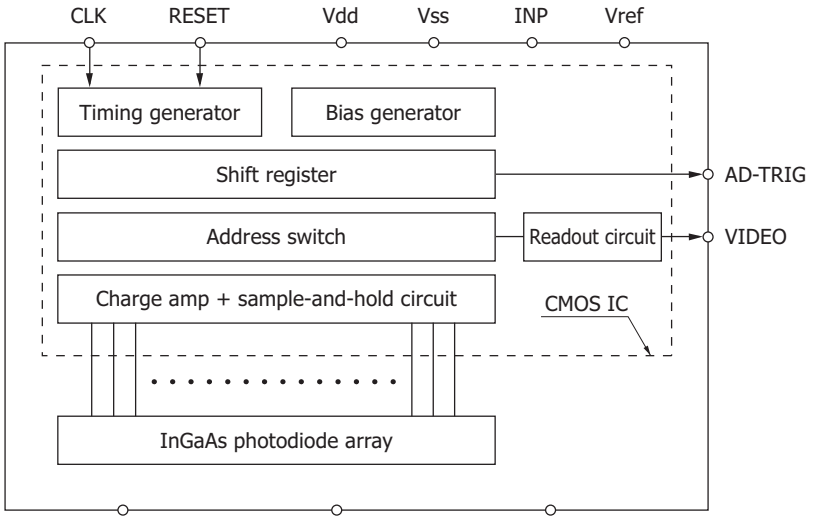
Block diagram



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Absolute maximum ratings

Parameter	Symbol	Condition	Min.	Max.	Unit
Operating temperature	Topr	Chip and package temperature, No dew condensation*5	-40	+70	°C
Storage temperature	Tstg	Chip and package temperature, No dew condensation*5	-40	+85	°C
Supply voltage	Vdd, INP, Vref	Ta=25 °C	-0.3	+6	V
Clock pulse voltage	Vϕ	Ta=25 °C	-0.3	+6	V
Reset pulse voltage	V(RES)	Ta=25 °C	-0.3	+6	V
Gain selection terminal voltage	Vcsel	Ta=25 °C	-0.3	+6	V

*5: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

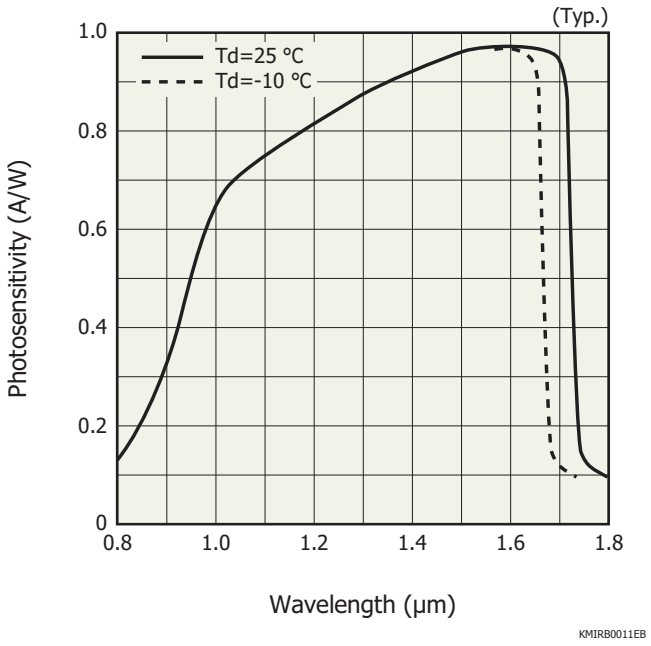
Recommended terminal voltage

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.9	5.0	5.1	V
		Vref	-	1.26	-	V
Element bias		INP	3.5	4.5	4.6	V
Ground		Vss	-	0	-	V
Clock pulse voltage	High	Vϕ	Vdd - 0.5	Vdd	Vdd + 0.5	V
	Low		0	0	0.4	
Reset pulse voltage	High	V(RES)	Vdd - 0.5	Vdd	Vdd + 0.5	V
	Low		0	0	0.4	

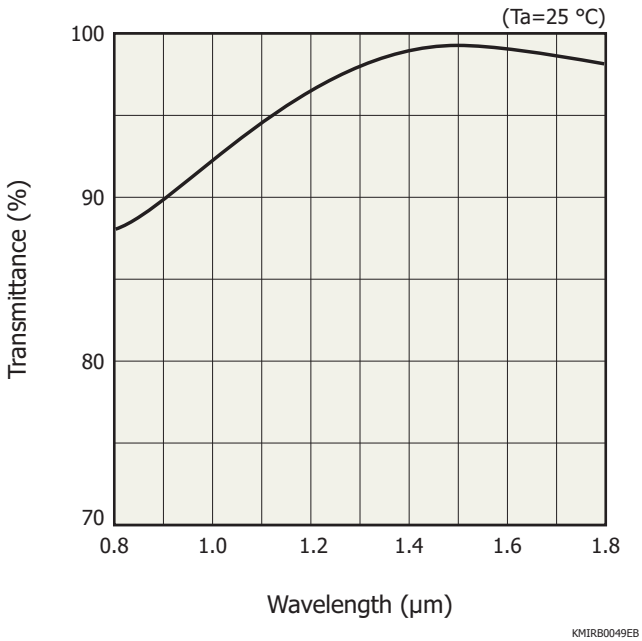
Electrical characteristics (Ta=25 °C)

Parameter		Symbol		Min.	Typ.	Max.	Unit
Consumption current		I(Vdd)	256 pixels	-	45	50	mA
			512 pixels	-	90	100	
		I(Vref)		-	-	1	mA
		I(INP)		-	-	1	mA
Clock frequency		f		0.1	-	4	MHz
Video data rate		fV		0.0125	f/8	0.5	MHz
Video output voltage	High	V_H		-	4.5	INP	V
	Low	V_L		Vref	1.26	-	V
Output offset voltage		Vos		-	Vref	-	V
A/D trigger voltage	High	V_{trigH}		-	Vdd	-	V
	Low	V_{trigL}		-	GND	-	V

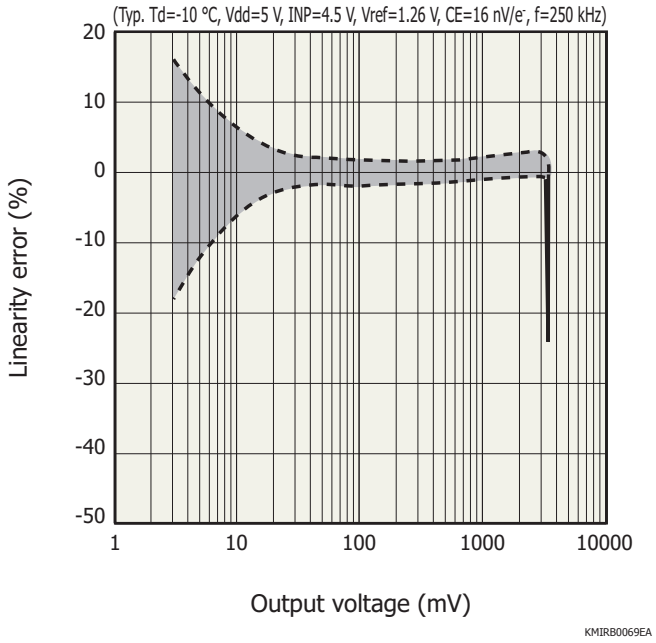
Spectral response



Spectral transmittance characteristic of window material (typical example)



Linearity error (G9203-256S)



Electrical and optical characteristics (Td=25 °C)

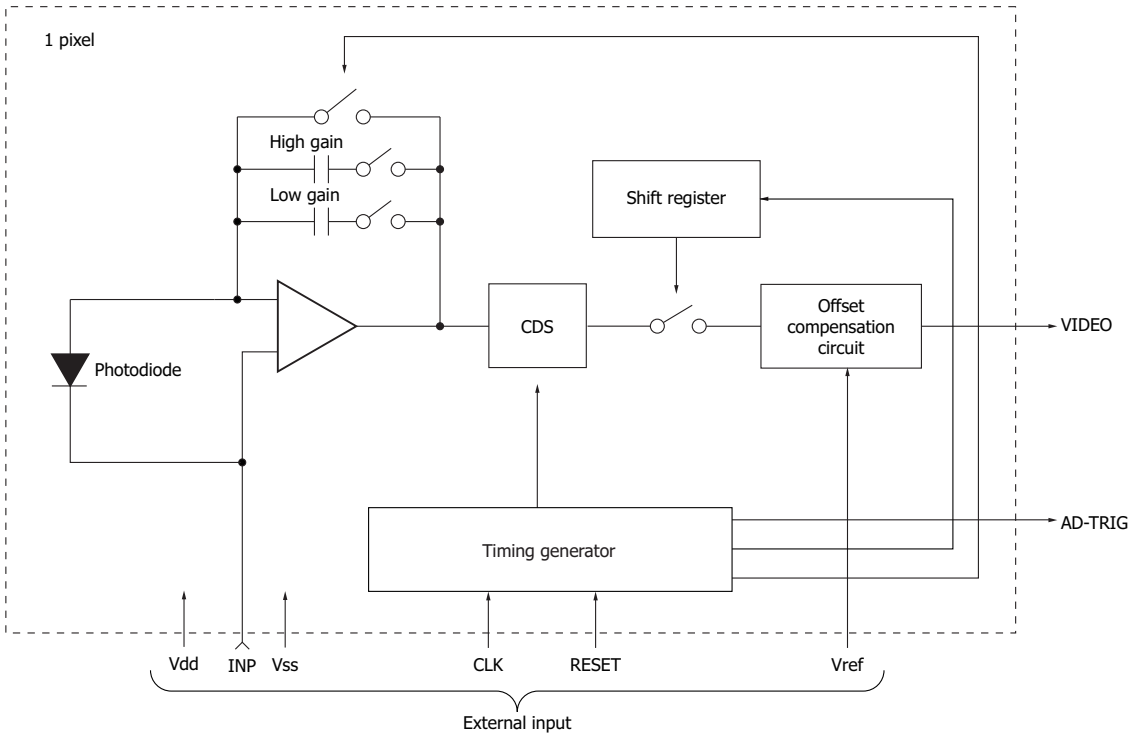
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Peak sensitivity wavelength	λp		-	1.55	-	µm
Photosensitivity	S	λ=λp	0.85	0.95	-	A/W
Conversion efficiency	CE	Cf=10pF	-	16	-	nV/e⁻
Saturation voltage	Vsat		3.0	3.2	-	V
Saturation charge	Qsat	*6	30	32	-	pC
Photoresponse nonuniformity	PRNU	*7	-	±2	±5	%
RMS noise voltage (readout noise)	N	Standard deviation, Integration count=50	-	180	300	µV rms
Dynamic range	D	*6	10000	17777	-	-
Defective pixels*8	-		-	-	0	%

*6: Vϕ=5 V, CE=16 nV/e⁻
*7: 50 % of saturation, integration time=10 ms, after dark output subtraction, excluding first and last pixels
*8: Pixels with photoresponse nonuniformity, readout noise or dark current higher than the maximum value

Dark output characteristics (Td=25 °C, CE=16 nV/e⁻)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Dark output (dark output nonuniformity)	G9201-256S	V_D	-1	0.2	1	V/s
	G9202-512S		-0.5	0.1	0.5	
	G9203-256S		-2	0.4	2	
	G9204-512S		-0.5	0.1	0.5	
Dark current	G9201-256S	I_D	-10	2	10	pA
	G9202-512S		-5	1	5	
	G9203-256S		-20	4	20	
	G9204-512S		-5	1	5	

Equivalent circuit



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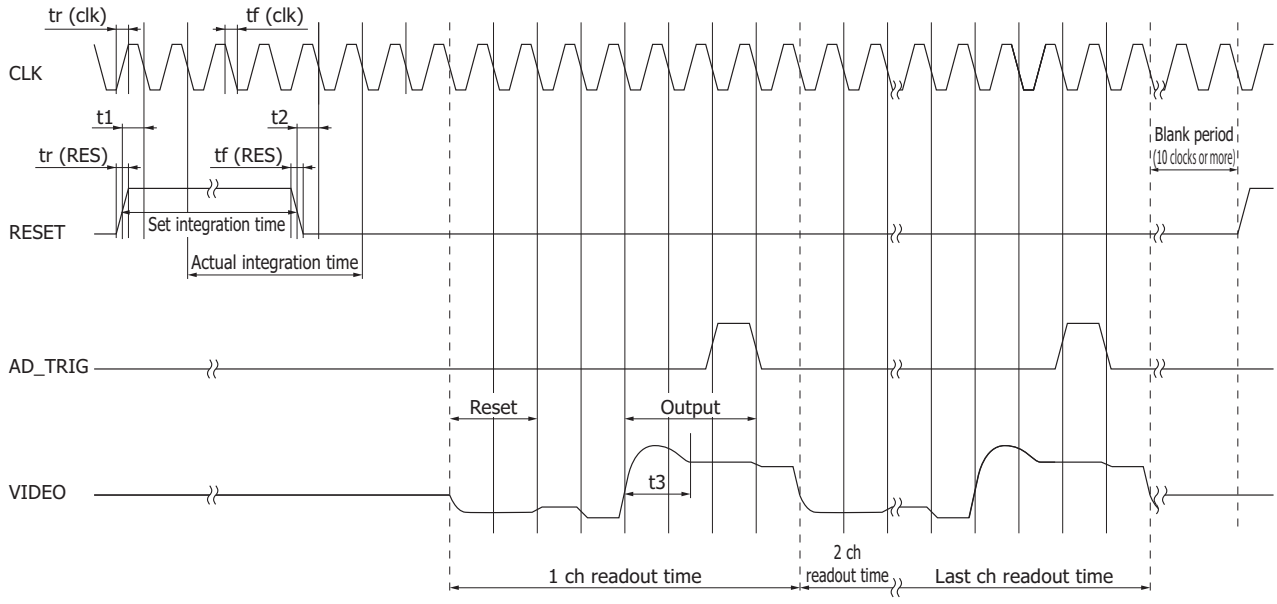
Timing chart



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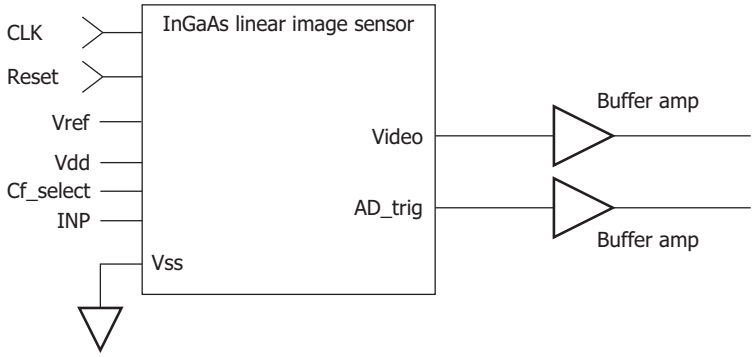
Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	-	0.1	-	4	MHz
Clock pulse width	tpw (clk)	100	-	-	ns
Clock pulse rise/fall times	tr (clk), tf (clk)	0	20	100	ns
Reset pulse width	tpw (RES)	6000	-	-	ns
Reset pulse rise/fall times	tr (RES), tf (RES)	0	20	100	ns
Reset (rise) timing	t1	50	-	-	ns
Reset (fall) timing	t2	50	-	-	ns
Output settling time	t3	-	-	600	ns

Basic circuit connection



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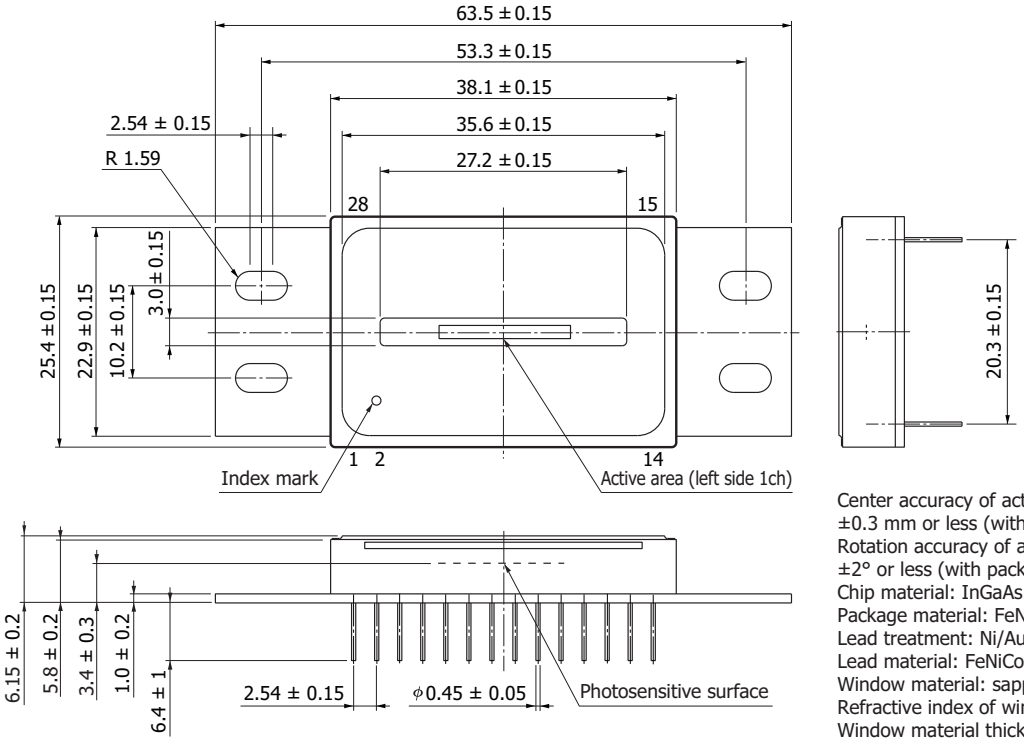
Dimensional outline (unit: mm)



Center accuracy of active area:
±0.3 mm or less (with package center as reference point)
Rotation accuracy of active area:
±2° or less (with package center as reference point)
Chip material: InGaAs
Package material: FeNi alloy
Lead treatment: Ni/Au plating
Lead material: FeNiCo alloy
Window material: sapphire
Refractive index of window material: n=1.76
Window material thickness: 0.66 mm
AR coat: coated (1.55 µm peak)
Window sealing method: brazing
Cap sealing: welding

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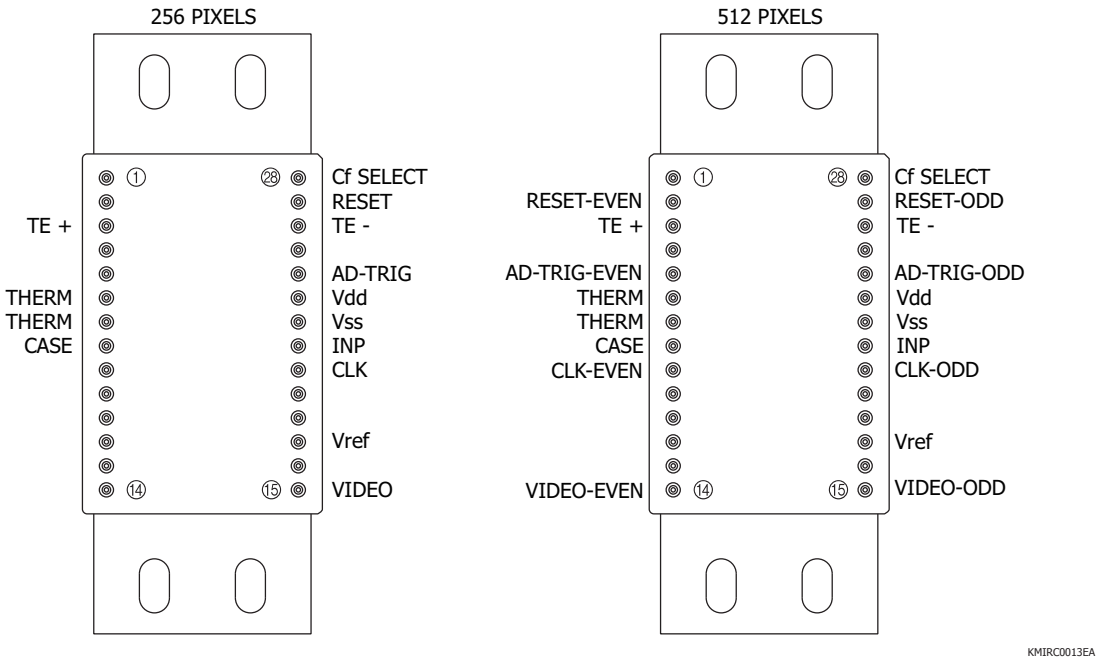
Pin connections (top view)



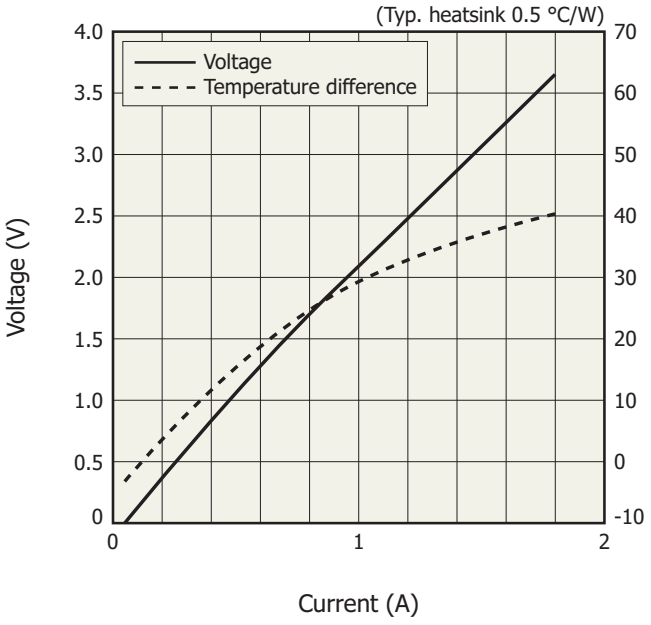
Terminal name	Input/Output	Function and recommended connection
CLK	Input (CMOS logic compatible)	Clock pulse for operating the CMOS shift register
RESET	Input (CMOS logic compatible)	Reset pulse for initializing the feedback capacitance in the charge amplifier formed on the CMOS chip. The width of the reset pulse is integration time.
Vdd	Input	Supply voltage for operating the signal processing circuit on the CMOS chip
Vss	-	Ground for the signal processing circuit on the CMOS chip
INP	Input	Reset voltage for the charge amplifier array on the CMOS chip
Cf SELECT	Input	Voltage that determines the feedback capacitance (Cf) on the CMOS chip. Low gain (CE=16 nV/e^-) at 0 V, and high gain (CE=320 nV/e^-) at 5 V.
CASE	-	This terminal is electrically connected to the package.
THERM	Output	Thermistor terminal for monitoring temperature inside the package
TE+, TE-	Input	Power supply terminal for the thermoelectric cooler that cools the photodiode array
AD-TRIG	Output	Digital signal for A/D conversion; positive polarity
VIDEO	Output	Analog video signal; positive polarity
Vref	Input	Reset voltage for the offset compensation circuit on the CMOS chip

Specifications of one-stage TE-cooler (Ta=25 °C, Vdd=5 V, INP=4.5 V)

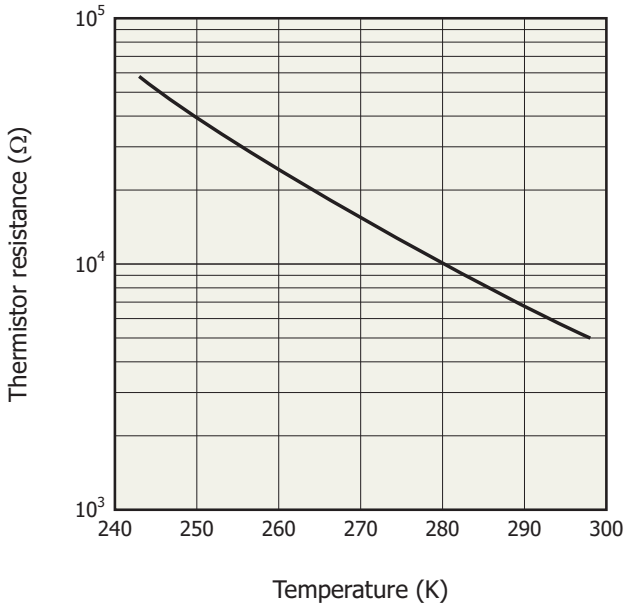
Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
TE-cooler allowable current		Ic Max.	-	-	1.8	A
TE-cooler allowable voltage		Vc Max.	-	-	5.0	V
Temperature difference *8	Ic=1.4 A	Δt	40	-	-	°C
Thermistor resistance		Rth	4.85	5.00	5.15	kΩ
Thermistor power dissipation		Pth	-	-	0.2	mW

*8: This is a temperature difference between the surface of active area and the heat radiating portion of package.

One-stage TE-cooler temperature characteristic



Thermistor temperature characteristic



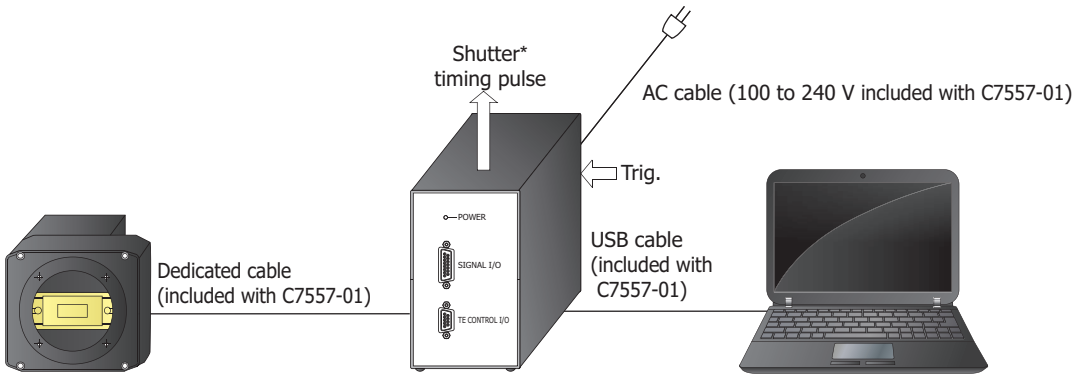
A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R1 = R2 \times \exp B\,(1/T1 - 1/T2)$

R1: Resistance at T1 [K]
R2: Resistance at T2 [K]
B : B constant (B=3200 K ± 2%)

Thermistor resistance = 5 kΩ ± 3% (298 K)

Connection of related products



* Shutter, etc. are not available.

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Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

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