SIEMENS

ICs for Communications

ISDN Echocancellation Circuit for Terminal Applications
IEC-Q TE

PSB 21911 Version 5.2

PSF 21911 Version 5.2

Data Sheet 11.97

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1 Overview

The PSB 21911, IEC-Q TE Version 5.2, is a specific derivative of the PEB 2091, IEC-Q for terminal and small PBX applications. It features all necessary functions required for NTs and terminal applications like PC add-on cards and terminal adapters.

In stand-alone mode the PSB 21911 IEC-Q TE Version 5.2 can be used fully pin compatible to IEC-Q V4.4 and former versions. In µP mode it offers a parallel or serial microprocessor interface.

The Processor Interface (PI) of the IEC-Q TE V 5.2 establishes the access of a microprocessor between U-interface and IOM-2. It's main function is illustrated in **figure 1**.

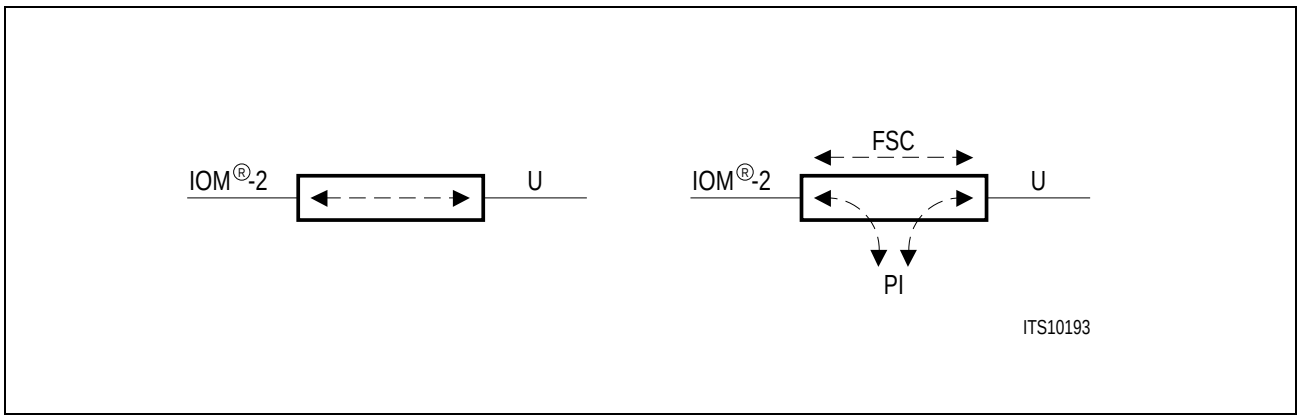


Figure 1 Stand-Alone Mode (left) and µP Mode (right)

In µP mode B channels, D channel, C/I codes and Monitor commands can either be passed between the U-transceiver and IOM-2 directly, or they can be looped through the µP via the PI. Any selection of "passed" or "looped" channels can be programmed via a control register.

The µP-interface mode is enabled by setting the pin PMODE to "1". This pin was not to be connected in older versions of the IEC-Q. Its internal pull down resistor selects the stand-alone mode, if the pin is left open.

In stand-alone mode the IEC-Q TE is controlled exclusively via the IOM-2 interface and mode selection pins.

SIEMENS

ISDN Echocancellation Circuit for Terminal Applications IEC-Q TE

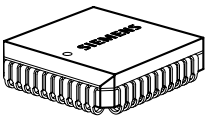
PSB 21911

Version 5.2

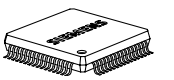
CMOS

1.1 Features

- ISDN U-transceiver with IOM-2 and optional micro-processor interface
- Compatible to NT modes and TE mode of PEB 2091 IEC-Q V5.1
- Perfectly suited for terminal and TA applications
- U-interface (2B1Q) conform to ANSI T1.601, ETSI ETR 080 and CNET ST/LAA/ELR/DNP/822:
  - Meets all transmission requirements on all ANSI, ETSI and CNET loops with margin
  - Conform to British Telecom's RC7355E
  - Compliant with ETSI 10ms micro interruptions
- IOM-2 interface for connection of e.g. ISAC-S, SICOFI-2/4TE, ARCOFI, ITAC, HSCX-TE, ISAR, IPAC, 3PAC
- Pin compatible to version 4.4 in the P-LCC-44 package



P-LCC-44



T-QFP-64

In µP mode:

- Parallel or serial microprocessor interface and watchdog
- µP access to B-channels, D-channel and intercommunication channels
- µP access to IOM-2 Monitor-channels and C/I-channels
- Adjustable microcontroller clock source between 0.96MHz and 7.68MHz
- Selection between Bit clock (BCL) and Data clock (DCL)
- Supports synchronization of basestations in cordless applications (e.g. RITL)
- Supports D-channel arbitration with ELIC linecard (e.g. PBX)

In all modes:

- Single 5 Volt power supply
- Low power CMOS technology with power down mode

1.2 Logic Symbol µP Mode

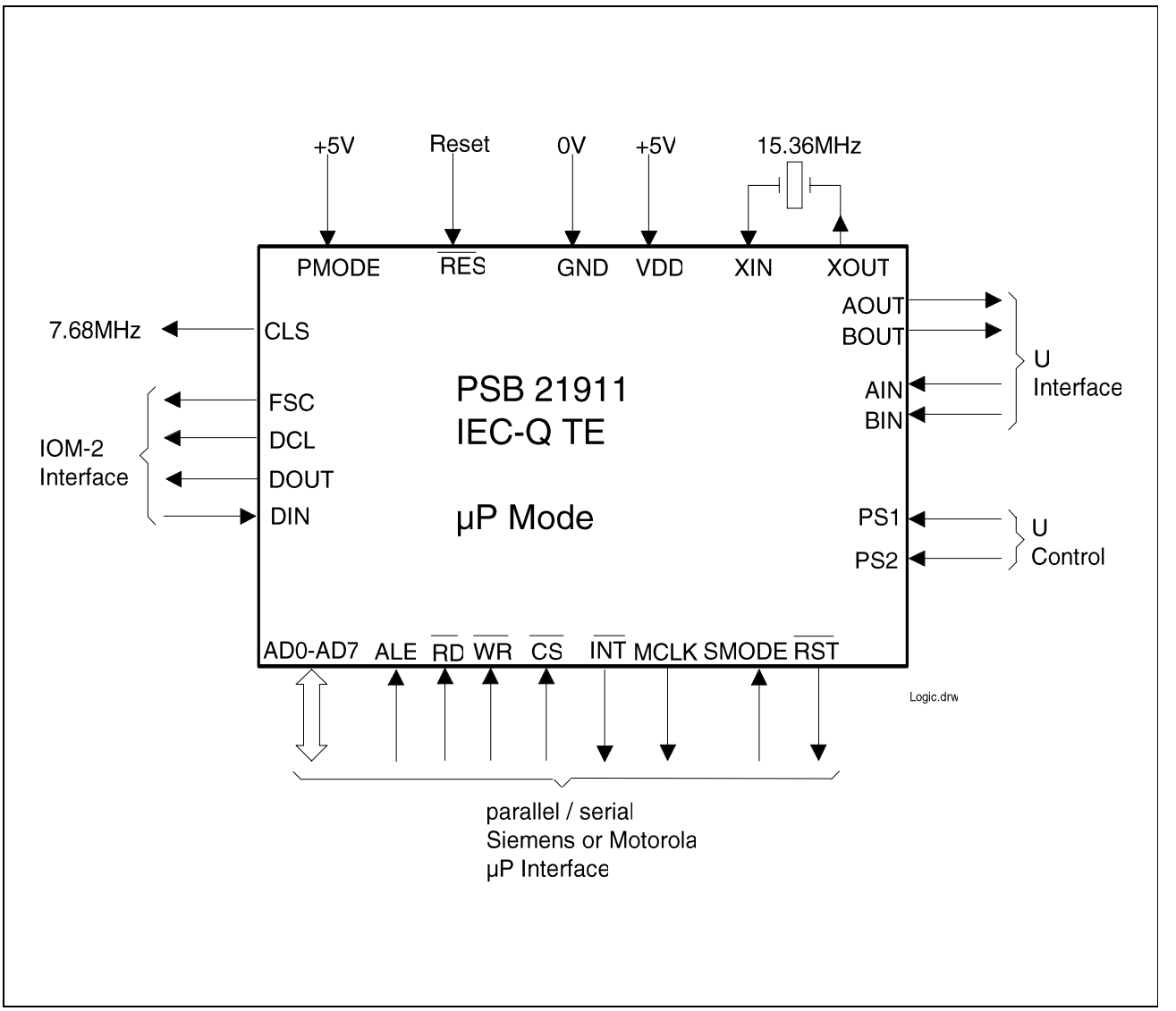


Figure 2 Logic Symbol µP Mode

1.3 Logic Symbol Stand-Alone Mode

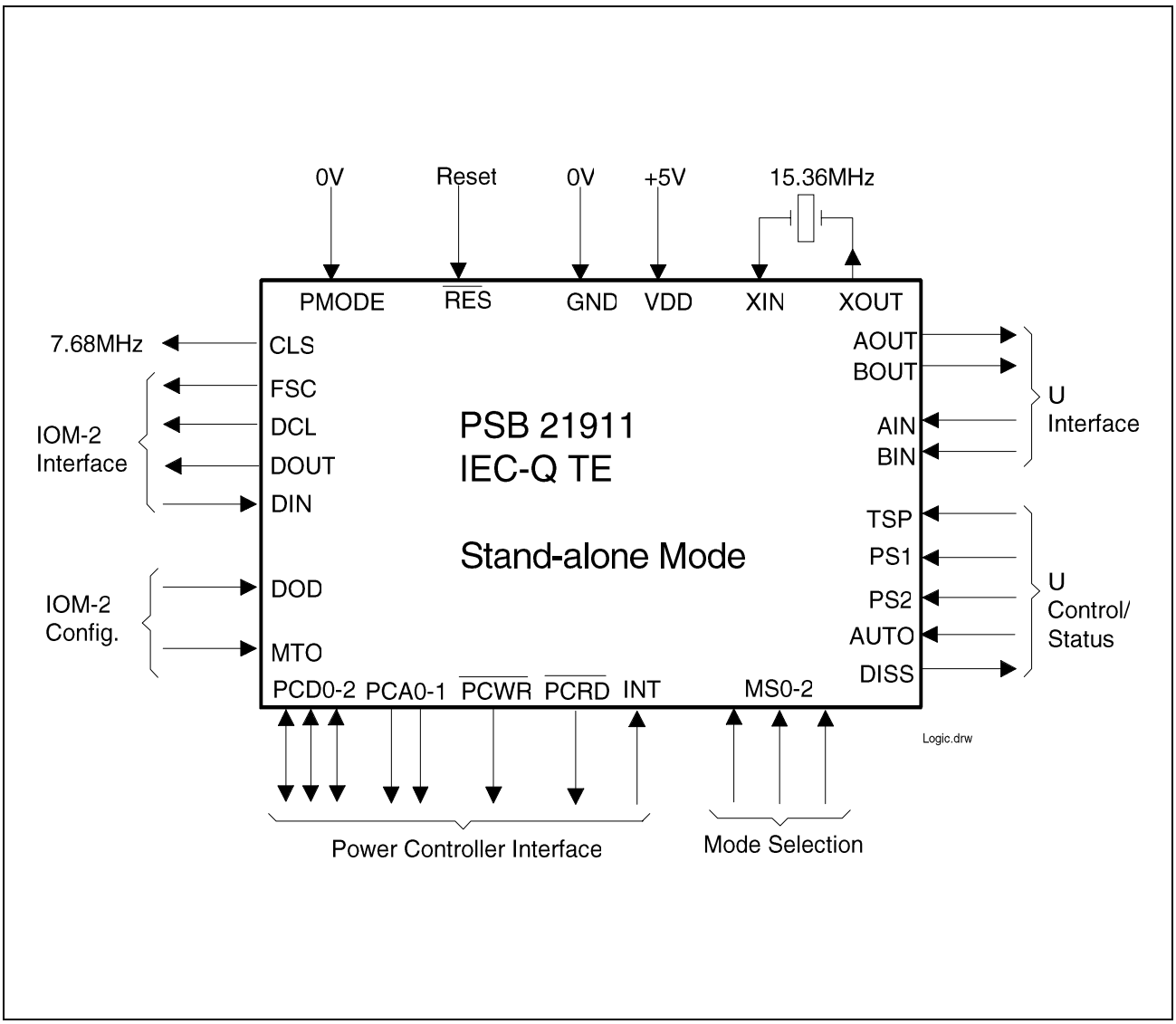


Figure 3 Logic Symbol Stand-Alone Mode

1.4 Pin Configuration

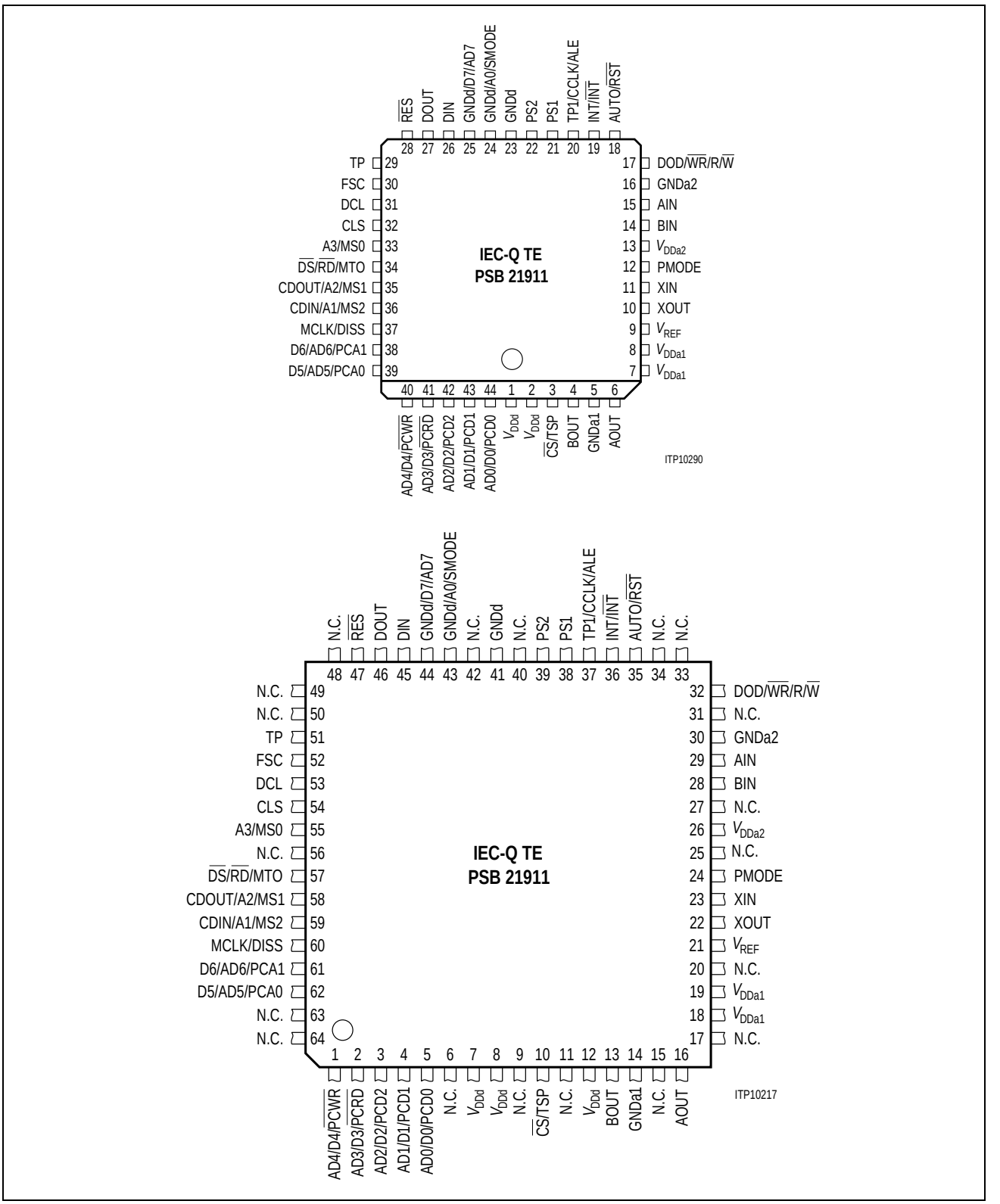


Figure 4 Pin Configuration P-LCC-44 and T-QFP-64 Package (top view)

1.5 Pin Definitions and Functions

The following tables group the pins according to their functions. They include pin name, pin number, type and a brief description of the function.

Pin No.		Symbol		I/O	Function
P-LCC-44	**T-QFP64**	**Stand-alone**	**µP mode**		
Power Supply Pins					
1, 2	7, 8, 12	V_{DDd}	V_{DDd}	I	5 V ± 5% digital supply voltage
5	14	GNDa1	GNDa1	I	0 V analog
7, 8	18, 19	V_{DDa1}	V_{DDa1}	I	5 V ± 5% analog supply voltage
9	21	V_{REF}	V_{REF}	O	V_{REF} pin to buffer internally generated voltage with capacitor 100 nF vs GND
13	26	V_{DDa2}	V_{DDa2}	I	5 V ± 5% analog supply voltage
16	30	GNDa2	GNDa2	I	0 V analog
23	41	GNDd	GNDd	I	0 V digital
Mode Selection Pins					
3	10	TSP		I	**Single Pulse Test Mode** For activation refer to table 3 on page 27. When active, alternating 2.5 V pulses are issued in 1.5 ms intervals. Tie to GND if not used.
			$\overline{CS}$	I	**Chip Select** (Multiplexed, demultiplexed and serial modes)**:** Low active.
18	35	AUTO		I	**Auto EOC Mode** Selection between auto- and transparent mode for EOC channel processing. (Automode = (1))
			$\overline{RST}$	O	**Reset output** (Multiplexed, demultiplexed and serial modes): Low active.

Pin No.		Symbol		I/O	Function
P-LCC-44	T-QFP64	Stand-alone	µP mode		
24	43	GNDd		I	**GNDd** Must be connected to GNDd in stand-alone mode.
			A0	I	**Address Bus Pin** (Demultiplexed mode)
			SMODE	I	**Serial Mode Pin:** SMODE = 1 selects serial mode, SMODE = 0 enables the multiplexed mode.
25	44	GNDd		I	**GNDd** Must be connected to GNDd in stand-alone mode.
			D7	I/O	**Data Bus Pin** (Demultiplexed modes)
			AD7	I/O	**Address Data Bus Pin** (Multiplexed mode)
			not used	I	(Serial mode) tie to GND.
33	55	MS0		I	**Mode Selection 0** refer to table 2 on page 26.
			not used	I	(Multiplexed mode) tie to GND.
			A3	I	**Address Bus Pin** (Demultiplexed modes).
			not used		(Serial mode) tie to GND.
35	58	MS1		I	**Mode Selection 1** refer to table 2 on page 26.
			not used	I	(Multiplexed mode) tie to GND.
			A2	I	**Address Bus Pin** (Demultiplexed modes).
			CDOUT	O	**Controller Data Out** CCLK determines the data rate. CDOUT is "high Z" if no data is transmitted.

Pin No.		Symbol		I/O	Function
P-LCC-44	T-QFP64	Stand-alone	µP mode		
36	59	MS2		I	**Mode Selection 2** refer to table 2 on page 26.
			not used	I	(Multiplexed mode) tie to GND.
			A1	I	**Address Bus Pin** (Demultiplexed modes).
			CDIN	I	**Controller Data In** (Serial mode) CCLK determines the data rate.
28	47	$\overline{RES}$	$\overline{RES}$	I	**Reset** Low active, must be (0) at least for 10 ns. Refer also to table 3 on page 27 for test modes invoked with this pin.

Power Controller Interface Pins

44	5	PCD0		I/O (PU)	**Data Bus 0 of Power Controller Interface** internal pull-up.
			AD0	I/O	**Address/Data Bus Pin** (Multiplexed mode)
			D0	I/O	**Data Bus Pin** (Demultiplexed modes)
			not used	I	(Serial mode) tie to GND.
43	4	PCD1		I/O (PU)	**Data Bus 1 of Power Controller Interface** Internal pull-up.
			AD1	I/O	**Address/Data Bus Pin** (Multiplexed mode)
			D1	I/O	**Data Bus Pin** (Demultiplexed modes)
			not used	I	(Serial mode) tie to GND.

Pin No.		Symbol		I/O	Function
P-LCC-44	T-QFP64	Stand-alone	µP mode		
42	3	PCD2		I/O (PU)	**Data Bus 2 of Power Controller Interface** Internal pull-up.
			AD2	I/O	**Address/Data Bus Pin** (Multiplexed mode)
			D2	I/O	**Data Bus Pin** (Demultiplexed modes)
			not used	I	(Serial mode) tie to GND.
39	62	PCA0		O	**Address bus 0 of Power Controller Interface**.
			D5	I/O	**Data Bus Pin** (Demultiplexed modes)
			AD5	I/O	**Address Data Bus Pin** (Multiplexed mode)
			not used	I	(Serial mode) tie to GND.
38	61	PCA1		O	**Address bus 1 of Power Controller Interface**
			D6	I/O	**Data Bus Pin** (Demultiplexed modes)
			AD6	I/O	**Address Data Bus Pin** (Multiplexed mode)
			not used	I	(Serial mode) tie to GND.
41	2	$\overline{\text{PCRD}}$		O	**Power Controller Bus Read Request** Low active.
			D3	I/O	**Data Bus Pin** (Demultiplexed modes)
			AD3	I/O	**Address/Data Bus Pin** (Multiplexed mode)
			not used	I	(Serial mode) tie to GND.

Pin No.		Symbol		I/O	Function
P-LCC-44	T-QFP64	Stand-alone	µP mode		
40	1	$\overline{\text{PCWR}}$		O	**Power Controller Bus Write Request** Low active.
			D4	I/O	**Data Bus Pin** (Demultiplexed modes)
			AD4	I/O	**Address/Data Bus Pin** (Multiplexed mode)
			not used	I	(Serial mode) tie to GND.
19	36	INT		I	**Interrupt** Change-sensitive. After a change of level has been detected the C/I code “INT” will be issued on IOM. Tie to GND if not used.
			$\overline{\text{INT}}$	O	**Interrupt Line** (Multiplexed, demultiplexed and serial modes): Low active**.**
37	60	DISS		O	**Disable Power Supply** This pin is set to ’1’ after receipt of MON-0 LBBD in EOC auto-mode.
			MCLK	O	**Microprocessor Clock Output** (Multiplexed, demultiplexed and serial modes): provided with four programmable clock rates: 7.68 MHz, 3.84 MHz, 1.92 MHz and 0.96 MHz.
21	38	PS1	PS1	I	**Power Status 1 (primary)**. ’1’ indicates primary power supply ok. The pin level is identical to the overhead bit ’PS1’ value.
22	39	PS2	PS2	I	**Power Status 2 (secondary)** ’1’ indicates secondary power supply ok. The pin level is identical to the overhead bit ’PS2’ value.

Pin No.		Symbol		I/O	Function
P-LCC-44	T-QFP64	Stand-alone	µP mode		
Miscellaneous Function Pins					
10	22	XOUT	XOUT	O	**Crystal OUT** To connect 15.36-MHz crystal. Leave open if not used.
11	23	XIN	XIN	I	**Crystal IN** To connect 15.36-MHz crystal or external 15.36-MHz clock.
17	32	DOD		I	**DOUT Open Drain** Select open drain with DOD = (1) (external pull-up resistor required) and tristate with DOD = (0). See also table 4 on page 27.
			$\overline{WR}$	I	**Write** (Siemens/Intel multiplexed and demultiplexed modes): indicates a write operation, active low.
			R/$\overline{W}$	I	**Read/Write** (Motorola demultiplexed mode): indicates a read (high) or write (low) operation.
			not used	I	(Serial mode) tie to GND.
29	51	TP	TP	I (PD)	**Test Pin** Not available to user. Do not connect. Internal pull-down resistor.
20	37	TP1		I (PD)	**Test Pin 1** Not available to user. Do not connect. Internal pull-down resistor.
			ALE	I	**Address Latch Enable** (Multiplexed mode): In the Siemens/ Intel µP interface modes a high indicates an address on the AD0..3 pins which is latched with the falling edge of ALE (see also page 39).

Pin No.		Symbol		I/O	Function
P-LCC-44	T-QFP64	Stand-alone	µP mode		
			ALE	I	**Address Latch Enable** (Demultiplexed mode): ALE tied to GND selects the Siemens/Intel type. ALE tied to VDD selects the Motorola type.
			CCLK	I	**Controller Data Clock** (Serial mode): Shifts data from (1) and to (0) the device.
32	54	CLS	CLS	O	**Clock Signal** A 7.68MHz clock, synchronous to the U-interface, is provided on this pin.
12	24	PMODE	PMODE	I (PD)	**Processor Interface Enable** Setting PMODE to "1" enables the Processor Interface**.** Tie to GND or do not connect to select stand-alone mode. Internal pull down.
34	57	MTO		I (PD)	**Monitor Procedure Time-Out** Disables the internal 6 ms Monitor time-out when set to (1). Internal pull-down resistor.
			$\overline{RD}$	I	**Read** (Siemens/Intel multiplexed and demultiplexed modes): indicates a read operation, active low.
			$\overline{DS}$	I	**Data Strobe** (Motorola demultiplexed mode): indicates a data transfer, active low.
			not used	I	(Serial mode) tie to GND.
	6, 9, 11, 15, 20, 25, 27, 31, 33, 34, 40, 48, 49, 50, 51, 63, 64	not used	not used		Leave open for future compatibility.

Pin No.		Symbol		I/O	Function
P-LCC-44	T-QFP64	Stand-alone	µP mode		
IOM®-2 Pins					
31	53	DCL	DCL	O	**Data Clock** Data clock output 512 or 1536 kHz (table 2 on page 26). In µP mode this pin can be programmed to deliver a bit clock (256 or 768 kHz).
30	52	FSC	FSC	O	**Frame Synchronization Clock** The start of the B1-channel in time-slot 0 is marked. FSC = (1) for one DCL-period indicates a superframe marker. FSC = (1) for at least two DCL-periods marks a standard frame.
26	45	DIN	DIN	I	**Data In** Input of IOM-2 data synchronous to DCL-clock (Data upstream direction).
27	46	DOUT	DOUT	O	**Data Out** Output of IOM-2 data synchronous to DCL-clock. Open drain or tristate depending on bit/pin DOD (Data Downstream direction).
U-Interface Pins					
15	29	AIN	AIN	I	**Differential U-Interface Input** Connect to hybrid.
14	28	BIN	BIN	I	**Differential U-Interface Input** Connect to hybrid.
6	16	AOUT	AOUT	O	**Differential U-Interface Output** Connect to hybrid.
4	13	BOUT	BOUT	O	**Differential U-Interface Output** Connect to hybrid.

PU: internal pull-up resistor

PD: internal pull-down resistor

1.6 Microprocessor Bus Interface (Overview)

The table below gives an overview of the different microprocessor bus modes.

Table 1 Microprocessor Bus Interface

Pin number		Stand-alone mode	Symbol in processor mode			
P-LCC 44	T-QFP 64		Siemens/ Intel multiplexed	Siemens/ Intel demultiplexed	Motorola demultiplexed	Serial
12	24	PMODE = 0	PMODE = 1			
45	5	PCD0	AD0	D0	D0	n.c.
43	4	PCD1	AD1	D1	D1	n.c.
42	3	PCD2	AD2	D2	D2	n.c.
41	2	$\overline{\text{PCRD}}$	AD3	D3	D3	n.c.
40	1	$\overline{\text{PCWR}}$	AD4	D4	D4	n.c.
39	62	PCA0	AD5	D5	D5	n.c.
38	61	PCA1	AD6	D6	D6	n.c.
25	44	GNDd	AD7	D7	D7	n.c.
19	36	INT	$\overline{\text{INT}}$	$\overline{\text{INT}}$	$\overline{\text{INT}}$	$\overline{\text{INT}}$
24	43	GNDd	SMODE=0	A0	A0	SMODE=1
36	59	MS2	n.c.	A1	A1	CDIN
35	58	MS1	n.c.	A2	A2	CDOUT
33	55	MS0	n.c.	A3	A3	n.c.
20	37	TP1	ALE	ALE=0	ALE=1	CCLK
34	57	MTO	$\overline{\text{RD}}$	$\overline{\text{RD}}$	$\overline{\text{DS}}$	n.c.
17	32	DOD	$\overline{\text{WR}}$	$\overline{\text{WR}}$	R/$\overline{\text{W}}$	n.c.
3	10	TSP	$\overline{\text{CS}}$	$\overline{\text{CS}}$	$\overline{\text{CS}}$	$\overline{\text{CS}}$
37	60	DISS	MCLK			
18	35	AUTO	$\overline{\text{RST}}$			

1.7 System Integration

Due to the IOM-2 interface the IEC-Q TE can be combined with a variety of other devices to fit in numerous applications. This chapter only shows some typical applications of the IEC-Q TE.

1.7.1 ISDN PC Adapter Card

An ISDN adapter card which supports the U-interface may be realized using the IEC-Q TE together with the PSB 2113 3PAC (**figure 5**). The 3PAC provides a D-channel and two B-channel HDLC controllers. Optionally, a PSB 2132 SICOFI2-TE can be connected to provide two POTS interfaces. If an S-interface is required, the PSB 2115 IPAC can be used instead of the 3PAC.

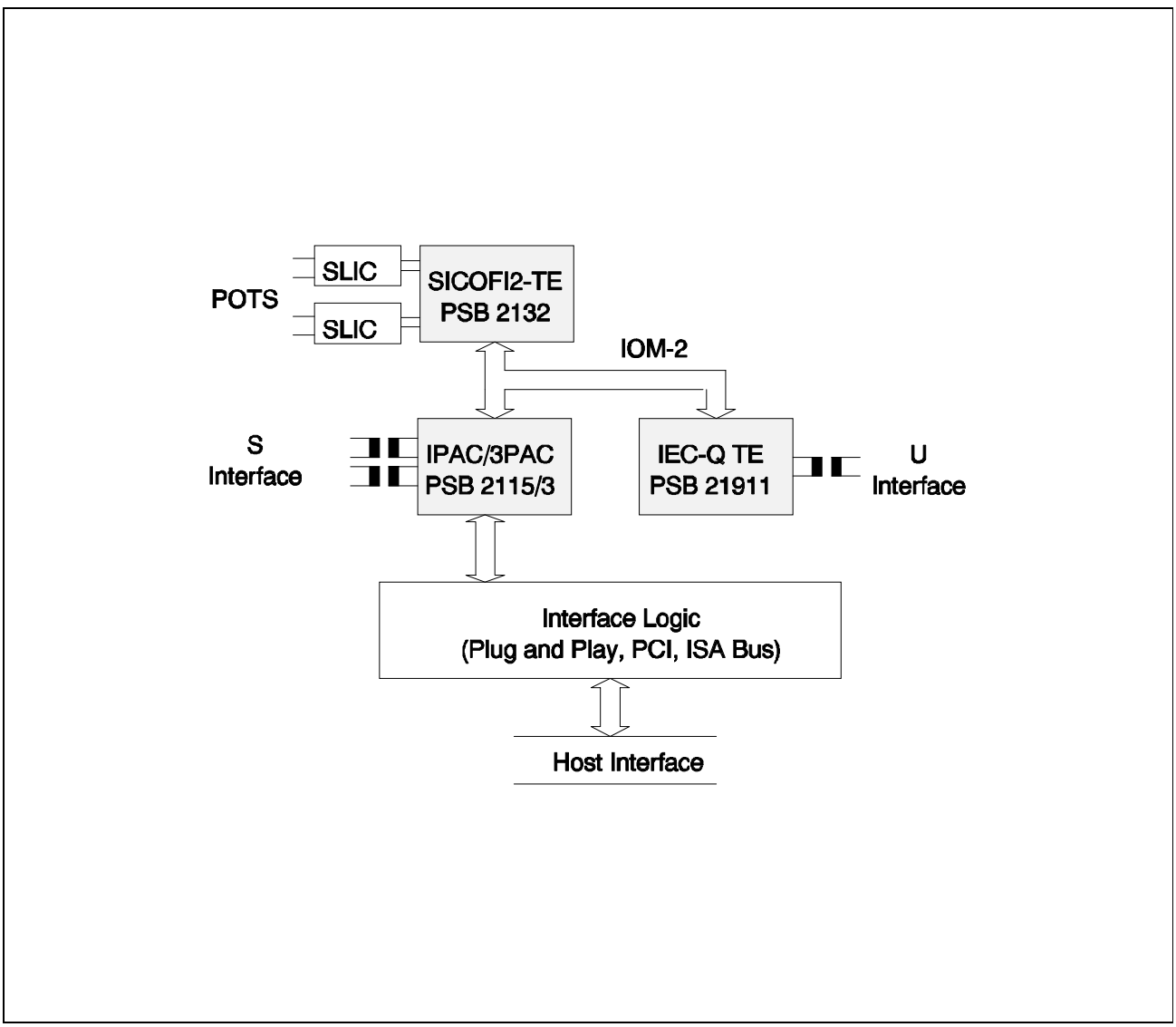


Figure 5 ISDN PC Adapter Card

1.7.2 ISDN Stand-Alone Terminal with POTS Interface

The IEC-Q TE can be integrated in a microcontroller based stand-alone terminal (figure 6) that is connected to the communications interface of a PC. The PSB 2132 SICOFI-TE enables connection of analog terminals (e.g. telephones or fax) to its dual channel POTS interface.

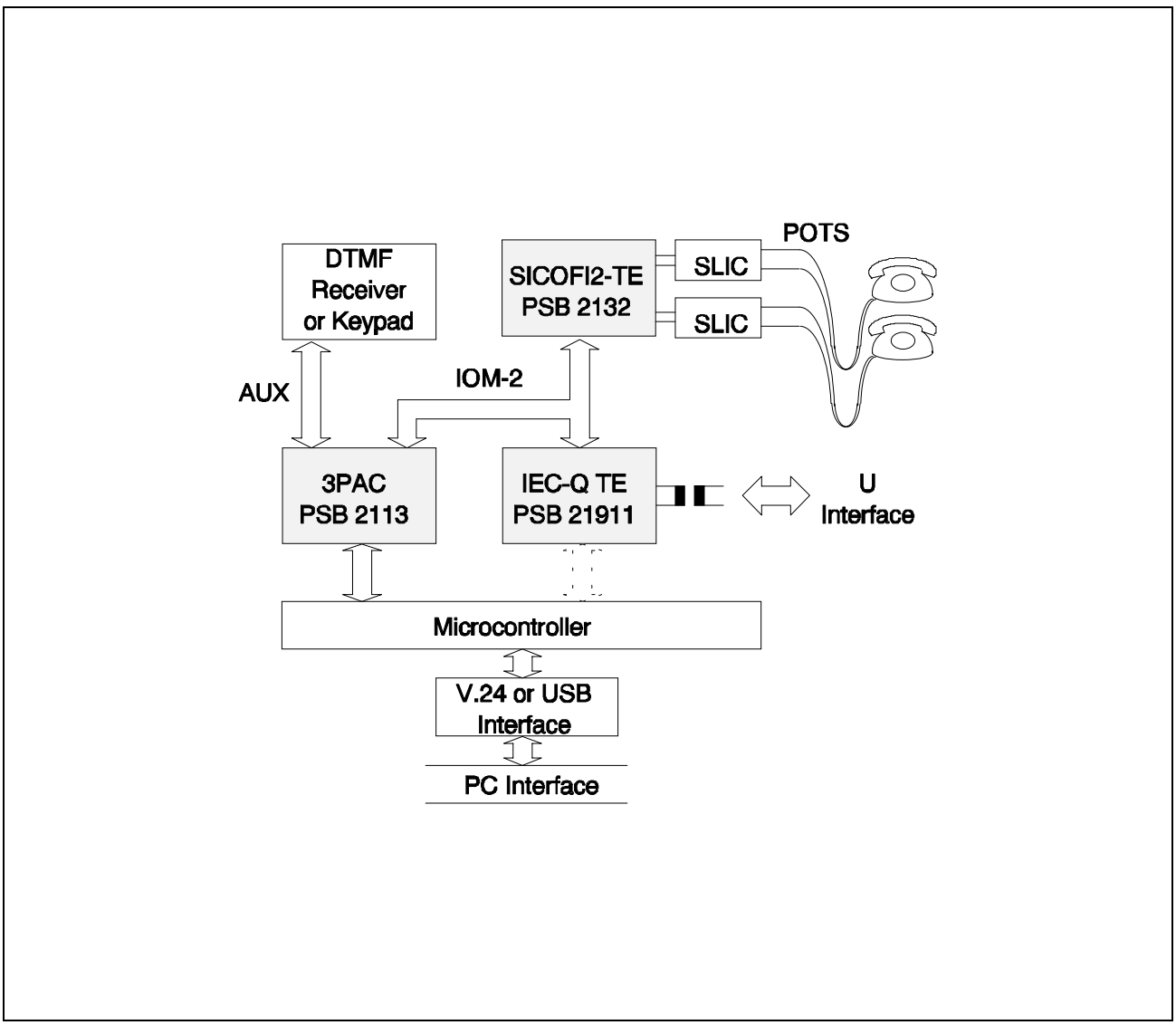


Figure 6 ISDN Stand-Alone Terminal with POTS Interface

1.7.3 ISDN Feature Phone

An ISDN feature phone with U-interface can be built using the IEC-Q TE together with the ARCOFI-SP and the ICC.

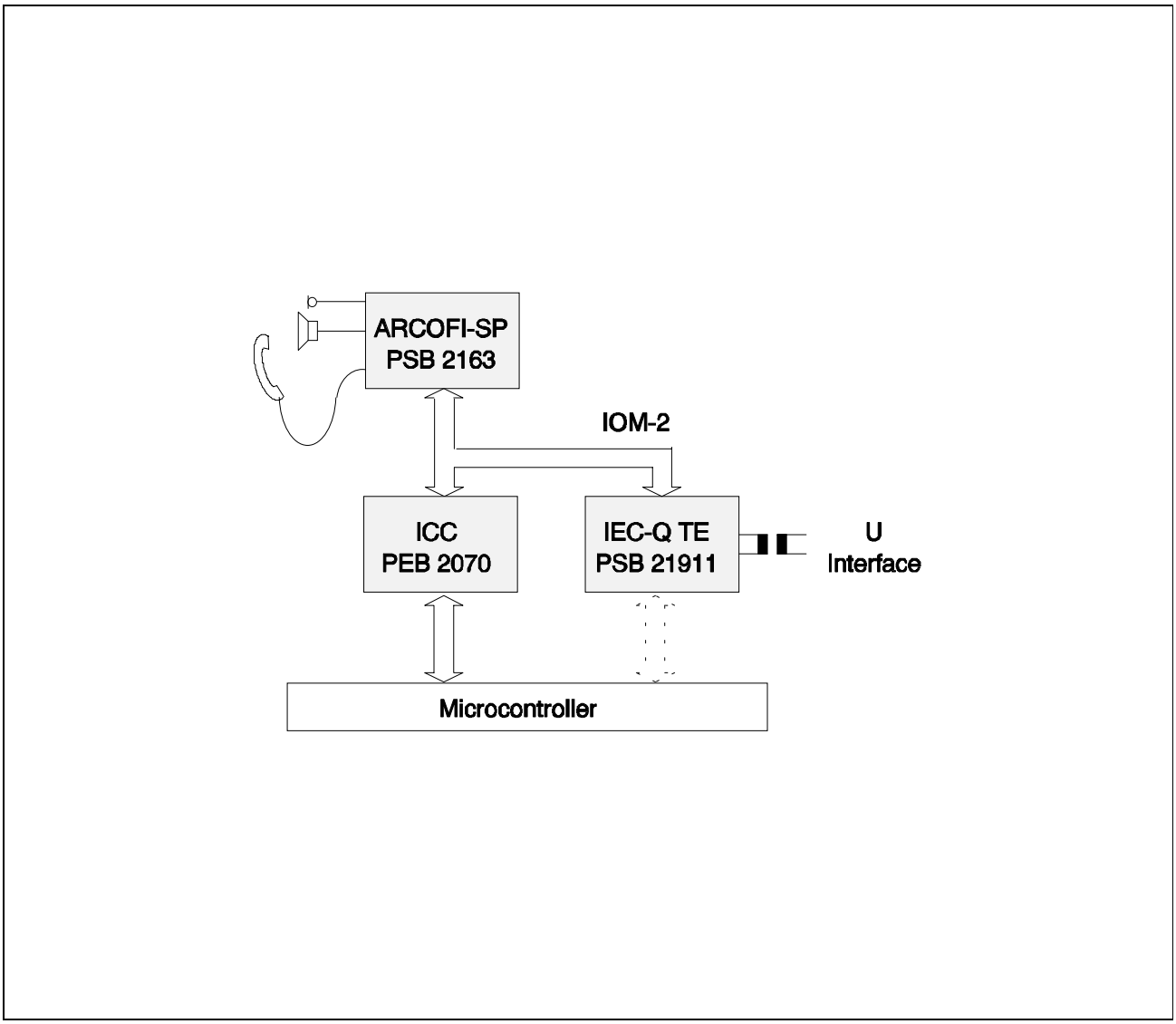


Figure 7 ISDN Feature Phone

1.7.4 ISDN-Modem PC Card

The combination of the IEC-Q TE and a PSB 7115 ISAR 34 allows to build an ISDN-modem PC card .

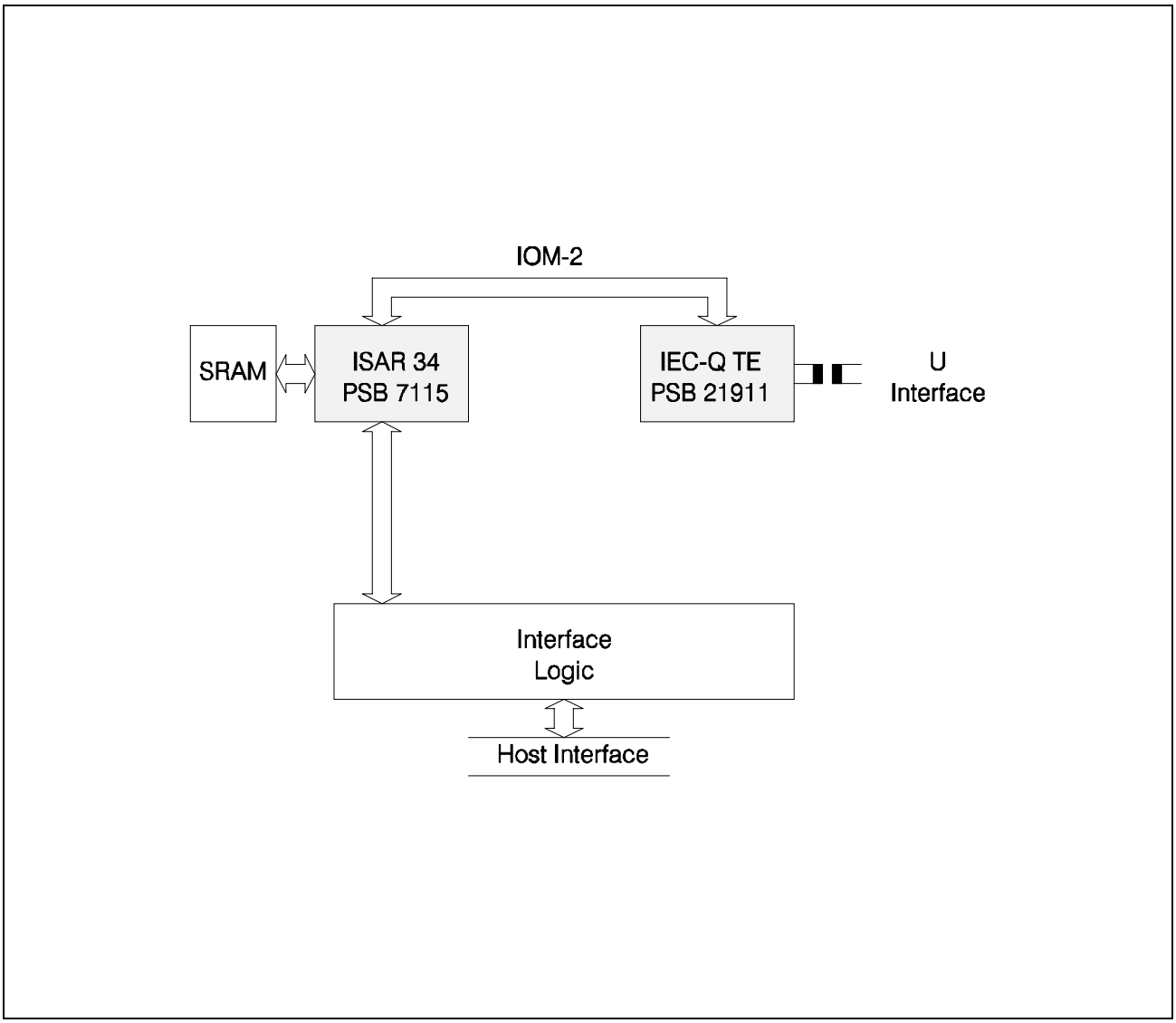


Figure 8 ISDN-Modem PC Card

2 Functional Description

2.1 Operating Modes

The default configuration after power-on or external reset depends on the state of the PMODE pin. The cases µP mode and stand-alone mode have to be distinguished:

µP mode (PMODE = VDD)

In µP mode a microprocessor interface gives access to the IOM-2 channel registers as well as configuration registers. The operating mode is selected via bits STCR:MS0-MS2 according to **table 2** . The STCR register is described on page 119.

Test modes Send Single Pulses, Quiet Mode or Data Through are invoked via the corresponding C/I channel command (page 75) or via bits STCR:TM1-2 (**table 3**).

Stand-alone mode (PMODE = GND)

In stand-alone mode the operating mode is selected via pin strapping according to **table 2**. It is possible to change the mode of a device during operation (e.g. for test purposes) if the mode change is followed by a reset.

The test modes Send Single Pulses (SSP), Quiet Mode (QM) and Data Through (DT) are invoked via the corresponding C/I channel command (page 75) or via pins $\overline{\text{RES}}$ and TSP (**table 3**).

Table 2 Modes of Operation (µP and Stand-Alone Mode)

	Mode Selection			Output Pins U Synchronized		
Mode	**Bit/Pin MS2**	**Bit/Pin MS1**	**Bit/Pin MS0**	**DCL OUT**	**CLS OUT**	**Super-frame-marker**[1)]
NT	0	0	0	512	7680[2)]	no
NT	1	0	0	512	7680[2)]	yes
NT-Auto	0	0	1	512	7680[2)]	no
TE	0	1	0	1536	7680[2)]	no
TE	1	1	0	1536	7680[2)]	yes
reserved	others					

Notes: [1)] 1 DCL-period high-phase of FSC at superframe position
2 DCL-periods high-phase of FSC at normal position
[2)] CLS-clock signal not available while device is in power-down

Table 3 Test Modes

Test-Mode	Bit TM1/ Pin $\overline{\text{RES}}$	Bit TM2/ Pin TSP
Master-Reset[1)]	0	0
Send Single-Pulses[2)]	1	1
Data-Through[3)]	0	1
Normal	1	0

1) Used for Quiet Mode and Return Loss measurements

2) Used for Pulse Mask measurements

3) Used for Insertion Loss, Power Spectral Density and Total Power measurements

Table 4 DOUT Driver Modes

Mode	Pin $\overline{\text{RES}}$ 1)	Pin TSP 2)	Pin / Bit DOD	Pin DOUT Output Driver		
				Value	DOUT in active time slot	DOUT in passive time slot
Pin-Reset	0	0	x	0	low	int. pull-up
				1	int. pull-up	
Normal (Tristate)	1	0	0	0	low	high Z
				1	high	
Normal (Open Drain 3))	1	0	1	0	low	floating
				1	floating	

1) In stand-alone mode and µP mode

2) Only in stand-alone mode. In µP mode the output driver of pin DOUT is selected via bit DOD in the ADF2 register

3) External pull-up resistors required (typ.1 kΩ)

2.2 Device Architecture

In µP mode the following interfaces and functional blocks are used:

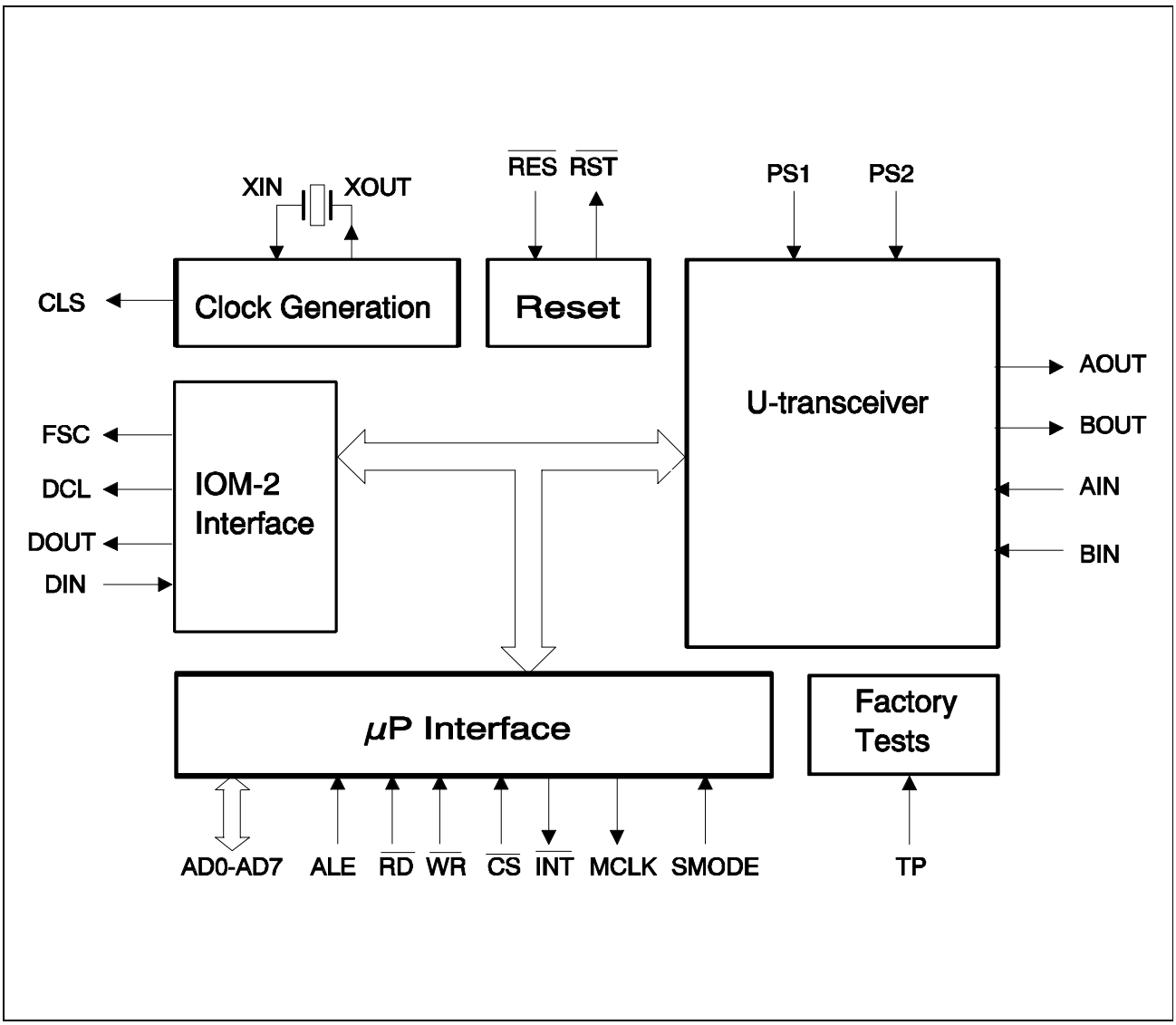


Figure 9 IEC-Q TE Device Architecture (µP Mode)

In stand-alone mode the following interfaces and functional blocks are used:

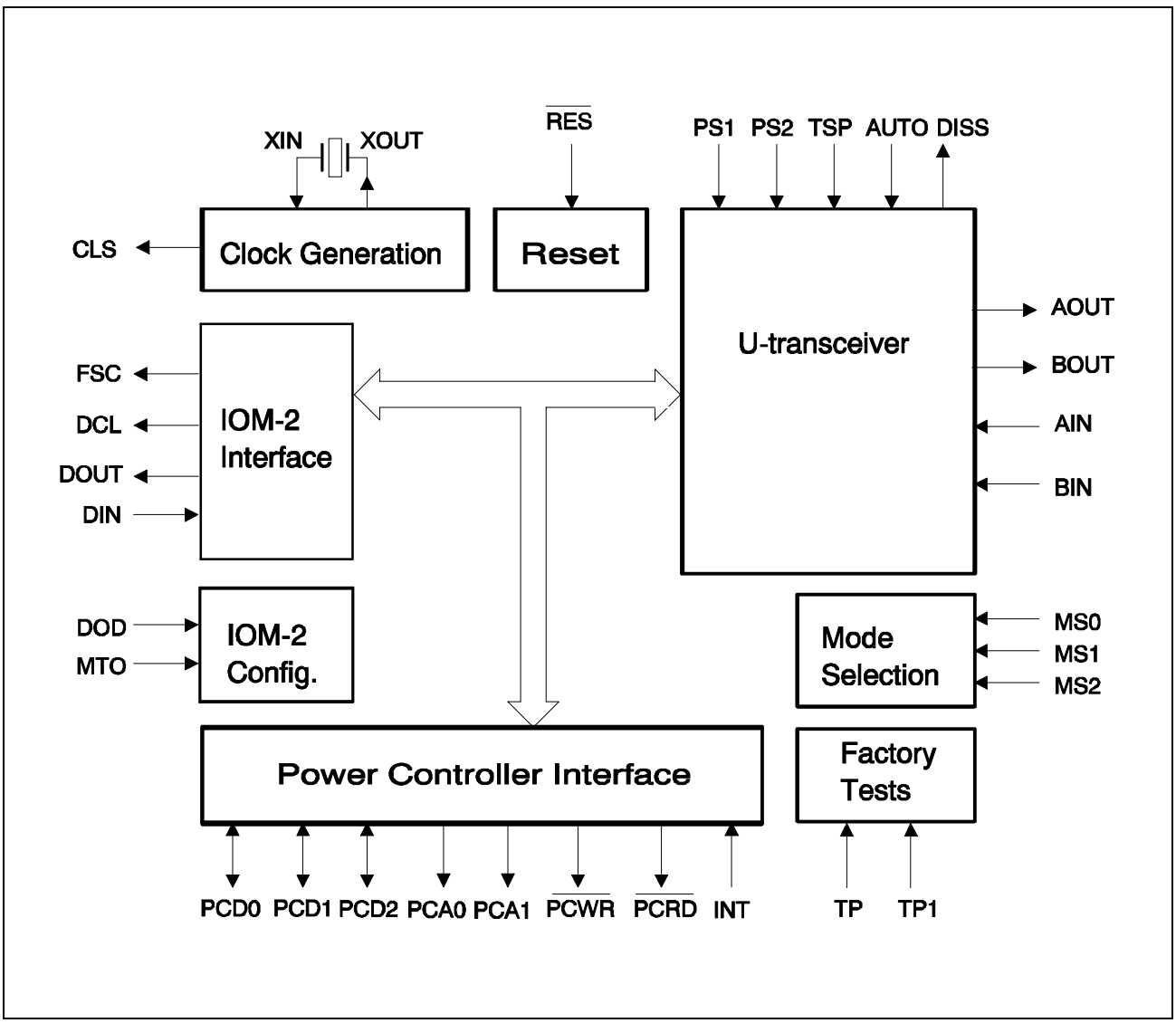


Figure 10 IEC-Q TE Device Architecture (Stand-Alone Mode)

2.3 IOM®-2 Interface

The IOM-2 interface is used to interconnect telecommunication ICs. It provides a symmetrical full-duplex communication link, containing user data, control/programming and status channels. The structure used follows the 2B + 1D-channel structure of ISDN. The ISDN user data rate of 144 kbit/s (B1 + B2 + D) is transmitted in both directions over the interface.

The IOM-2 interface is a generalization and enhancement of the IOM-1 interface.

2.3.1 IOM®-2 Frame Structure

The IOM-2 interface comprises two clock lines for synchronization and two data lines.

Data is carried over Data Upstream (DU) and Data Downstream (DD) signals. The downstream and upstream direction are always defined with respect to the exchange. Downstream refers to information flow from the exchange to the subscriber and upstream vice versa respectively. The IOM-2 Interface Specification describes open drain data lines with external pull-up resistors. However, if operation is logically point-to-point, tristate operation is possible as well.

The data is clocked by a Data Clock (DCL) that operates at twice the data rate. Frames are delimited by an 8-kHz Frame Synchronization Clock (FSC). Incoming data is sampled on every second falling edge of the DCL clock.

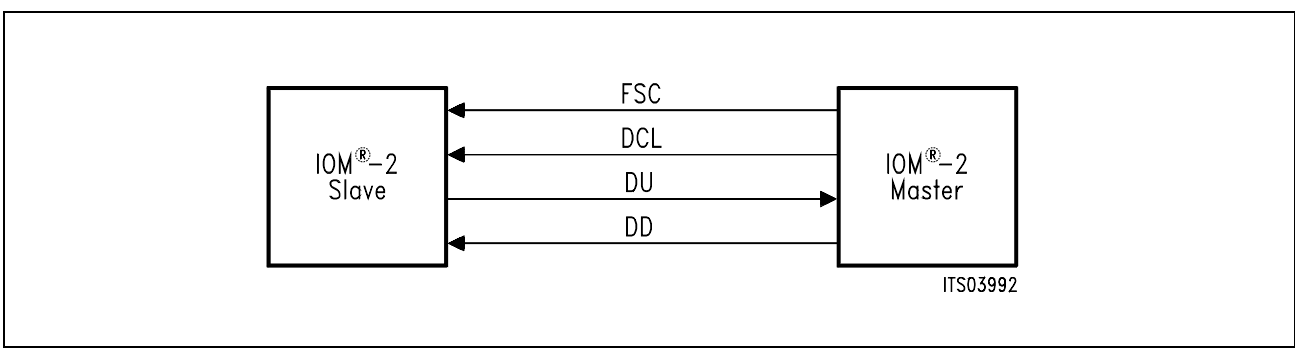


Figure 11 IOM®-2 Clocks and Data Lines

Within one FSC period 32 bit or 96 bit are transmitted, corresponding to DCL frequencies of 512 kHz or 1.536 MHz.

Two optimized IOM-2 timing modes exist:

– NT mode for NT1 applications
– TE mode for terminal and intelligent NT applications

NT or TE mode is selected via pins MS0-2 in stand-alone mode and via bits MS0-2 in µP mode. Both the NT and TE mode utilize the same basic frame and clocking structure, but differ in the number and usage of the individual channels.

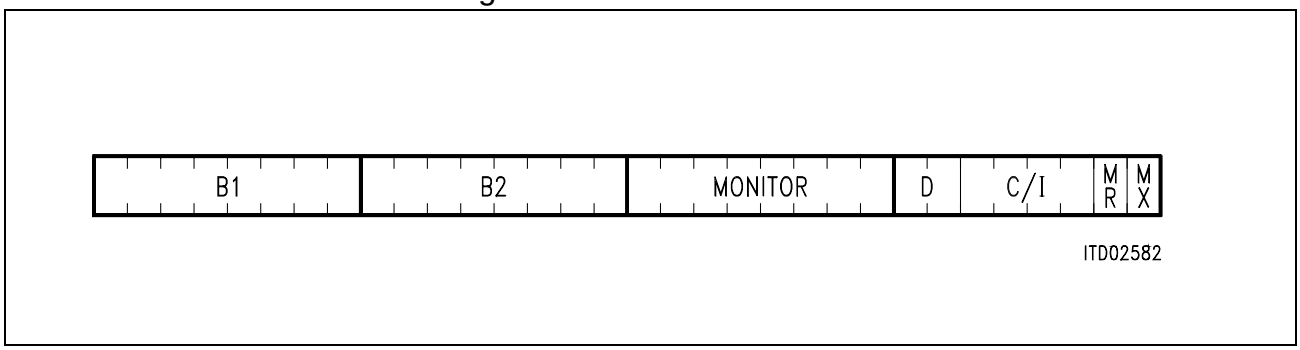


Figure 12 Basic Channel Structure of IOM®-2

Each frame consists of

- two 64 kbit/s channels B1 and B2
- the Monitor channel for transferring maintenance information
- two bits for the 16 kbit/s D-channel
- four command/indication (C/I) bits for controlling of layer-1 functions (U- and S-transceiver).
- two bits MR and MX for the handshake procedure in the Monitor channel

2.3.1.1 TE Mode Frame Structure

In TE mode the IEC-Q TE provides a data clock DCL with a frequency of 1536 kHz. As a consequence the IOM-2 interface provides three channels each with a nominal data rate of 256 kbit/s.

- Channel 0 contains 144 kbit/s (for 2B+D) plus Monitor and Command/Indication channels for the layer-1 device.
- Channel 1 contains two 64-kbit/s intercommunication channels plus Monitor and Command/Indication channels for other IOM-2 devices.
- Channel 2 is used for IOM bus arbitration (access to the TIC bus). Only the Command/ Indication bits are used in channel 2.

The IOM-2 signals are:

DIN, DOUT	768 kbit/s
DCL	1536 kHz output
FSC	8 kHz output

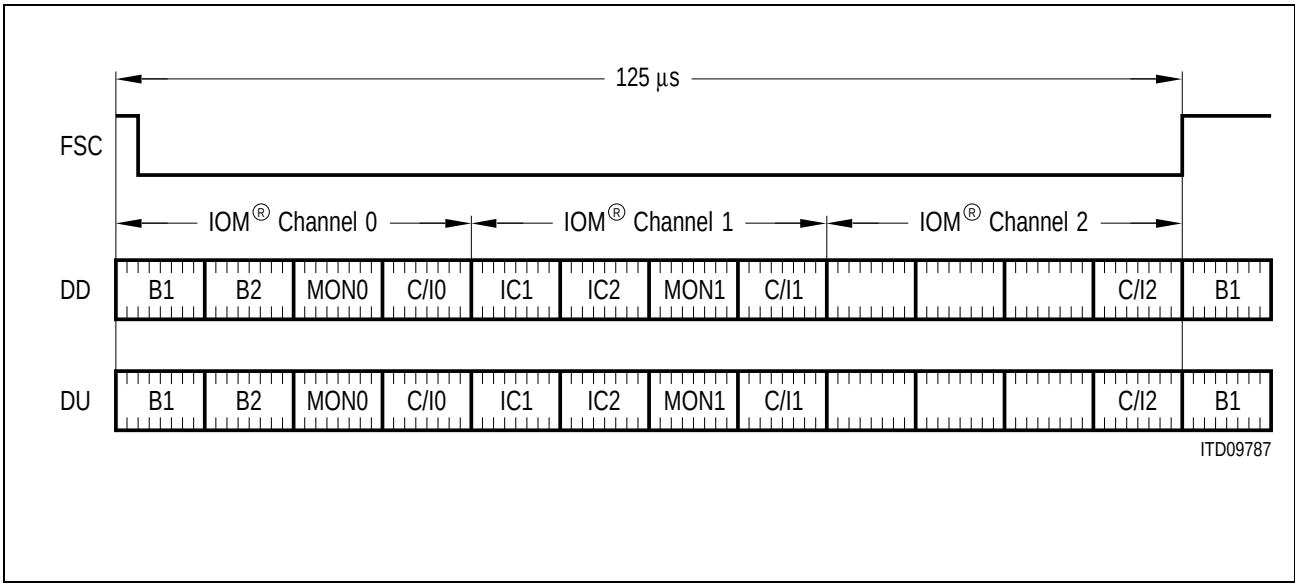


Figure 13 Definition of the IOM®-2 Frame in TE Mode

– **C/I0 in IOM®-2 Channel 0:**

DU / DD	D	D	C/I4	C/I3	C/I2	C/I1	MR	MX

D: two bits for the 16 kbit/s D-channel

C/I: The four command/indication (C/I) bits are used for control of the U-transceiver (activation/deactivation and additional control functions).

MR, **MX:** two bits MR and MX for the handshake in the Monitor channel 0

– **C/I1 in IOM®-2 Channel 1:**

DU / DD	C/I6	C/I5	C/I4	C/I3	C/I2	C/I1	MR	MX

C/I1 to C/I6 are used for control of a transceiver or an other device in IOM-2 channel 1 (activation/deactivation and additional control functions).

MR, **MX:** two bits MR and MX for handshake in the Monitor channel 1

– **C/I2 in IOM®-2 Channel 2:**

DU	1	1	BAC	TBA2	TBA1	TBA0	1	1
DD	E	E	S/G	A/B	1	1	1	1

E: D-echo bits

BAC-bit (Bus ACcessed). When the TIC bus is occupied the BAC-bit is low.

S/G-bit (Stop/Go), available to a connected HDLC controller to determine if it can access the D-channel (S/G = 1: stop, S/G = 0: go).

A/B-bit (available/blocked), supplementary bit for D-channel control. (A/B = 1: D-channel available, A/B = 0: D-channel blocked).

TBA0-2: TIC Bus Address

2.3.1.2 NT Mode Structure

In NT mode the IEC-Q TE provides a data clock DCL with a frequency of 512 kHz. As a consequence the IOM-2 interface provides only one channel with a nominal data rate of 256 kbit/s.

- Channel 0 contains 144 kbit/s (for 2B+D) plus Monitor and Command/Indication channels.

The IOM-2 signals are:

DIN, DOUT 256 kbit/s

DCL 512 kHz output

FSC 8 kHz output

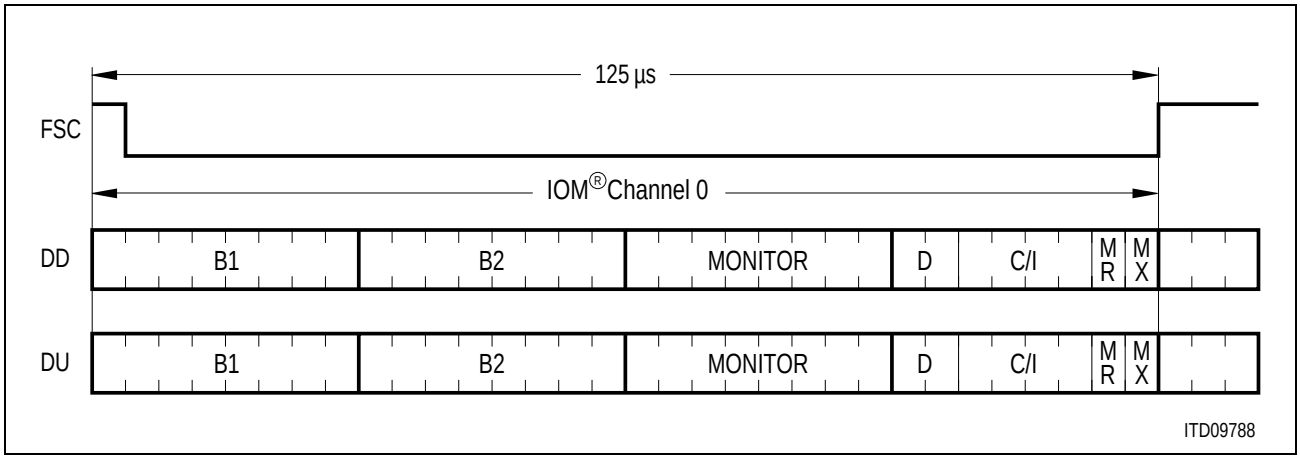


Figure 14 Definition of the IOM®-2 Frame in NT Mode

2.3.2 IOM®-2 Command / Indication Channels

The Command/Indication channels carry real-time control and status information over the IOM-2 interface.

C/I Channel 0

C/I channel 0 (C/I0) is available in both operational modes (NT and TE mode). The channel consists of four bits in each direction. Activation and deactivation of the U-transceiver is always controlled via the C/I0 channel. The C/I codes going to the U-transceiver are called “commands”, those originating from it are referred to as “indications”. The C/I codes of the U-transceiver are listed and explained in chapter 2.5.8 on page 74.

In **stand-alone mode** the C/I0 channel is controlled by an external device, e.g. the ICC, 3PAC, IPAC or ISAR.

In **µP mode** the C/I0 channel can either be controlled by an external device or via the microprocessor interface. For a description on how to access the C/I0 channel via the µP-interface please refer to chapter 2.6.3 on page 83.

C/I Channel 1

C/I channel 1 (C/I1) is only available in TE mode (DCL = 1.536 MHz). The channel consists of six bits in each direction.

In **stand-alone mode** the C/I1 channel is ignored by the U-transceiver.

In **µP mode** it can be accessed via registers CIWI/U and CIRI/U (page 83).

2.3.3 IOM®-2 Monitor Channel

The Monitor channel protocol is a handshake protocol used for programming and monitoring devices in Monitor channel "0" or "1". These can include the on-chip U-transceiver of the IEC-Q TE as well as external devices connected to the IOM-2 interface.

The Monitor channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure. For example: data is placed onto the Monitor channel and the MX bit is activated. This data will be transmitted repeatedly once per 8-kHz frame until the transfer is acknowledged via the MR bit.

Monitor Channel 0

Monitor channel 0 is available in both operational modes (NT and TE mode). The U-transceiver is always controlled and monitored via Monitor channel 0. The Monitor channel commands and indications of the U-transceiver are listed and explained on page 51-61.

In **stand-alone mode** the Monitor channel is controlled by an external device, e.g. the ICC, 3PAC, IPAC or ISAR.

In **µP mode** the Monitor channel can either be controlled by an external device or via the microprocessor interface. For a description on how to access the Monitor 0 channel via the µP-interface please refer to chapter 2.6.4 on page 84.

Monitor Channel 1

Monitor channel 1 is only available in TE mode (DCL = 1.536 MHz). The channel consists of six bits in each direction.

In **stand-alone mode** the Monitor 1 channel is ignored by the U-transceiver.

In **µP mode** it can be accessed via the microprocessor interface (page 83) to control an external device (e.g. ARCOFI).

Monitor Procedure 'Timeout'

The U-transceiver offers an automatic reset (Monitor procedure "Timeout") for the Monitor routine. This reset function transfers the Monitor channel into the idle state (MR and MX set to high) by issuing "EOM" (End of Message) after a timer has elapsed. As an effect, unacknowledged Monitor messages sent by the U-transceiver are taken away from the Monitor channel.

The U-transceiver checks for unacknowledged Monitor messages every 5 ms. In case the timer expires "EOM" will be issued. The U-transceiver does not repeat the message, hence it will be lost.

In slow applications e.g. testing or evalution platforms this internal reset function may be disabled by setting

– Pin MTO in stand-alone mode
– Bit ADF2:MTO in µP mode.

If Monitor Timeout is disabled, no restrictions regarding the time for completing a Monitor transfer exists.

2.3.4 Activation/Deactivation of IOM®-2 Clocks

The IOM-2 clocks may be switched off if the U-transceiver is in state 'Deactivated'. This reduces power consumption to a minimum. In this deactivated state the clock lines are low and the data lines are high. The power-down condition within the 'Deactivated' state will only be entered if no Monitor messages are pending on IOM-2.

For information on how to keep the IOM-2 clocks active in all states please refer to the application note 'Providing Clocks in Deactivated State' of 09.97.

The **deactivation procedure** is shown in **figure 15**. After detecting the code DI (Deactivation Indication) the U-transceiver responds by transmitting DC (Deactivation Confirmation) during subsequent frames and stops the timing signals after the fourth frame.

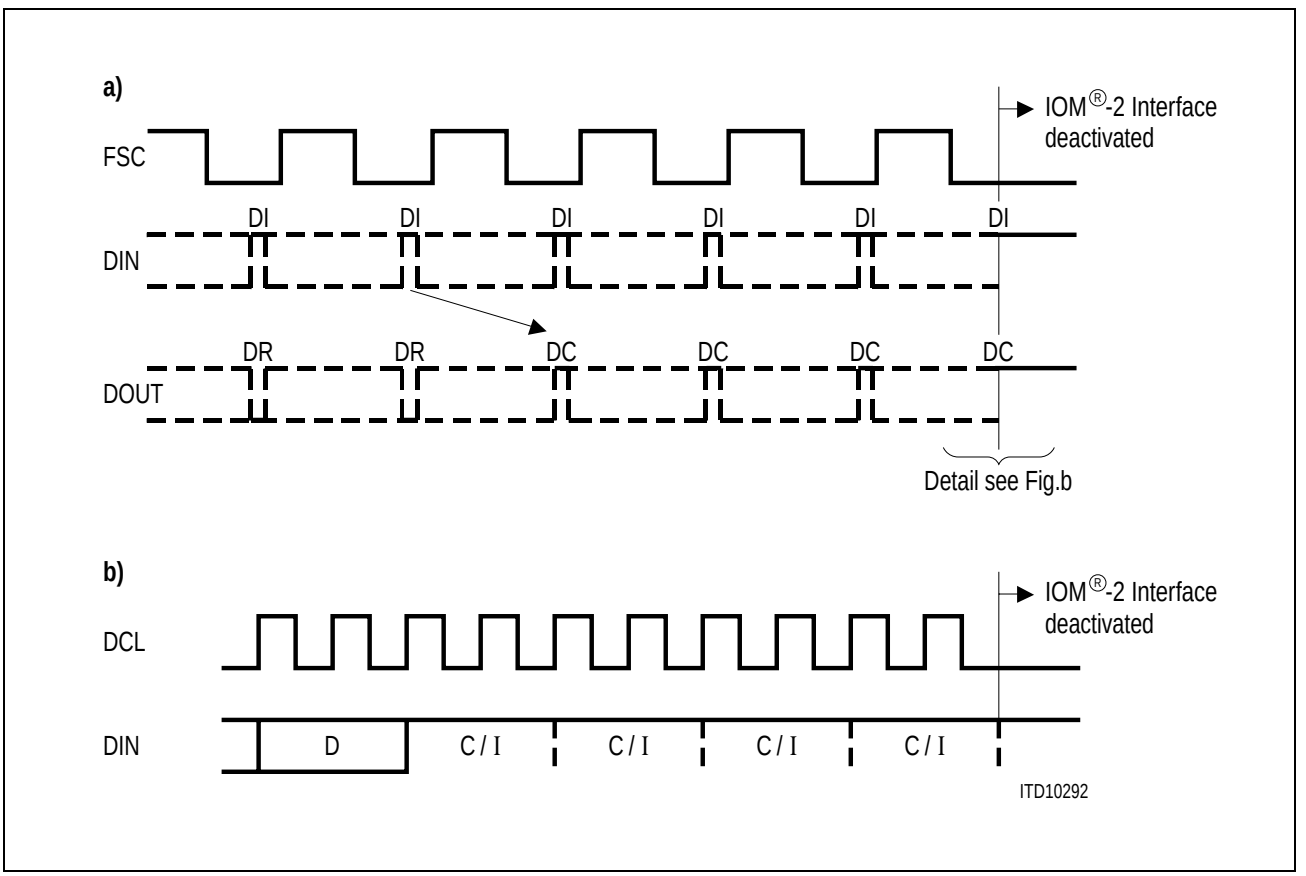


Figure 15 Deactivation of the IOM®-2 Clocks

The IOM-2 clocks are **activated** automatically when the DIN line is pulled low or a line activation is detected on the U-interface. If a PSB 2186 (ISAC-S TE) or PEB 2070 (ICC) is connected to the IEC-Q TE via IOM-2, the DIN line of the IEC-Q TE is pulled low by

setting the SPU bit of the ISAC-S TE or ICC to ’1’. Otherwise, the DU line has to be pulled to low via an I/O port of the microcontroller

DCL is activated such that its first rising edge occurs with the beginning of the bit following the C/I0 channel. After the clocks have been enabled this is indicated by the PU code in the C/I0 channel.

2.3.5 Superframe Marker

The start of a new superframe on the U-interface may be indicated with a FSC high-phase lasting for one single DCL-period. A FSC high-phase of two DCL-periods is transmitted for all other IOM-2 frame starts.

The superframe marker is disabled if pin/bit MS2 = 0.

2.3.6 IOM®-2 Output Driver Selection

In µP mode the output type of the IOM dataline DOUT is selectable via bit ADF2:DOD. In stand-alone mode it is configured via pin DOD. Bit/pin DOD set to 0 selects tristate (reset value) and DOD set to 1 selects open drain outputs.

In the "open drain" mode pull-up resistors (1 kΩ – 5 kΩ) are required on DOUT. FSC and DCL always are push pull.

2.4 Microprocessor Interface

The parallel/serial microprocessor interface can be selected to be either of the

1. **Siemens/Intel non-multiplexed** bus type with control signals **$\overline{CS}$, $\overline{WR}$, $\overline{RD}$**
2. **Motorola** type with control signals **$\overline{CS}$, R/$\overline{W}$, $\overline{DS}$**
3. **Siemens/Intel multiplexed** address/data bus type with control signals **$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE**
4. **Serial mode** using control signals **CDIN, CDOUT, CCLK and $\overline{CS}$**.

The selection is performed via pins ALE/CCLK and SMODE as follows:

Table 5 Microprocessor Interface Modes

	ALE	SMODE
Siemens/Intel non-Mux	0	x
Motorola	1	x
Siemens/Intel Mux	edge	0
Serial	edge	1

The occurrence of an edge on ALE/CCLK, either positive or negative, at any time during the operation immediately selects interface type 3 or 4. A return to one of the other interface types is possible only if a hardware reset is issued.

2.4.1 Microprocessor Clock Output

The microprocessor clock is provided in µP mode on the MCLK-output. Four clock rates are provided by a programmable prescaler. These are 7.68 MHz, 3.84 MHz, 1.92 MHz and 0.96 MHz. Switching between the clock rates is realized without spikes. The oscillator remains active all the time. The clock is synchronized to the 15.36 MHz clock at the XIN pin.

2.4.2 Watchdog Timer

The watchdog is enabled by setting the SWST:WT bit to “1”. The value of SWST:WT after hardware reset (pin $\overline{RES}$ low and pin TSP low) is "0".

After the microcontroller has enabled the watchdog timer it has to write the bit patterns “10” and “01” in ADF:WTC1 and ADF:WTC2 within a period of 132 ms. If it fails to do so, a reset signal of 5 ms at pin $\overline{RST}$ is generated. The clock at pin MCLK remains active during this reset.

2.5 U-Transceiver

The U-interface establishes the direct link between the exchange and the terminal side over two copper wires. Transmission over the U-interface is performed at a rate of 80 kBaud. The code used is reducing two binary informations to one quaternary symbol (2B1Q) resulting in a total of 160 kbit/s to be transmitted. 144 kbit/s are user data (2B + D), 16 kbit/s are used for maintenance and synchronization information.

The IEC-Q TE uses two differential outputs (AOUT, BOUT) and two differential inputs (AIN, BIN) for transmission and reception. These differential signals are coupled via a hybrid and a transformer to the two-wire U-interface.

Figure 16 shows a block diagram of the U-transceiver which can be subdivided in three main blocks:

SIU System Interface Unit
REC Receiver
LIU Line Interface Unit

The System Interface Unit (SIU) provides the connection of the U- and the IOM-interfaces. After scrambling/descrambling and rate adaptation the data channels (2B + D) are transferred to the appropriate frame. Complete activation and deactivation procedures are implemented, which are controlled by activation and deactivation indications from U- or IOM-interfaces. State transition of the procedures depend on the actual status of the receiver (adaptation and synchronization) and timing functions to watch fault conditions. Two different modes can be selected for maintenance functions: In the auto-mode all EOC-procedure handling and executing as specified by ANSI is performed. In the transparent mode all bits are transferred transparently to the IOM-2 interface without any internal processing.

The Receiver block (REC) performs the filter algorithmic functions using digital signal processing techniques. Modules for echo cancellation, pre- and post-equalization, phase adaptation and frame detection are implemented in a modular multi-processor concept.

The Line Interface Unit (LIU) contains the crystal oscillator and all of the analog functions, such as the A/D-converter and the awake unit in the receive path, the pulse-shaping D/A-converter, and the line driver in the transmit path.

Note: Due to the integrated microprocessor interface the IEC-Q TE V5.2 has a few µs more delay from IOM-2 to the U-interface than the IEC-Q V4.4. This may be relevant in very delay sensitive appplications like Radio in the Loop (RITL) and Wireless PBXs.

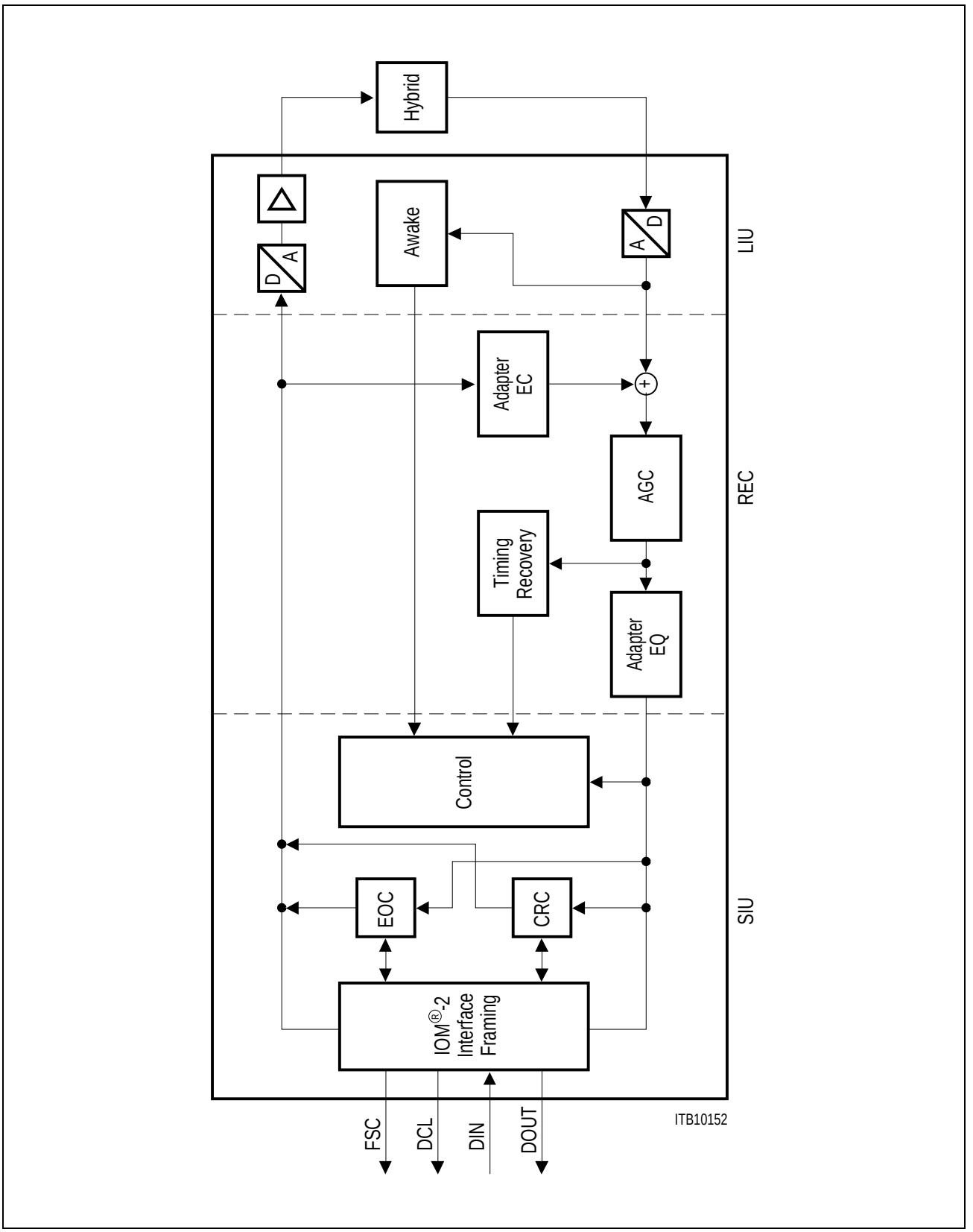


Figure 16 U-Transceiver Block Diagram

2.5.1 U-Frame Structure

Each basic frame consists of 18 bits for the (inverted) synchronization word; 6 overheads bits are allocated for system functions, and 216 bits transfer the userdata of 2B + D-channel (i.e. userdata of 12 IOM-frames is packed into one basic U-frame).

Data is grouped together into U-superframes of 12 ms. The beginning of a new superframe is marked with an inverted synchronization word (ISW). Each superframe consists of eight basic frames (1.5 ms) which begin with a standard synchronization word (SW) and contain 222 bits of information (**table 6**).

Table 6 U-Frame Structure

		Framing	2B + D	Overhead Bits (M1 – M6)					
	Quat Positions	1 – 9	10 – 117	118	118	119	119	120	120
	Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B + D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B + D	EOCa1	EOCa2	EOCa3	ACT/ ACT	1	1
	2	SW	2B + D	EOC d/m	EOCi1	EOCi2	DEA / PS1	1	FEBE
	3	SW	2B + D	EOCi3	EOCi4	EOCi5	1/ PS2	CRC1	CRC2
	4	SW	2B + D	EOCi6	EOCi7	EOCi8	1/ NTM	CRC3	CRC4
	5	SW	2B + D	EOCa1	EOCa2	EOCa3	1/ CSO	CRC5	CRC6
	6	SW	2B + D	EOC d/m	EOCi1	EOCi2	1	CRC7	CRC8
	7	SW	2B + D	EOCi3	EOCi4	EOCi5	UOA / SAI	CRC9	CRC10
	8	SW	2B + D	EOCi6	EOCi7	EOCi8	AIB / NIB	CRC11	CRC12
2,3…									
						LT- to NT dir. >	/	< NT- to LT dir.	

– ISW Inverted Synchronization Word (quad): – 3 – 3 + 3 + 3 + 3 – 3 + 3 – 3 – 3
– SW Synchronization Word (quad): + 3 + 3 – 3 – 3 – 3 + 3 – 3 + 3 + 3
– CRC Cyclic Redundancy Check
– EOC Embedded Operation Channel

a = address bit
d/m = data / message bit
i = information (data / message)

– ACT Activation bit — ACT = (1) –> Layer 2 ready for communication
– DEA Deactivation bit — DEA = (0) –> LT informs NT that it will turn off
– CSO Cold Start Only — CSO = (1) –> NT-activation with cold start only
– UOA U-Only Activation — UOA = (0) –> U-only activated
– SAI S-Activity Indicator — SAI = (0) –> S-interface is deactivated
– FEBE Far-end Block Error — FEBE = (0) –> Far-end block error occurred
– PS1 Power Status Primary Source — PS1 = (1) –> Primary power supply ok
– PS2 Power Status Secondary Source — PS2 = (1) –> Secondary power supply ok
– NTM NT-Test Mode — NTM = (0) –> NT busy in test mode
– AIB Alarm Indication Bit — AIB = (0) –> Interruption (according to ANSI)
– NIB Network Indication Bit — NIB = (1) –> no function (reserved for network use)

2.5.1.1 Cyclic Redundancy Check

The cyclic redundancy check provides a possibility to verify the correct transmission of data. The checksum of a transmitted U-superframe is calculated from the bits in the D-channel, both B-channels, and the M4 bits according to the CRC polynominal

$$G(u) = u^{12} + u^{11} + u^3 + u^2 + u + 1$$

(+ modulo 2 addition)

The check digits (CRC bits CRC1, CRC2, …, CRC12) generated are transmitted at position M5 and M6 in the U-superframe. At the receiving side this value is compared with the value calculated from the received superframe.

In case these values are not identical a CRC-error will be indicated to both sides of the U-interface. It is indicated as a NEBE (Near-end Block Error) on the side where the error is detected and as a FEBE (Far-end Block Error) on the remote side. The FEBE-bit will be placed in the next available U-superframe transmitted to the originator.

Far-end or near-end error indications increment the corresponding block error counters of exchange and terminal side. The IEC-Q TE additionally issues a MON-1 message every time a NEBE or FEBE has occurred (chapter 2.5.3, page 54). The block error counters can be read via MON-8 commands (refer to chapter 2.5.5, page 59).

It is not possible to directly access the CRC-checksum itself. Hence the user cannot read or write the checksum values.

Figure 17 illustrates the CRC-process.

Due to the scrambling algorithm described hereafter, a wrong bit decision in the receiver automatically leads to at least three bit errors. Whether all of these are recorded by a bit error counter depends on whether all faulty bits are part of the monitored channels (2B+D, M4) or not.

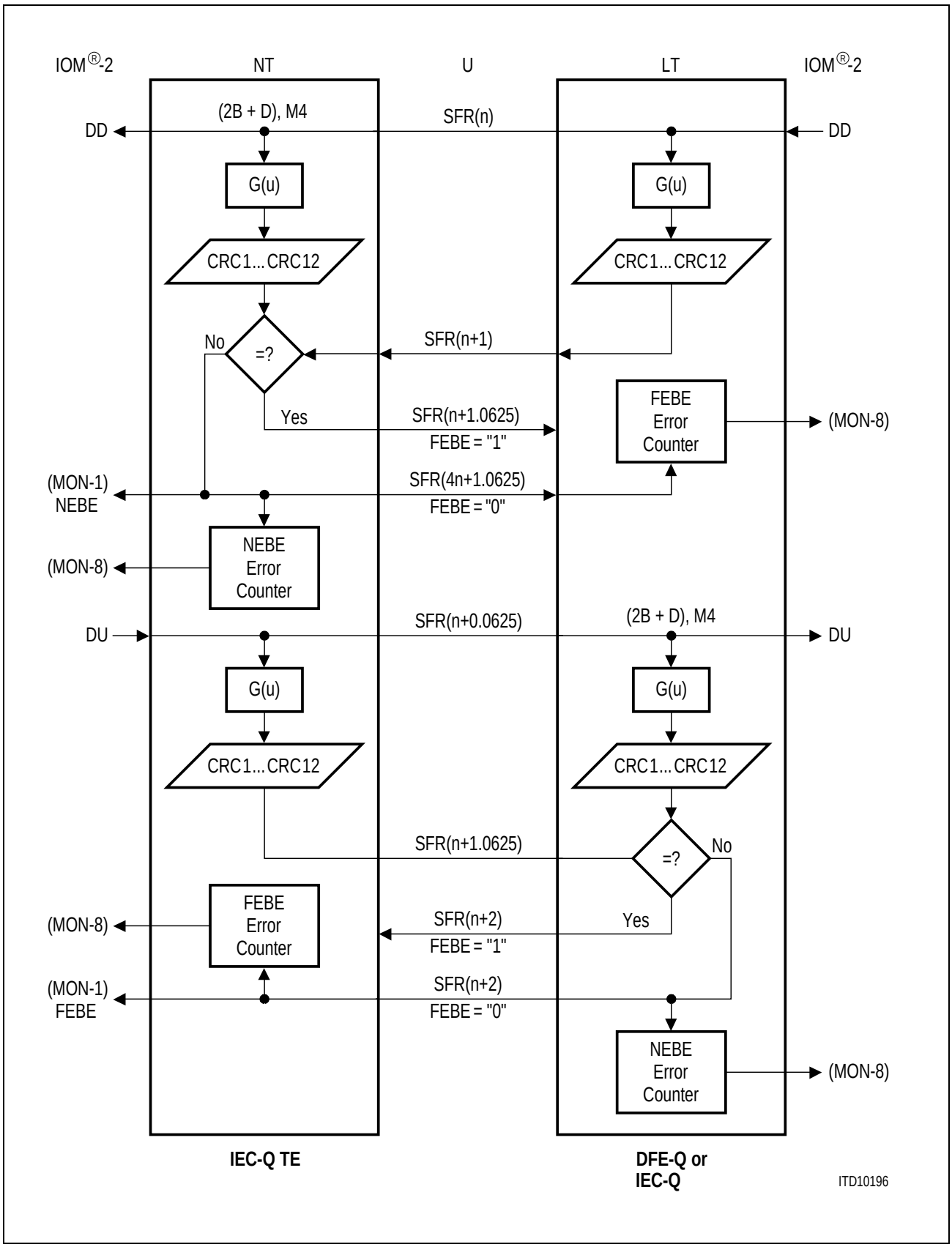


Figure 17 CRC-Process

2.5.1.2 Block Error Counters

The U-transceiver provides internal counters for far-end and near-end block errors. This allows a comfortable surveillance of the transmission quality at the U-interface. In addition, MON-1 messages indicate the occurrence of near-end errors, far-end errors, and the simultaneous occurrence of both errors.

A block error is detected each time when the calculated checksum of the received data does not correspond to the control checksum transmitted in the following superframe. One block error thus indicates that one U-superframe has not been transmitted correctly. No conclusion with respect to the number of bit errors is therefore possible.

The following two sections describe the operation of near and far-end block error counters as well as the commands available to test them.

Near-End and Far-End Block Error Counter

A near-end block error (NEBE) indicates that the error has been detected in the receive direction (i.e. NEBE in the NT after an LT --> NT error). This will be indicated with a MON-1-message NEBE. Each detected NEBE-error increments the 8-bit NEBE-counter. When reaching the maximum count, counting is stopped and the counter value reads (FF_H).

The current value of the NEBE counter is read with the MON-8 command RBEN. The response comprises two bytes: the first byte always indicates that a MON-8 message is replied to (80_H), the second represents the counter value (00_H) … (FF_H). Each read operation resets the counter to (00_H).

A far-end block error identifies errors in transmission direction (i.e. FEBE in the NT = NT => LT-error). FEBE errors are processed in the same manner as NEBE errors. A far-end block error will be indicated with a MON-1 message FEBE. The FEBE counter is read and reset with the MON-8 command RBEF.

In case both, far-end and near-end block errors occur simultaneously, the MON-1 message FNBE will be issued.

Both counters are also reset in all U-transceiver states except ’Synchronized’, ’Wait for Act’, ’Transparent’ and ’Error S/T’.

Testing Block Error Counters

Figure 18 illustrates how the IEC-Q TE supports testing of the LT's block error counters. Transmission errors are simulated with artificially corrupted CRCs. With two commands the cyclic redundancy checksum can be inverted in the downstream and in the upstream direction. A third command offers to invert single FEBE-bits.

With EOC command **NCC** the LT notifies the NT of corrupted CRCs. Again, there are differences in the functional behavior of the NEBE-counter depending on the EOC mode:

Auto-mode	NEBE-detection stopped, no MON-1 NEBE-messages and NEBE-counter disabled
Transparent mode	NEBE-detection enabled, MON-1-message NEBE issued and NEBE-counter enabled

With EOC command **RCC** the LT requests the NT-side to send corrupted CRCs. In EOC auto mode the IEC-Q TE will react automatically with a permanently inverted upstream CRC. In EOC transparent mode this reaction has to be prompted by a MON-8 CCRC command. Note that MON-8 CCRC is not excecuted if it was not preceeded by the EOC command RCC.
There are also differences in the functional behavior of the FEBE-counter depending on the EOC mode:

EOC Auto mode	FEBE-detection stopped, no MON-1 FEBE-messages and FEBE-counter disabled
Transparent mode	FEBE-detection enabled, MON-1-message FEBE issued and FEBE-counter enabled

The EOC command **RTN** disables all previously sent EOC commands. In EOC transparent mode EOC command RTN must be followed by a MON-8 NORM command to become effective.

With the MON-8-command **SFB** it is possible to invert single FEBE-bits. Because this command does not provoke permanent FEBE-bit inversion but sets only one FEBE-bit to (0) per SFB command, it is possible to predict the exact FEBE-counter reading.

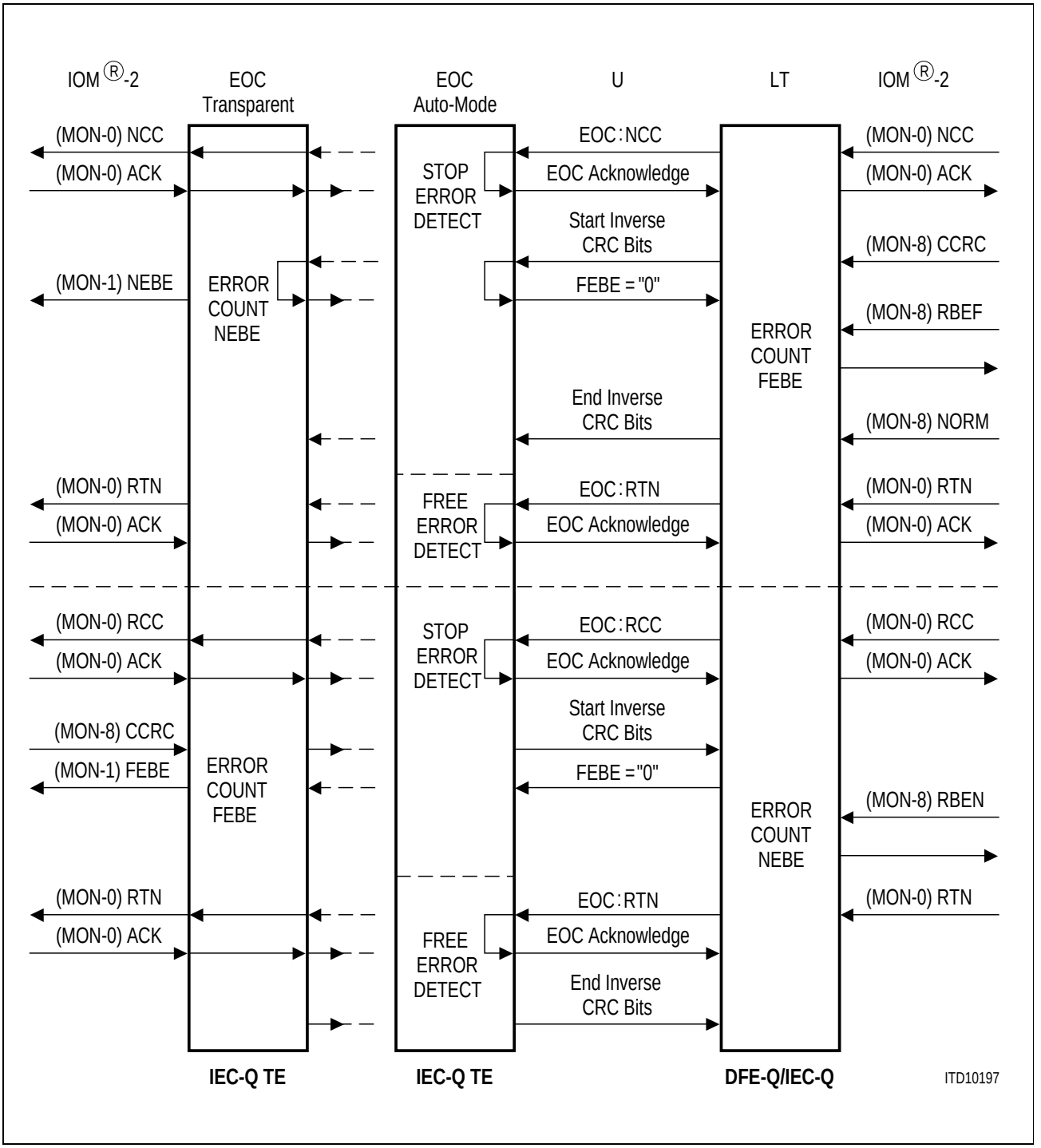


Figure 18 Block Error Counter Test

2.5.1.3 Scrambler / Descrambler

The scrambling algorithm as defined by ANSI T1.601 ensures that no sequences of permanent binary 0s or 1s are transmitted. The algorithms used for scrambling and descrambling are described in **figure 19**. The scrambling/descrambling process is controlled fully by the IEC-Q TE. Hence, no influence can be taken by the user.

Please refer to page 77 for a description of loop 3.

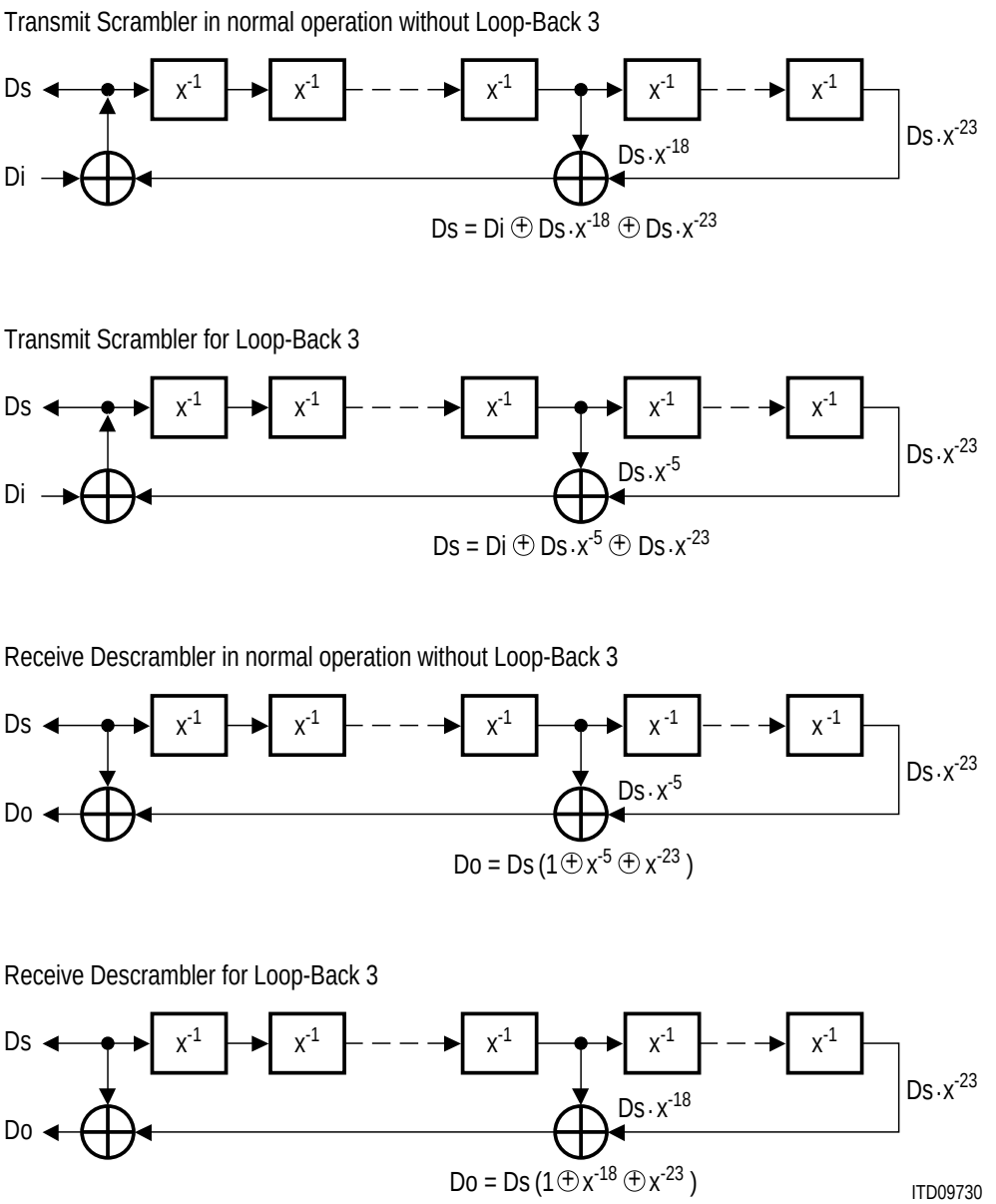


Figure 19 Scrambler / Descrambler Algorithms

2.5.1.4 Embedded Operations Channel (EOC)

EOC-data is inserted into the U-frame at the positions M1, M2 and M3 thereby permitting the transmission of two complete EOC-messages (2 × 12 bits) within one U-superframe.

The EOC contains an address field, a data/message indicator (d/m) and an eight-bit information field.

With the **address field** the destination of the transmitted message/data is defined. Addresses are defined for the NT, 6 repeater stations and broadcasting.

The **data/message indicator** needs to be set to (1) to indicate that the information field contains a message. If set to (0), numerical data is transferred to the NT. Currently no numerical data transfer to or from the NT is required.

From the 256 codes possible in the **information field** 64 are reserved for non-standard applications, 64 are reserved for internal network use and eight are defined by ANSI/ ETSI for diagnostic and loop-back functions. All remaining 120 free codes are available for future standardization.

Table 7 EOC-Codes

EOC						
Address			**d/m**	**Information (hex)**	**Direction**	**Message**	**Function**
a1	**a2**	**a3**	**d/m**	**i1 - i8**			
0	0	0	x			NT	
1	1	1	x			Broadcast	
0 1	0 1	1 0	x			Repeater stations No. 1 – No. 6	
			0			Data	
			1			Message	
			1	50	NT <---- LT	LBBD	Close complete Loop
			1	51	NT <---- LT	LB1	Close Loop B1
			1	52	NT <---- LT	LB2	Close Loop B2
			1	53	NT <---- LT	RCC	Request Corrupt CRC
			1	54	NT <---- LT	NCC	Notify of corrupt CRC
			1	FF	NT <---- LT	RTN	Return to normal
			1	00	NT <---> LT	H	Hold

Table 7 EOC-Codes (cont'd)

EOC					
Address	**d/m**	**Information (hex)**	**Direction**	**Message**	**Function**
a1 a2 a3	**d/m**	**i1 - i8**			
	1	AA	NT ----> LT	UTC	Unable to comply
	1	XX	NT ----> LT	ACK	Acknowledge

2.5.2 EOC-Processor and MON-0

An EOC-processor on the chip is responsible for the correct insertion and extraction of EOC-data on the U-interface. The EOC-processor can be programmed to auto mode (default) or transparent mode via bit EOCA in the UMOD register (**table 20**). Access to the EOC is only possible when a superframe is transmitted. This is the case in the U-transceiver states 'Synchronized', 'Wait for ACT', 'Transparent', 'Error S/T' and 'Pend. Deac. U'. In all other states the EOC-bits on the U-interface are clamped to high.

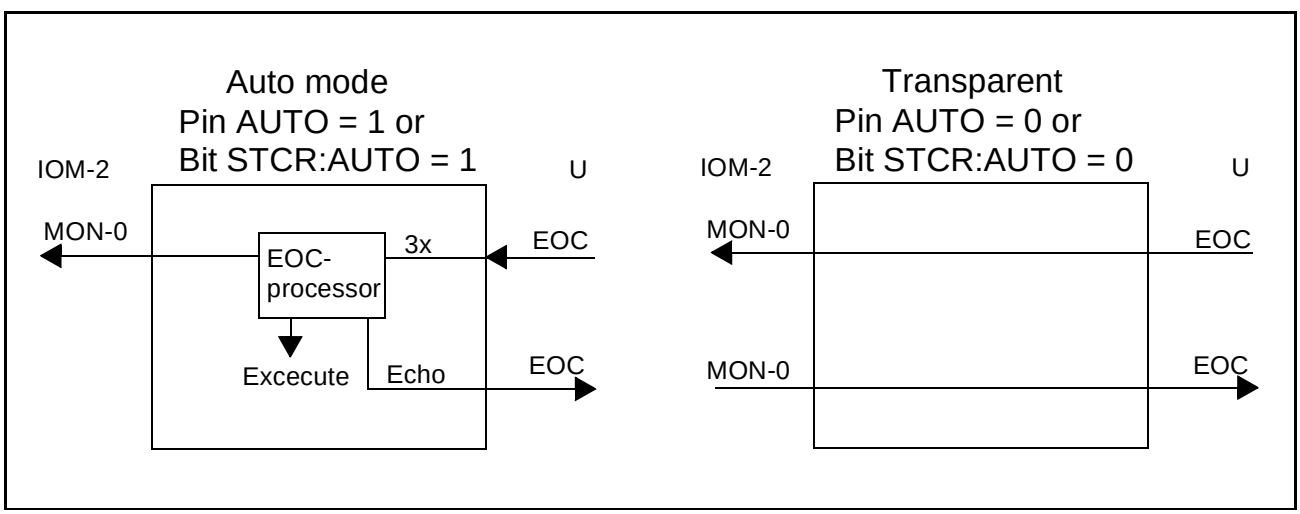


Figure 20 EOC-Processor: Auto Mode, Transparent Mode

The EOC is controlled and monitored via MON-0 commands and messages in the IOM-2 Monitor channel. The structure of a MON-0-message is shown below. The structure is identical in EOC auto and transparent mode.

MON-0 Structure

1. Byte		2. Byte	
0 0 0 0	A A A | X	i1 i2 i3 i4	i5 i6 i7 i8
MON-0	Addr. | d/m	EOC Code	

Addr: Address
- 0 = NT
- 1 … 6 = Repeater
- 7 = Broadcast

d/m: Data/Message
- 0 = Data
- 1 = Message

i1-i8: EOC Code
- 00 … FF_H = coded EOC command/indication

EOC Auto Mode

Acknowledgment: All received EOC-frames are echoed back to the exchange immediately without triple-last-look. If an address other than (000_B) or (111_B) is received, a HOLD message with address 000_B is returned. However, there is an exception: The IEC-Q TE will send a 'UTC' after three consecutive receptions of d/m = (0) or after an undefined command.

Latching: All detected EOC-commands are latched, i.e. they are valid as long as they are not disabled with the EOC 'RTN' command or a deactivation.

Transfer to IOM: With the triple-last-look criteria fulfilled the new EOC-command will be passed to IOM-2 with one single MON-0-message, independently of the address used and the status of the d/m indicator. MON-0-commands from IOM will be ignored.

Execution: The EOC-commands listed in **table 8** will be executed automatically by the PSB 21911 if they were addressed correctly (000_B or 111_B) and the d/m bit was set to message (1). The execution of a command is performed only after the "triple-last-look" criterion is met.

Table 8 Executed EOC Commands in Auto Mode

EOC-code i1 - i8 (Hex)	Direction D	Direction U	Function
50	LBBD		**Close complete loop-back (B1, B2, D).** The U-transceiver does not close the complete loop-back immediately after receipt of this code. Instead it issues the C/I-command AIL (in “Transparent” state) or ARL in the states “Error S/T” and “Synchronized”. This allows the downstream device to close the loop-back if desired (e.g. S-transceiver or microcontroller).
51	LB1		**Closes B1 loop-back** in NT. All B1-channel data will be looped back within the U-transceiver.
52	LB2		**Closes B2 loop-back** in NT. All B2-channel data will be looped back within the U-transceiver.
53	RCC		**Request corrupt CRC.** Upon receipt the IEC-Q TE transmits corrupted (= inverted) CRCs upstream. This allows to test the near end block error counter on the LT-side. The far end block error counter at the NT-side is disabled and NT-error indications (MON-1) are suppressed.
54	NCC		**Notify of corrupt CRC.** Upon receipt of NCC the near end block error counter is disabled and error indications are suppressed. This prevents wrong error counts while corrupted CRCs are sent.
FF	RTN		**Return to normal.** With this command all previously sent EOC-commands will be released. The EOC-processor is reset to its initial state (FF_H).

EOC Transparent Mode

In transparent mode no acknowledgment, no triple-last-look and no execution of the received commands is performed. The received EOC-frame is transmitted directly downstream via a MON-0-message. Thus, a MON-0-message is issued on IOM every 6 ms. Acknowledgment and execution of the received command have to be initiated by the microcontroller. The microcontroller can execute all defined test functions (close/ open loops, send corrupted CRCs) in the NT using MON-8-commands.

In the upstream direction the last incoming EOC-code from the IOM-2-Monitor channel is transmitted to the LT.

2.5.3 Maintenance (MON-1)

This category comprises commands and messages relating to maintenance bits of the U-interface and the self-test according to ANSI T1.601. The commands and messages may be mapped to the S/Q channel of the S/T-interface via the microprocessor. This provides a method to exchange U-interface related information between a terminal on the S-bus and the NT. Thus, the terminal can be informed about transmission errors that occurred on the U-interface (NEBE, FEBE, FNBE) or request the NT to perform a self-test (ST).

MON-1 messages are two bytes long. The first nibble of the second byte contains S/Q-indications, the second nibble contains maintenance bit related commands. The operation of MON-1-messages is identical in auto- and transparent mode.

The following tables give an overview of indications available in the MON-1 category.

MON-1 Structure

1. Byte		2. Byte	
0 0 0 1	0 0 0 0	S S S S	M M M M
MON-1		S/Q-Code	M-bits

S/Q: S/Q-channel – 00 … FF_H = coded S/Q-command indication
M: Maintenance bits – 00 … FF_H = set/reset maintenance bits

The following indications and maintenance bits are defined in MON-1-messages.

Table 9 Mon-1 S/Q-Channel Commands and Indications

S/Q	Direction		Function
SSSS (Bin)	D	U	S/Q-Channel
0 0 0 1		ST	**Self-test request**. This command is issued by the terminal to inquire whether layer 1 is present. No test is performed within the U-transceiver. Upon reception the U-transceiver replies with MON-1 “STP”.
0 0 1 0	STP		**Self-test pass**. Indicates to the terminal that the U-transceiver has received the command “ST” correctly.
0 1 0 0	FEBE		**Far-end block error**. Via the FEBE bit set to (0) on the U-interface it is indicated to the NT that transmission errors occurred in the direction NT –> LT or NT –> LT-RP.

Table 9 Mon-1 S/Q-Channel Commands and Indications (cont'd)

S/Q	Direction		Function
SSSS (Bin)	D	U	S/Q-Channel
1 0 0 0	NEBE		**Near-end block error**. Transmission errors occurred in the direction LT –> NT.
1 1 0 0	FNBE		**Far- and near-end block error**. Transmission errors were observed in LT –> NT direction.
1 1 1 1		NORM	**Normal**. Return to normal (idle) state. This command initiates no U-transceiver action.

Table 10 Mon-1 M-Bit Commands

M-Bit	Direction		Function
MMMM (Bin)	D	U	Maintenance Bits
1 x x 0		NTM	**NT-test mode**. After reception of this command the NTM-bit of the U-interface is set active (= 0) in order to inform the exchange that the NT is involved in testing and not available for transparent transmission. This message needs to be sent out by the downstream device if the terminal requests tests which prevent transparent transmission (e.g. loops B1, B2, D).
1 1 1 1		NORM	**Normal** sets back the NTM-bit to 1. No other action taken.

2.5.4 Overhead Bits (MON-2)

MON-2-indications are used to transfer all overhead bits (M4, M5, M6) except those representing EOC- and CRC-bits. Starting with the ACT-bit, the order is identical to the position of the bits at the U-interface.

Table 11 MON-2 Structure

1. Byte		2. Byte
0 0 1 0	D11 D10 D9 D8	D7 D6 D5 D4 D3 D2 D1 D0
MON-2	Overhead Bits	Overhead Bits

D0 … 11: Overhead bits

These bit positions in the MON-2-message correspond to the following overhead bits:

Table 12 Control of Overhead Bits

Position MON-2/U	Upstream (Write)		Downstream (Read)	
	Bit	Control	Bit	Control
D11/M41	ACT	U-transc.	ACT	network
D10/M51	1	MON-2	1	network
D9/M61	1	MON-2	1	network
D8/M42	PS1	Pin PS1	DEA	network
D7/M52	1	MON-2	1	network
D6/M62	FEBE	U-transc./ MON-8	FEBE	network
D5/M43	PS2	Pin PS2	1	network
D4/M44	NTM	MON-1	1	network
D3/M45	CSO	U-transc.	1	network
D2/M46	1	MON-2	1	network
D1/M47	SAI	U-transc./ MON-2	UOA	network
D0/M48	1	MON-2	1	network

Control via Network

– All Downstream bits.

Automatic control via U-transceiver

– ACT (Activation bit) = (1) –> Layer 2 ready for communication
– SAI (S Activity Indicator) = (0) –> S-interface is deactivated;
can be controlled via MON-2 after MON-8 'PACE'.
– FEBE (Far-end Block Error) = (0) –> Far-end block error occurred
can additionally be controlled via MON-8-'SFB'.
– CSO (Cold Start Only). = (0) –> U-transceiver is warm start capable;

Control via Pins

– PS1 (Power Prim. Source) = (1) –> PS1 = (1) –> Prim. supply ok
– PS2 (Power Sec. Source) = (1) –> PS2 = (1) –> Sec. supply ok

Control via MON-2

– only the undefined bits marked with binary '1'
– SAI (S Activity Indicator) = (0) –> S-interface is deactivated;
can be controlled via MON-2 after MON-8 'PACE'.

Control via other MON-Commands

– NTM (NT-Test Mode) = (0) –> NT busy in test mode (MON-1)
– FEBE (Far-end Block Error);MON-8 message 'SFB' sets a single FEBE bit to '0'

For details about the meaning of the overhead bits please refer to ETSI ETR 080 and ANSI T1.601.

Overhead Bits Upstream Transmission

– The upstream overhead bits are controlled by means of the U-transceiver due to its state, pins, MON-2 commands and other MON commands.
– Only the undefined bits market with binary "1" may be controlled directly by a MON-2-message.
– All overhead bits are set to binary "1" when leaving a power-down state.

Overhead Bits Downstream Reception

– In the receive direction, the overhead bits of the last two U-interface superframes are compared and a MON-2-message defining all 12 bits is issued if a difference between both was found on at least one single bit other than the "FEBE" bit. Therefore, a MON-2-message is sent not more often than once per superframe (12 ms interval).

– In order to notify the controller of the initial system status, one MON-2-message is issued immediately after reaching the “Synchronized” state in NTmode.
– The U-transceiver will not issue MON-2-messages while CRC-violations are detected. Because the CRC-checksum is transmitted one superframe later, a maximum of one corrupted MON-2-indication can be issued. In this case a MON-2-message indicating the correct system status will be issued after the transmitted CRC-checksum is again identical to the calculated checksum.

2.5.5 Local Functions (MON-8)

Local functions are controlled via MON-8-commands. The following tables give an overview of structure and features of commands belonging to this category.

Format of MON-8-Messages

1. Byte		2. Byte
1 0 0 0	r | 0 0 0	D7 D6 D5 D4 D3 D2 D1 D0
MON-8	Register | Addr.	Local Command (Message/Data)

r: Register address – 0 = local function register
– 1 = internal register

D0…7 Local command – 00 … FF_H = local function code
– 00 … FF_H = internal register address

The following local commands are defined. If a response is expected, it will comprise 4 bytes (2 messages a 2 bytes) if the value of an internal coefficient is returned, and 2 bytes in all other cases.
In a two-byte response the first byte will indicate that a MON-8 answer is transmitted, the second byte contains the requested information. This procedure is repeated for a four-byte transfer (MON-8, Info 1, MON-8, Info 2).

Table 13 Mon-8 Local Function Commands

r	Code	Direction		Function
	D7-D0 (Bin)	D	U	Local Commands
0	1011 1110		PACE	**Partial Activation Control External**. With the PACE-command issued, the U-transceiver will ignore the actual status of the received UOA-bit and behave as if the UOA-bit was set to (1). After issuing PACE the UOA/SAI-bits can be controlled by MON-2-commands.
0	1011 1111		PACA	**Partial Activation Control Automatic**. PACA enables the device to interpret the UOA-bit and control the SAI-bit automatically. Partial activation and deactivation is therefore possible. The U-transceiver is automatically reset into this mode in the states “Test”, “Receive Reset” and “Tear Down”.

Table 13 Mon-8 Local Function Commands (cont'd)

r	Code	Direction		Function
	D7-D0 (Bin)	D	U	Local Commands
0	1111 0000		CCRC	**Corrupt CRC**. This command is only recognized if the device is set to EOC transparent mode. The microcontroller should issue the command in case the MON-0-command RCC was received before. CCRC then causes corrupt CRCs to be transmitted upstream.
0	1111 0100		LB1	**Loop-back B1**. The command is only recognized in EOC transparent mode. The microcontroller should issue the command in case the MON-0-command LB1 was received before. LB1 loops back the B1 channel. The loop is closed near the IOM-2 interface.
0	1111 0010		LB2	**Loop-back B2**. The command is only recognized in EOC transparent mode. The microcontroller should issue the command in case the MON-0-command LB2 was received before. LB2 loops back the B2 channel. The loop is closed near the IOM-2 interface.
0	1111 0001		LBBD	**Loop-back B1 + B2 + D**. The command is used in the EOC transparent and EOC auto-mode. LBBD loops back both B-channels and the D-channel. The loops are closed near the IOM-2 interface. In transparent mode the loop is closed unconditionally. In auto-mode the loop is closed only if LBBD was received in the EOC-channel before.
0	1111 1111		NORM	**Return to Normal**. The NORM-command resets the device into its default mode, i.e. loops are resolved and corrupted CRCs are stopped. It is only used in transparent mode.
0	1111 1011		RBEN	**Read Near-End Block Error Counter**. The value of the near-end block error counter is returned and the counter is reset to zero. The maximum value is FF_H.

Table 13 Mon-8 Local Function Commands (cont'd)

r	Code	Direction		Function
	D7-D0 (Bin)	D	U	Local Commands
0	1111 1010		RBEF	**Read Far-End Block Error Counter**. The value of the far-end block error counter is returned and the counter is reset to zero. The maximum value is FF_H.
0	r r r r r r r r	ABEC		**Answer Block Error Counter**. The value of the requested block error counter is returned (8 bit).
0	0000 0000		RID	**Read Identification**. Request for device identification.
0	r r r r r r r r	AID		**Answer identification**. Reply to an RID is '03_H'.
0	1111 1001		SFB	**Set FEBE Bit** to 0
1	cccc cccc		RCOEF	**Read Coeffiecient**
1 1	bbbb bbbb bbbb bbbb	DCOEF		**Data Coefficients**, 2 bytes. Data bits D0 … D 7, 1. byte Data bits D8 … D15, 2. byte

Notes: b … b internal coefficient value
c … c internal coefficient address
r … r result from block error counter

2.5.6 State Machine Notation Rules

The state machine includes all information necessary for the user to understand and predict the activation/deactivation status of the U-transceiver. The information contained in a state bubble is:

State name, **U-signal** transmitted, **Single Bits** (Overhead bits) transmitted, **C/I-indication** transmitted on the C/I-channel, **Transition criteria** and **Timers**.

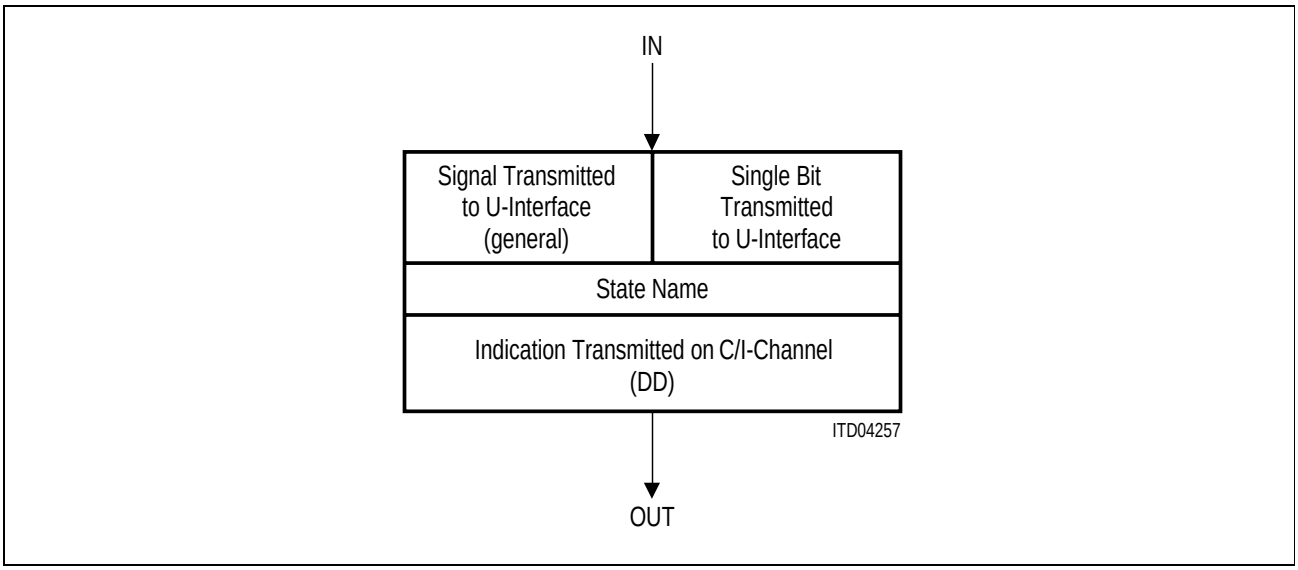


Figure 21 State Diagram Notation U-Transceiver

The following example explains the use of the state diagram by an extract of the NT-state diagram. The state explained is the “EC-Training” state.

Example:

The state may be entered by either of two methods:

–from state “Alerting” after time T11 has expired.
–from state “EC-Training 1” after the C/I command “DI” has been received.

The following informantion is transmitted:

–SN1 is sent on the U-interface.
–No overhead bits are sent
–C/I message “DC” is issued on the IOM-2 interface.

The state is be left at occurrence of one of the following events:

–Leave for state “EQ-Training” after LSEC has been detected.
–Leave for state “EQ-Training” after timer T12 has expired.

Combinations of transition criteria are possible. Logical “AND” is indicated by “&” (TN & DC), logical “OR” is written “or” and for a negation “/” is used. The start of a timer is indicated with “TxS” (“x” being equivalent to the timer number). Timers are always started when entering the new state. The action resulting after a timer has expired is indicated by the path labelled “TxE”.

2.5.7 State Machine

This chapter describes the activation and deactivation behavior of the IEC-Q TE. It applies for both NT and TE mode.

2.5.7.1 Cold and Warm Starts

Two types of start-up procedures are supported by the U-transceiver: cold starts and warm starts.

Cold starts are performed after a reset and require all echo and equalizer coefficients to be recalculated. This procedure typically is completed after 1-7 seconds depending on the line characteristics. Cold starts are recommended for activations where the line characteristics have changed considerably since the last deactivation.

A warm start procedure uses the coefficient set saved during the last deactivation. It is therefore completed much faster (maximum 300 ms). Warm starts are however restricted to activations where the line characteristics do not change significantly between two activations.

Regarding the path in the transition diagram, cold starts have in particular that the U-transceiver has entered the state ’Test’ (e.g. due to a reset) prior to an activation. The activation procedure itself is then identical in both cases. Therefore, the following sections apply to both warm and cold starts.

2.5.7.2 State Diagram

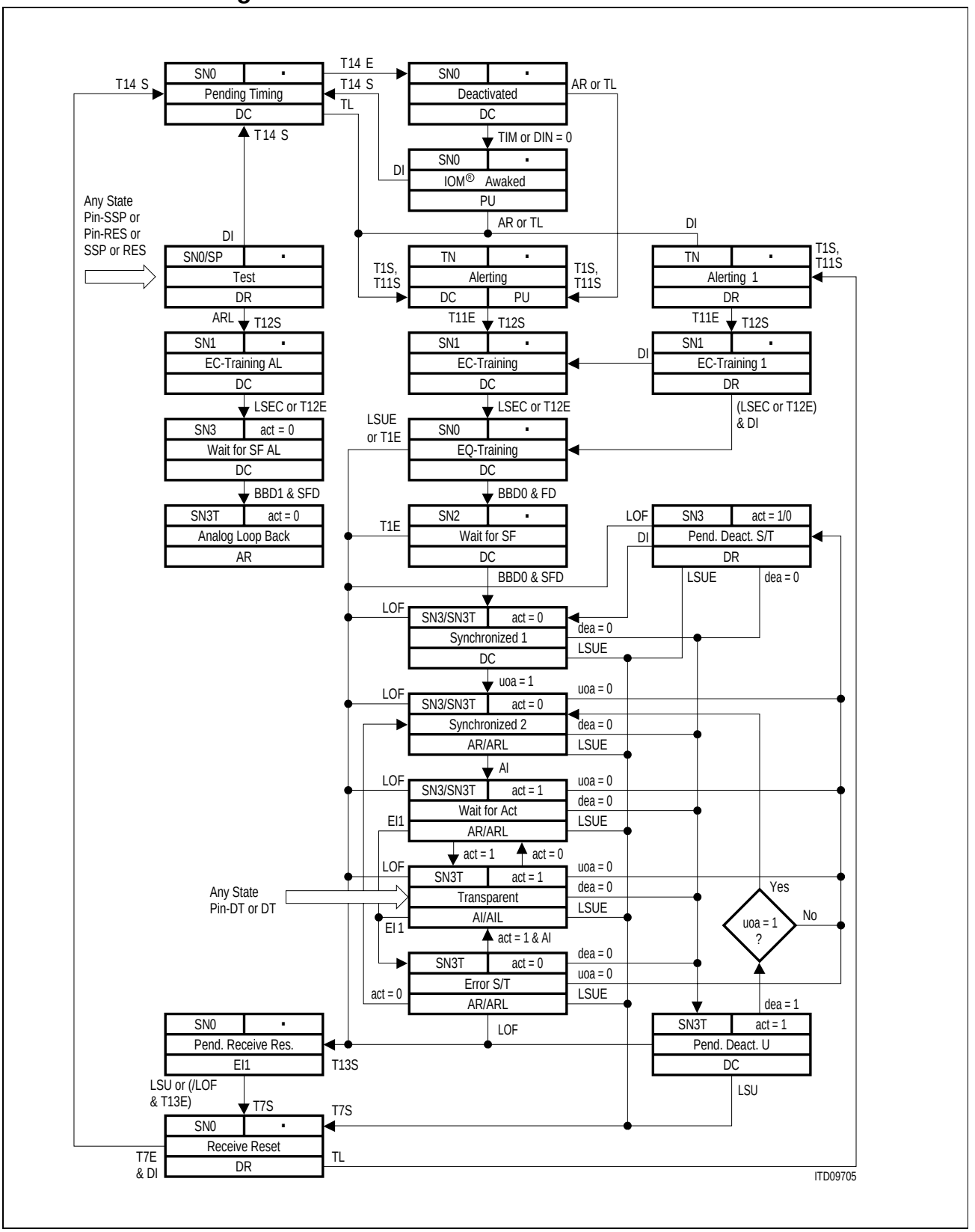


Figure 22 State Transition Diagram

2.5.7.3 Inputs to the U-Transceiver

C/I-Commands

AI Activation Indication
The S-transceiver issues this indication to announce that the S-receiver is synchronized. The U-transceiver informs the LT side by setting the “ACT” bit to “1”.

AR Activation Request
INFO1 has been received by the S-transceiver or the Intelligent NT wants to activate the U-interface. The U-transceiver is requested to start the activation process by sending the wake-up signal TN.

ARL Activation Request Local Loop-back
The U-transceiver is requested to operate an analog loop-back (close to the U-interface) and to begin the start-up sequence by sending SN1 (without starting timer T1). This command may be issued only after the U-transceiver has been reset by making use of the C/I-channel code RES or a hardware reset. This assures that the EC- and EQ-coefficient updating algorithms converge correctly. The ARL-command has to be issued continuously as long as the loop-back is required.

DI Deactivation Indication
This indication is used during a deactivation procedure to inform the U-transceiver that timing signals are needed no longer and that the U-transceiver may enter the deactivated (power-down) state. The DI-indication has to be issued until the U-transceiver has answered with the DC-code.

DIN = 0 Binary “0” polarity on DIN
This asynchronous signal requests the U-transceiver to provide IOM clocks. Hereafter, binary “0s” in the C/I-channel (code TIM “0000” or any other code different from DI “1111”) keep the IOM-2 interface active.

DT Data Through
This unconditional command is used for test purposes only and forces the U-transceiver into a state equivalent to the “Transparent” state. The far-end transceiver is assumed to be in the same condition.

EI1 Error Indication 1
The S-transceiver indicates an error condition on its receive side (loss of frame alignment or loss of incoming signal). The U-transceiver informs the LT-side by setting the ACT-bit to “0” thus indicating that transparency has been lost.

RES Reset
Unconditional command which resets the whole chip; especially the EC- and EQ-coefficients are set to zero.

SSP Send Single Pulses
Unconditional command which requests the transmission of single pulses on the U-interface. The pulses are issued at 1.5 ms intervals and have a duration of 12.5 µs.
The chip is in the “Test” state, the receiver will not be reset.

TIM Timing
In the NT-mode the U-transceiver is requested to continue providing timing signals and not to leave the “Power-up” state.

Pins

Pin-Res Pin-Reset
Corresponds to a low-level at pin $\overline{\text{RES}}$ or a power-on reset. The function of this pin is the same as of the C/I-code RES. C/I-message DR will be issued. The duration of the reset pulse must be longer than 10 ns.

Pin-SSP Pin-Send Single Pulses
Corresponds to a high-level at pin TSP in stand-alone mode. The function of this pin is the same as of the C/I-code SSP. C/I-message DR will be issued. The high-level must be applied continuously for single pulses.

Pin-DT Pin-Data Through
This function is activated when both pins $\overline{\text{RES}}$ and TSP are active in stand-alone mode ($\overline{\text{RES}}$ = ’0’ and TSP = ’1’). The function of this pin is the same as of the C/I-code DT. C/I-message DR will be issued.

U-Interface Events

The signals SLx and TL received on the U-interface are defined in **table 22** on **page 100**

ACT ACT-bit received from LT-side.

- ACT = 1 requests the U-transceiver to transmit transparently in both directions. As transparency in receive direction (U-interface to IOM) is already performed when the receiver is synchronized, the receipt of ACT = 1 establishes transparency in transmit direction (IOM to U-interface), too. In the case of loop-backs, however, transparency in both directions of transmission is established when the receiver is synchronized.
- ACT = 0 indicates that the LT-side has lost transparency.

DEA DEA-bit received from the LT-side

– DEA = 0 informs the U-transceiver that a deactivation procedure has been started by the LT-side.

– DEA = 1 reflects the case when DEA = 0 was detected by faults due to e.g. transmission errors and allows the U-transceiver to recover from this situation (see state 'Pend. Deact. U').

UOA UOA-bit received from network side

– UOA = 0 informs the U-transceiver that only the U-interface is to be activated. The S/T-interface must remain deactivated.

– UOA = 1 enables the S/T-interface to activate.

LOF Loss of Framing on the U-interface

This condition is fulfilled if framing is lost for 576 ms. 576 ms are the upper limit. If the correlation between synchronization word and the input signal is not optimal, LOF may be issued earlier.

LSEC Loss of Signal level behind the Echo Canceler
Internal signal which indicates that the echo canceler has converged.

LSU Loss of Signal level on the U-interface
This signal indicates that a loss of signal level for a duration of 3 ms has been detected on the U-interface. This short response time is relevant in all cases where the NT waits for a response (no signal level) from the LT-side, i.e. after a deactivation has been announced (receipt of DEA = 0), after the NT has lost framing, and after timer T1 has elapsed.

LSUE Loss of Signal level on the U-interface
After a loss of signal has been noticed, a 588 ms timer is started. When it has elapsed, the LSUE-criterion is fulfilled. This long response time (see also LSU) is valid in all cases where the NT is not prepared to lose signal level i.e. the LT has stopped transmission because of loss of framing, an unsuccessful activation, or the transmission line is interrupted.
Note that 588 ms represent a minimum value; the actual loss of signal might have occurred earlier, e.g. when a long loop is cut at the NT-side and the echo coefficients need to be readjusted to the new parameters. Only after the adjusted coefficients cancel the echo completely, the loss of signal is detected and the timer can be started (if the long loop is cut at the remote end, the coefficients are still correct and loss of signal will be detected immediately).

SFD Superframe (ISW) Detected on U-interface

FD Frame (SW) Detected on U-interface

TL Wake-up signal received from the LT
The U-transceiver is requested to start an activation procedure. The TL-criterion is fulfilled when 12 consecutive periods of the 10-kHz wake-up tone were detected.
When in the “Pending Timing” state and automatic activation after reset is selected (NT-AUTO mode), a recognition of TL is assumed every time the “Pending Timing” state has been entered from the “Test” state (caused by C/I code DI). This behavior allows the U-transceiver to initiate one single activation attempt after having been reseted.

BBD0/1 Binary “0s” or “1s” detected in the B- and D-channels
This internal signal indicates that for 6-12 ms, a continuous stream of binary “0s” or “1s” has been detected. It is used as a criterion that the receiver has acquired frame synchronization and both its EC- and EQ-coefficients have converged. BBD0 corresponds to the signal SL2 in the case of normal activation and BBD1 corresponds to the internally received signal SN3 in case of an analog loop back in the NT-mode.

Timers

The start of timers is indicated by TxS, the expiry by TxE. The following **table 14** shows which timers are used by the U-transceiver:

Table 14 Timers

Timer	Duration (ms)	Function	State
T1	15000	Supervisor for start-up	
T7	40	Hold time	Receive reset
T11	9	TN-transmission	Alerting
T12	5500	Supervisor EC-converge	EC-training
T13	15000	Frame synchronization	Pend. receive reset
T14	0.5	Hold time	Pend. timing

2.5.7.4 Outputs of the U-Transceiver

Signals and indications are issued on IOM-2 (C/I-indications) and on the U-interface (predefined U-signals).

C/I Indications

AI Activation Indication
The U-transceiver has established transparency of transmission in the direction IOM to U-interface. In an NT1, the S-transceiver is requested to send INFO4 and to achieve transparency of transmission in the direction IOM to S/T-interface.

AIL Activation Indication Loop-back
The U-transceiver has detected ACT = 1 while loop-back 2 is still established. In an NT1, the S-transceiver is requested to send INFO4 (if a transparent loop-back 2 is to be implemented) and to keep loop-back 2 active.

AR Activation Request
The U-receiver has synchronized on the incoming signal. In an NT1, the S-transceiver is requested to start the activation procedure on the S/T-interface by sending INFO2.

ARL Activation Request Loop-back
The U-transceiver has detected a loop-back 2 command in the EOC-channel and has established transparency of transmission in the direction IOM to U-interface. In an NT1, the S-transceiver is requested to send INFO2 (if a transparent loop-back 2 is to be implemented) and to operate loop-back 2.

DC Deactivation Confirmation
Idle code on the IOM-2 interface. The U-transceiver stays in the power-down mode unless an activation procedure has been started from the LT-side. The U-interface may be activated but the S/T-interface has to remain deactivated.

DR Deactivation Request
The U-transceiver has detected a deactivation request command from the LT-side for a complete deactivation or a S/T only deactivation. In an NT1, the S-transceiver is requested to start the deactivation procedure on the S/T-interface by sending INFO0.

EI1 Error Indication 1
The U-transceiver has entered a failure condition caused by loss of framing on the U-interface or expiry of timer T1.

INT Interrupt (Stand-alone mode only)
A level change on input pin INT triggers the transmission of this C/I code in four successive IOM-2 frames. Please refer to page 96 for details.

PU Power Up
The U-transceiver provides IOM-2 clocks.

Signals on U-Interface

The signals SNx, TN and SP transmitted on the U-interface are defined in **Table 22 on page 100**.
The polarity of the transmitted ACT-bit is as follows:

a = 0/1 corresponds to ACT-bit set to binary “0/1”

The polarity of the issued SAI-bit depends on the received C/I-channel code: DI and TIM leads to SAI = 0, any other C/I-code sets the SAI-bit to 1 indicating any activity on the S/T-interface.

2.5.7.5 States

The following states are used:

Alerting

The wake-up signal TN is transmitted for a period of T11 either in response to a received wake-up signal TL or to start an activation procedure on the LT-side.

Alerting 1

“Alerting 1” state is entered when a wake-up tone was received in the “Receive Reset” state and the deactivation procedure on the NT-side was not yet finished. The transmission of wake-up tone TN is started.

Analog Loop-Back

Upon detection of binary “1s” for a period of 6–12 ms and of the superframe indication, the “Analog loop-back” state is entered and transparency is achieved in both directions of transmission. This state can be left by making use of any unconditional command. Only the C/I-channel code RES should be used, however. This assures that the EC- and EQ-coefficients are set to zero and that for a subsequent normal activation procedure the receiver updating algorithms converge correctly.

Deactivated

The ’Deactivated’ state is a power-down state. If there are no pending Monitor channel messages from the U-transceiver, i.e. all Monitor channel messages have been

acknowledged, the IOM-clocks are turned off. No signal is sent on the U-interface.
The U-transceiver waits for a wake-up signal TL from the LT-side to start an activation procedure. To enter state 'IOM Awake' a wake-up signal (DIN = 0) is required if the IOM-clocks are disabled. The wake-up signal is provided via the IOM-2 interface (pin DIN = 0). If the IOM-clocks were active in state 'Deactivated' C/I-code TIM is sufficient for a transition to state 'IOM Awake'.

EC Training

The signal SN1 is transmitted on the U-interface to allow the NT-receiver to update the EC-coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled. The "EC-training" state is left when the EC has converged (LSEC) or when timer T12 has elapsed.

EC-Training 1

The "EC-Training 1" state is entered if transmission of signal SN1 has to be started and the deactivation procedure on the NT-side is not yet finished.

EC-Training AL

This state is entered in the case of an analog loop-back. The signal SN1 is transmitted on the U-interface to allow the NT-receiver to update the EC-coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled. The "EC-training" state is left when the EC has converged (LSEC) or when timer T12 has elapsed.

EQ-Training

The receiver waits for signal SL1 or SL2 to be able to update the AGC, to recover the timing phase, to detect the synch-word (SW), and to update the EQ-coefficients. The "EQ-training" state is left upon detection of binary "0s" in the B- and D-channels for a period of 6–12 ms corresponding to the detection of SL2.

Error S/T

Loss of framing or loss of incoming signal has been detected on the S/T-interface (EI1). The LT-side is informed by setting the ACT-bit to "0" (loss of transparency on the NT-side). The following codes are issued on the C/I-channel:

– Normal activation or single-channel loop-back: AR
– Loop-back 2: ARL

IOM®-2 Awaked

Timing signals are delivered on the IOM-2 interface. The U-transceiver enters the "Deactivated" state again upon detection of the C/I-channel code DI (idle code).

Pending Deactivation of S/T

The U-transceiver has received the UOA-bit at zero after a complete activation of the S/T-interface. The U-transceiver deactivates the S/T-interface by issuing DR in the C/I-channel. The value of the ACT-bit depends on its value in the previous state.

Pending Deactivation of U-Interface

The U-transceiver waits for the receive signal level to be turned off (LSU) to enter the “Receiver Reset” state and start the deactivation procedure.

Pending Receive Reset

The “Pending Receive Reset” state is entered upon detection of loss of framing on the U-interface or expiry of timer T1. This failure condition is signalled to the LT-side by turning off the transmit level (SN0). The U-transceiver then waits for a response (no signal level LSU) from the LT-side to enter the “Receive Reset” state.

Pending Timing

The pending timing state assures that the C/I-channel code DC is issued four times before the timing signals on the IOM-2 interface are turned off.
In case the NT-auto mode (Pin AUA=1) is selected the recognition of the LT wake-up tone TL is assumed everytime the “Pending Timing” state has been entered from the “Test” state. This function guarantees that the NT (in NT-auto mode) starts one single activation attempt after having been resetted. After the assumed TL recognition in this state the activation will proceed normally.

Receive Reset

The “Receive Reset” state is entered upon detection of a deactivation request from the LT-side, after a failure condition on the U-interface (loss of signal level LSUE), or following the “Pending Reset” state upon expiry of timer T1 or loss of framing. No signal is transmitted on the U-interface, especially no wake-up signal TN, and the S-transceiver or microcontroller is requested to start the deactivation procedure on the NT-side (DR). Timer T7 assures that no activation procedure is started from the NT-side for a minimum period of T7. This gives the LT a chance to activate the NT.
The state is left only after completion of the deactivation procedure on the NT-side (receipt of the C/I-channel code DI), unless a wake-up tone is received from the LT-side.

Synchronized 1

When reaching this state the U-transceiver informs the LT-side by sending the superframe indication (inverted synch.-word). The loop-back commands decoded by the EOC-processor control the output of the transmit signals:

– Normal ACT and UOA = 0: SN3
– Any loop-back and UOA = 0 (no loop-back): SN3T

The value of the issued SAI-bit depends on the received C/I-channel code: DI and TIM lead to SAI = 0, any other C/I-code sets the SAI-bit to 1 indicating activity on the S/T-interface. The U-transceiver waits for the receipt of UOA = 1 to enter the “Synchronized 2” state.

Synchronized 2

In this state the U-transceiver has received UOA = 1. This is a request to activate the S/T-reference point. The loop-back commands detected by the EOC-processor control the output of indications and transmit signals:

– Normal activation and UOA = (1): SN3 and AR
– Single channel loop-back and UOA = (1): SN3T and AR
– Loop-back 2 (LBBD): SN3T and ARL

The value of the issued SAI-bit depends on the received C/I-channel code: DI and TIM lead to SAI = 0, any other C/I-code sets the SAI-bit to 1 indicating activity on the S/T-interface. The U-transceiver waits for the receipt of the C/I-channel code AI to enter the “Wait for ACT” state.

Test

The “Test” mode is entered when the unconditional commands RES, SSP, Pin-RES or Pin-SSP are used. It is left when normal U-transceiver operation is selected via pins $\overline{\text{RES}}$ and TSP and the C/I-channel codes DI or ARL are received.

The following signals are transmitted on the U-interface:

– No signal level (SN0) when the C/I-channel code RES is applied or a hardware reset is activated.
– Single pulses (SP) when the C/I-channel code SSP is applied or pin TSP =1.

Transparent

This state is entered upon the detection of ACT = 1 received from the LT-side and corresponds to the fully active state. In the case of a normal activation in both directions of transmission the the following codes are output:

– Normal activation or single-channel loop-back: AI
– Loop-back 2: AIL

Wait for ACT

Upon the receipt of AI, the ACT-bit is set to “1” and the NT waits for a response (ACT = 1) from the LT-side. The output of indications and transmit signals is as defined for the “Synchronized” state.

Wait for SF

Upon detection of SL2, the signal SN2 is sent on the U-interface and the receiver waits for detection of the superframe indication. Timer T1 is then stopped and the “Synchronized” state is entered.

Wait for SF AL

This state is entered in the case of an analog loop-back and allows the receiver to update the AGC, to recover the timing phase, and to update the EQ-coefficients. Signal SN3 is sent instead of signal SN2 in the “Wait-for-SF” state.

2.5.8 C/I Codes

Both commands and indications depend on the data direction. **Table 15** presents all defined C/I codes. A new command or indication will be recognized as valid after it has been detected in two successive IOM frames (Double last-look criterion). Indications are strictly state orientated. Refer to the state diagrams in the previous sections for commands and indications applicable in various states.

Table 15 U-Transceiver C/I Codes

Code	NT-Mode	
	IN	OUT
0000	TIM	DR
0001	RES	–
0010	–	–
0011	–	–
0100	EI1	EI1
0101	SSP	–
0110	DT	INT
0111	–	PU
1000	AR	AR
1001	–	–
1010	ARL	ARL
1011	–	–
1100	AI	AI
1101	–	–
1110	–	AIL
1111	DI	DC

AI	Activation Indication	EI1	Error Indication 1
AR	Activation Request	INT	Interrupt
ARL	Activation Request Local Loop	PU	Power-Up
DC	Deactivation Confirmation	RES	Reset
DI	Deactivation Indication	SSP	Send-Single-Pulses test mode
DR	Deactivation Request	TIM	Timing request
DT	Data-Through test mode		

2.5.9 Layer 1 Loop-Backs

Test loop-backs are specified by the national PTTs in order to facilitate the location of defect systems. Four different loop-backs are defined. The position of each loop-back is illustrated in **figure 23**.

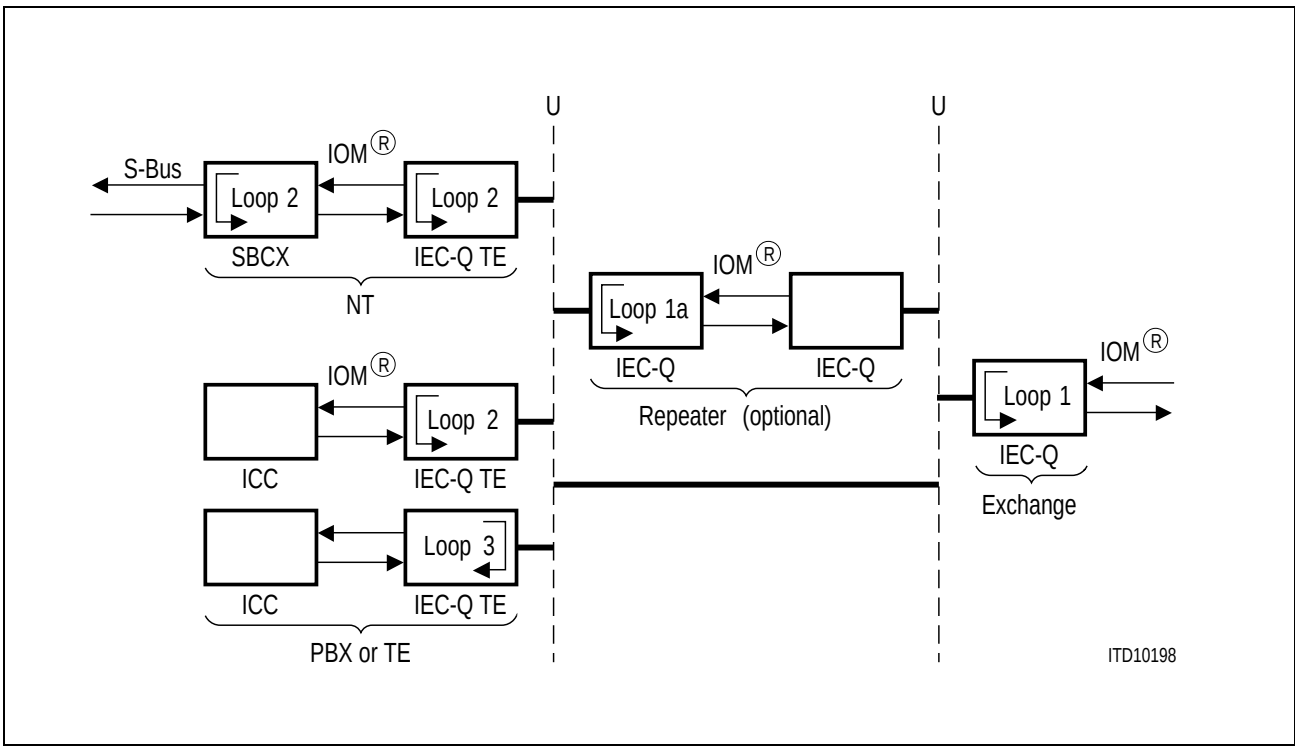


Figure 23 Test Loop-Backs Supported by the IEC-Q TE

Loop-backs #1, #1A and #2 are controlled by the exchange. Loop-backs #3 is controlled by the terminal. All loop-back types are transparent. This means all bits that are looped back will also be passed onwards in the normal manner.

2.5.9.1 Loop-Back (No. 2)

Normally loop-back #2 is controlled from the exchange via the EOC commands LBBD, LB1 and LB2. In EOC auto mode the EOC commands are recognized and executed automatically (see page 51). The single channel loop-backs (LB1, LB2) are closed in the U-transceiver itself whereas the complete loop-back (LBBD) is closed in a connected S-transceiver.

All loop-back functions are latched. This allows channel B1 and channel B2 to be looped back simultaneously. All loop-backs are opened when the EOC command RTN is sent by the LT.

Complete loop-back

The complete loop-back comprises both B-channels and the D-channel. It may be closed either in the U-transceiver itself , in the S-transceiver or in an external device.

When receiving the EOC-command LBBD in EOC auto mode, the U-transceiver does not close the loop-back immediately. Because the intention of this loop-back is to test the complete NT, the U-transceiver passes the complete loop-back request on to the IOM-2 interface. This is achieved by issuing the C/I-code AIL in the “Transparent” state or C/I = ARL in states different than “Transparent”. In applications that include a microcontroller, the software decides where to close the loop, whereas in an NT1 the loop is closed automatically in the S-transceiver (e.g. SBCX).

Single-channel loop-back (B1/B2)

Single-channel loop-backs are always performed directly in the U-transceiver if EOC auto mode is selected. No difference between the B1-channel and the B2-channel loop-back control procedure exists. They are therefore discussed together.

The B1-channel is closed with the EOC-command LB1. LB2 causes the channel B2 to loop-back. Because these functions are latched, both channels may be looped back simultaneously by sending first the command to close one channel followed by the command for the remaining channel.

2.5.9.2 Analog Loop-Back (No. 3)

Loop-back #3 is invoked by sending C/I command ARL to the U-transceiver. The loop is closed by the U-transceiver as near to the U-interface as possible. For this reason it is also called analog loop-back. All analog signals will still be passed on to the U-interface. As a result the opposite station (LT) is activated as well.

In order to open an analog loop-back correctly, reset the U-transceiver into the TEST state with the C/I-command RES. This ensures that the echo coefficients and equalizer coefficients will converge correctly when activating the following time.

2.5.10 Analog Line Port

The analog part of the IEC-Q TE consists of three main building blocks:

– The analog-to-digital converter in the receive path
– The digital-to-analog converter in the transmit path
– The output buffer in the transmit path

Furthermore it contains some special functions. These are:

– Analog test loop-back
– Level detect function

Analog-to-Digital Converter

The ADC is a sigma-delta modulator of second order using a clock rate of 15.36-MHz.

The peak input signal measured between AIN and BIN must be below 4 Vpp. In case the signal input is too low (long range), the received signal is amplified internally by 6 dB. The maximum signal to noise ratio is achieved with 1.3 Vpp (long range) and 2.6 Vpp (short range) input signal voltage.

Digital-to-Analog Converter

The output pulse is shaped by a special DAC. The DAC was optimized for excellent matching between positive and negative pulses and high linearity. It uses a fully differential capacitor approach. The staircase-like output signal of the DAC drives the output buffers. The shape of a DAC-output signal is shown below, the peak amplitude is normalized to one. This signal is fed to an RC-lowpass of first order with a corner frequency of 1 MHz $\pm$ 50%.

The duration of each pulse is 24 steps, with T0 = 0.78 µs per step. On the other hand, the pulse rate is 80-kHz or one pulse per 16 steps. Thus, the subsequent pulses are overlapping for a duration of 8 steps.

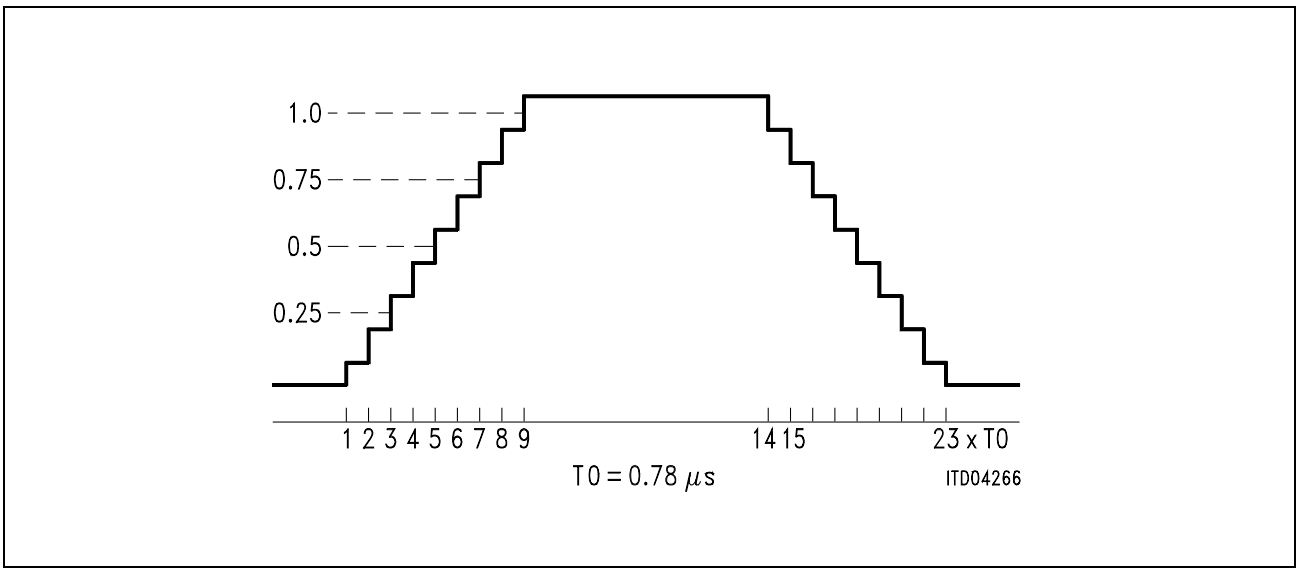


Figure 24 DAC-Output for a Single Pulse

Output Stage

The output stage consists of two identical buffers, operated in a differential mode. This concept allows an output-voltage swing of 6.4 Vpp at the output pins of the IEC-Q TE. The buffers are optimized for:

– High output swing
– High linearity
– Low quiescent current to minimize power consumption

The output jitter produced by the transmitter (with jitter-free input signals) is below 0.02 UIpp (Unit intervall = 12.5 µs, peak-peak) measured with a high-pass filter of 30-Hz cutoff frequency. Without the filter the cutoff frequency is below 0.1 UIpp.

Analog Loop-Back Function

The loop-back C/I command ARL activates an internal, analog loop-back. This loop-back is closed near the U-interface. All signals received on AIN / BIN will neither be evaluated nor recognized after reaching the “Synchronized” state in NT-mode.

Level Detect

The level detect circuit evaluates the differential signal between AIN and BIN. The differential threshold level is between 4 mV and 28 mV. The DC-level (common mode level) may be between 0 V and 3 V. Level detect is not effected by the range setting.

Pulse Shape

The pulse mask for a single positive pulse measured between AOUT and BOUT at a load of 98 Ω is given in the following figure.

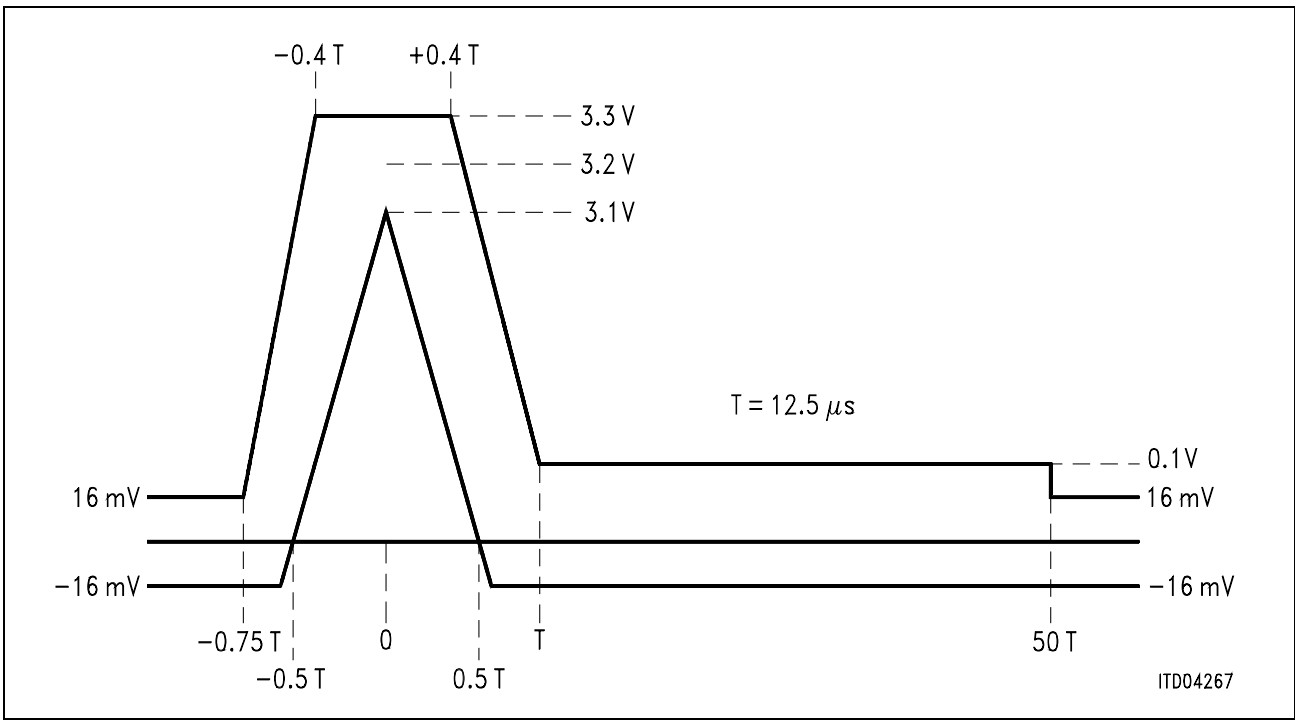


Figure 25 Pulse Mask for a Single Positive Pulse

Hybrid

The hybrid circuit for the IEC-Q TE is shown on page 110.

2.6 Access to IOM-2 Channels

Important: This chapter applies only in µP mode

In µP mode the microcontroller has access to the IOM-2 channels via the processor interface (PI) and registers.

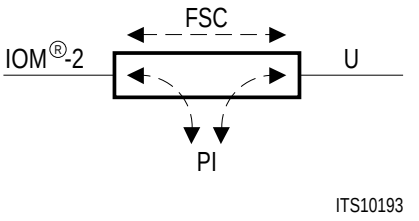


Figure 26 Access to IOM-2 Channels (µP mode)

The processor interface can be understood as an intelligent switch between IOM-2 and the U-transceiver. It handles D, B1, B2, C/I and Monitor-channel data. The data can either be transferred directly between IOM-2 and the U-transceiver, or be controlled via the PI. The PI acts as an additional participant to the Monitor channel.

Switching directions are selected by setting the register SWST as indicated below:

SWST-Register

WT	B1	B2	D	CI	MON	BS	SGL

- Setting one of the 5 bits B1, B2, D, CI, or MON of SWST to "1" enables the µP access to the corresponding data.
- Setting the bits listed above to "0" directly passes the corresponding data from IOM-2 to the U-transceiver and vice versa.

For a description of the bits WT, BS and SGL please refer to **page 127**. The default value after hardware reset is "0" at all 8 positions.

2.6.1 B-Channel Access

Setting SWST:B1 (B2) to "1" enables the microprocessor to access B1 (B2)-channel data between IOM-2 and the U-transceiver.

Eight registers (see **table 16**) handle the transfer of data from IOM-2 to the µP, from the µP to IOM-2, from the µP to U and from U to the µP:

Table 16 B1/B2-Channel Data Registers

Register	Function
WB1U	write B1-channel data to U-interface
RB1U	read B1-channel data from U-interface
WB1I	write B1-channel data to IOM-2
RB1I	read B1-channel data from IOM-2
WB2U	write B2-channel data to U-interface
RB2U	read B2-channel data from U-interface
WB2I	write B2-channel data to IOM-2
RB2I	read B2-channel data from IOM-2

Every time B-channel bytes arrive, an interrupt ISTA:B1 or ISTA:B2 respectively is created. It is cleared after the corresponding registers have been read. ISTA:B1 is cleared after RB1U and RB1I have been read. ISTA:B2 is cleared after RB2I and RB2U have been read. After an interrupt the data in RB1U and RB1I is stable for 125µs.

2.6.2 D-Channel Access

Setting SWST:D to "1" enables the microprocessor to access D-channel data between the IOM-2 and the U-interface.

Four registers (see **table 17**) handle the transfer of data from IOM-2 to the µP, from the µP to IOM-2, from the µP to U and from U to the µP.

Table 17 D-channel data registers

Register	Function
DWU	write D-channel data to U-interface
DRU	read D-channel data from U-interface
DWI	write D-channel data to IOM-2
DRI	read D-channel data from IOM-2

Two 2-bit FIFOs of length 4 collect the incoming D-channel packets from IOM and U. Every fourth IOM-frame they are full, an interrupt ISTA:D is generated and the contents

of the FIFOs are parallely shifted to DRU and DRI respectively. DRU and DRI have to be read before the next interrupt ISTA:D can occur, otherwise 8 bits will be lost. DWU and DWI have to be loaded with data for 4 IOM-frames. Data in DWU and DWI is assumed to be valid at the time ISTA:D occurs. The register contents are shifted parallely into two 2-bit FIFOs of length four, from where the data is put to IOM-2 and U respectively during the following 4 IOM-frames. During this time, new data can be placed on DWU and DWI. DWU and DWI are not cleared after the data was passed to the FIFOs. That is, a byte may be put into DWU or DWI once and continously passed to IOM or U, respectively. **Figure 27** illustrates this procedure:

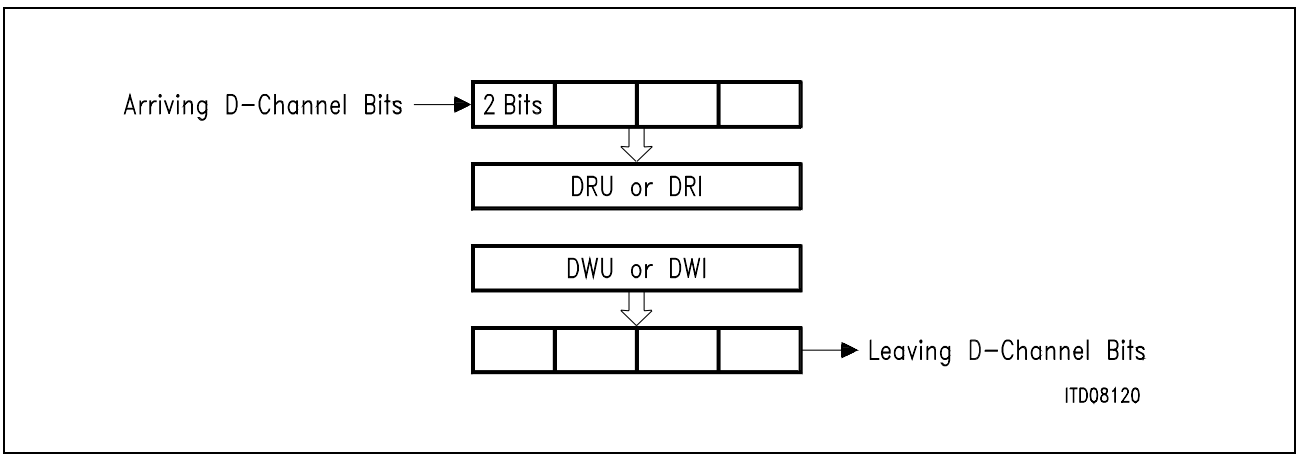


Figure 27 Procedure for the D-Channel Processing

Note: Default of DWU, DWI, DRU and DRI after reset is "FF_H".

2.6.3 C/I Channel Access

Setting SWST:CI to "1" enables the microprocessor to access C/I-commands and indications between IOM-2 and the U-transceiver.

A change in two consecutive frames (double last look) in the C/I-channel on IOM-2 is indicated by an interrupt ISTA:CICI. The received C/I-command can be read from register CIRI. A change in the C/I-channel coming from the U-transceiver is indicated by an interrupt ISTA:CICU. The new C/I-indication can be read from register CIRU .

Note: The term C/I-indication always refers to a C/I-code coming from the U-transceiver, whereas the term C/I-command refers to a C/I-code going into the U-transceiver.

A C/I-code going to the U-transceiver has to be written into the CIWU-register. A C/I-code to IOM-2 has to be written into the CIWI-register. The contents of both registers (CIWU and CIWI) will be transferred at the next available IOM-2 frame. The registers are not cleared after the transfer. Therefore, it is possible to continously send C/I codes to IOM-2 or the U-transceiver by only writing the code into the register once.

C/I-commands to the U-transceiver have to be applied at least for two IOM-2 frames (250 µs) to be considered as valid.

In TE mode (i.e. 1.536 MHz DCL), the ADF2:TE1 bit is used to direct the C/I-channel access either to IOM-2 channel 0 (ADF2:TE1 = 0, default) or to IOM-2 channel 1 of the IOM-2 terminal structure (ADF2:TE1 = 1), **figure 28** on **page 84**. This allows to program terminal devices such as the ARCOFI via the processor interface of the IEC-Q TE. The C/I code going to IOM-2 is 4 bits long if it is written to IOM-2 channel 0 (ADF2:TE1 = 0). If written to IOM-2 channel 1 this C/I code is 6 ibts long (ADF2:TE1 = 1). If the ADF2:TE1 bit is 1, the C/I channel on IOM-2 channel 0 is passed transparently from the IOM-2 interface to the IEC-Q TE itself.

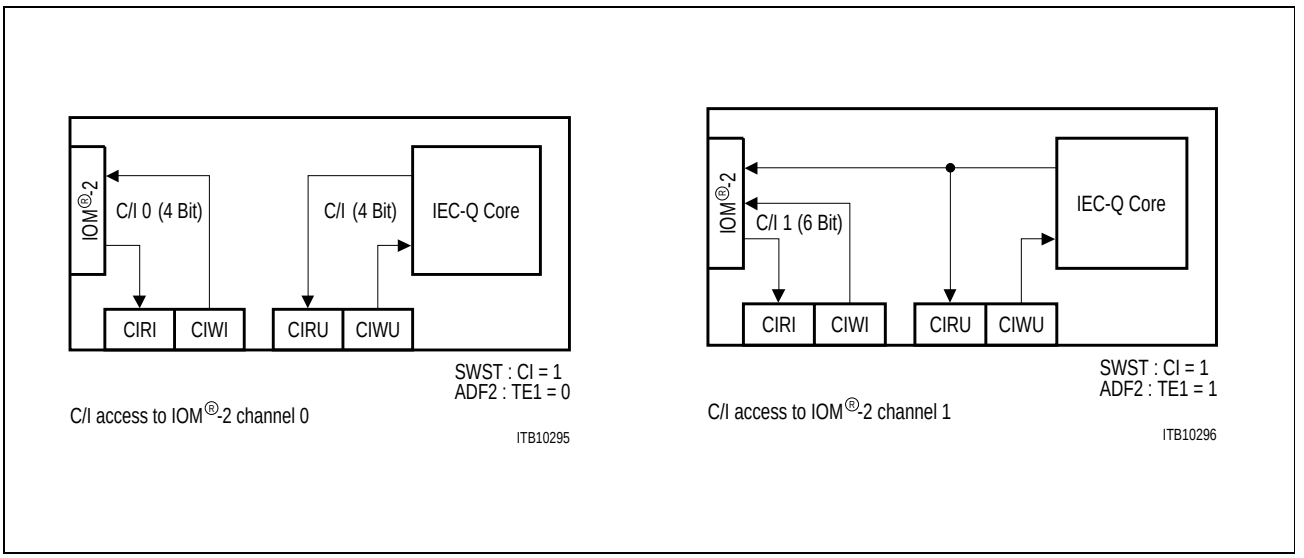


Figure 28 C/I Channel Access

2.6.4 Monitor Channel Access

Setting SWST:MON to "1" enables the microprocessor to access Monitor-channel messages at IOM-2 interface and the U-transceiver. Monitor-channel access can be performed in three different IOM-2 channels (see **figure 29, page 85**).

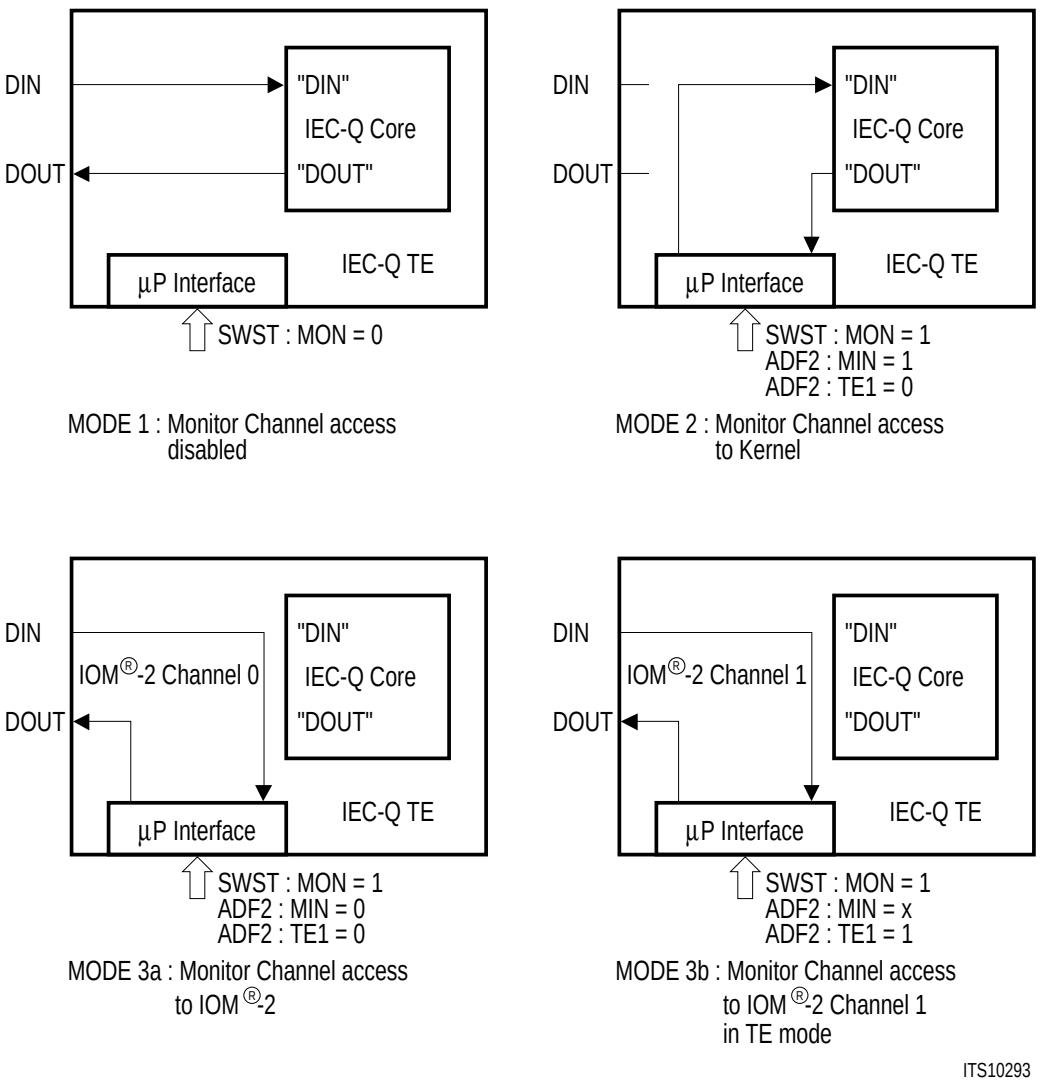


Figure 29 Monitor Channel Access Directions

Setting SWST:MON to ’0’ disables the controller access to the Monitor channel (**figure 29** upper left part).

Setting SWST:MON to ’1’ enables three different ways of controller access to the Monitor channel. ADF2:TE1 set to ’0’ allows to either access the U-transceiver core of the IEC-Q TE (see **figure 29** upper right part, ADF2:MIN = ’1’) or the IOM-2 interface of the IEC-Q TE (**figure 29** lower left part, ADF2:MIN = ’0’).

Setting ADF2:TE1 to ’1’ in TE mode gives access to IOM-2 channel 1 rather than IOM-2 channel 0 directed out of the IEC-Q TE. This allows to program devices linked to IOM-2 channel 1 (e.g. ARCOFI) via the processor interface of the IEC-Q TE.

2.6.4.1 Monitor Channel Protocol

The PI allows to program the IEC-Q TE Monitor channel in the way known from the PEB 2070 ICC.

The Monitor channel operates on an *asynchronous* basis. While data transfers on the IOM-bus occur synchronized to frame sync FSC, the flow of data is controlled by a handshake procedure using the Monitor Channel Receive (MR) and Monitor Channel Transmit (MX) bits. For example: data is placed onto the Monitor channel and the MX bit is activated. This data will be transmitted repeatedly once per 8-kHz frame until the transfer is acknowledged via the MR bit.

The microprocessor may either enforce a "1" (idle) in MR, MX by setting the control bit MOCR:MRC or MOCR:MXC to "0", or enable the control of these bits internally by the IEC-Q TE according to the Monitor channel protocol. Thus, before a data exchange can begin, the control bits MRC or MXC should be set to "1" by the microprocessor.

The Monitor channel protocol is illustrated in **figure 30**. The relevant control and status bits for transmission and reception are:

Monitor Transmit Bits

Register	Bit	control / status	Function
MOCR	MXC	control	MX Bit Control
	MXE		Transmit Interrupt Enable
MOSR	MDA	status	Data Acknowledged
	MAB		Data Abort
STAR	MAC		Transmission Active

Monitor Receive Bits

Register	Bit	control / status	Function
MOCR	MRC	control	MR Bit Control
	MRE		Receive Interrupt Enable
MOSR	MDR	status	Data Received
	MER		End of Reception

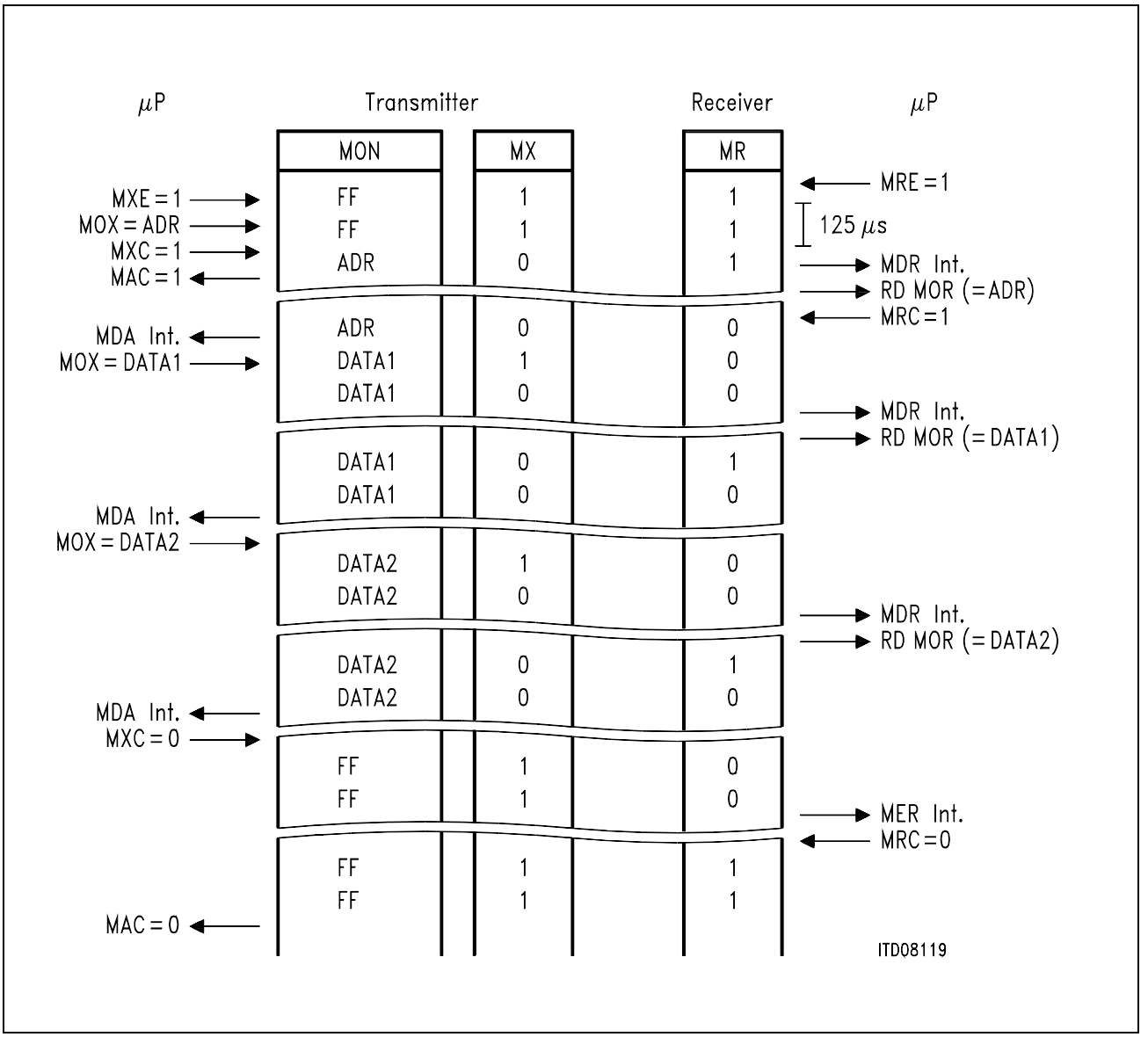


Figure 30 Monitor Channel Protocol

Before starting a transmission, the microprocessor should verify that the transmitter is inactive, i.e. that a possible previous transmission has been terminated. This is indicated by a "0" in MOSR:MAC, the Monitor Channel Active status bit.

To enable interrupts for the transmitter the MOCR:MXE bit must be set to “1“ (For details see **section 4.1.1 on page 115**). After having written the Monitor Data Transmit (MOX) register, the microprocessor sets the Monitor Transmit Control bit MXC to "1". This enables the MX bit to go active (“0“), indicating the presence of valid Monitor data (contents of MOX) in the corresponding frame. As a result, the receiving device stores the Monitor byte in its Monitor Receive (MOR) register and generates an MDR interrupt status.

Alerted by the MDR interrupt, the microprocessor reads the Monitor Receive (MOR)

register. When it is ready to accept data (e.g. based on the value in MOR, which in a point-to-multipoint application might be the address of the destination device), it sets the MR control bit MRC to "1" to enable the receiver to store succeeding Monitor channel bytes and acknowledge them according to the Monitor channel protocol. In addition, it enables other Monitor channel interrupts by setting Monitor receive Interrupt Enable (MRE) to "1".

As a result, the first Monitor byte is acknowledged by the receiving device setting the MR bit to "0". This causes a Monitor Data Acknowledge (MDA) interrupt status at the transmitter.

A new Monitor data byte can now be written by the microprocessor in MOX. The MX bit is still in the active (“0“) state. The transmitter indicates a new byte in the Monitor channel by returning the MX bit active after sending it once in the inactive state. As a result, the receiver stores the Monitor byte in MOR and generates a new MDR interrupt status. When the microprocessor has read the MOR register, the receiver acknowledges the data by returning the MR bit active after sending it once in the inactive state. This in turn causes the transmitter to generate an MDA interrupt status.

This "MDA interrupt – write data – MDR interrupt – read data – MDA interrupt" handshake is repeated as long as the transmitter has data to send. Note that the Monitor channel protocol imposes no maximum reaction times to the microprocessor.

When the last byte has been acknowledged by the receiver (MDA interrupt status), the microprocessor sets the Monitor Transmit Control bit (MXC) to "0". This enforces an inactive ("1") state in the MX bit. Two frames of MX inactive signifies the end of a message. Thus, a Monitor Channel End of Reception (MER) interrupt status is generated by the receiver when the MX bit is received in the inactive state in two consecutive frames. As a result, the microprocessor sets the MR control bit MRC to “0“, which in turn enforces an inactive state in the MR bit. This marks the end of the transmission, making the Monitor Channel Active (MAC) bit return to "0".

During a transmission process, it is possible for the receiver to ask for a transmission to be aborted by sending an inactive MR bit value in two consecutive frames. This is effected by the microprocessor writing the MR control bit MRC to "0". An aborted transmission is indicated by a Monitor Channel Data Abort (MAB) interrupt status at the transmitter.

In TE mode, the ADF2:TE1 bit is used to direct the Monitor access either to IOM-channel 0 (ADF2:TE1 = "0", default) or to IOM-channel 1 of the IOM-Terminal structure. This allows to program terminal devices such as the ARCOFI via the processor interface of the IEC-Q TE. If the ADF2:TE1 bit is "1", the Monitor channel on IOM-channel 0 is passed transparently from the IOM-2 interface to the IEC-Q TE itself.

2.7 S/G Bit and BAC Bit in TE Mode

Important: This chapter applies only in µP mode and if DCL = 1.536 MHz (TE mode).

If DCL = 1.536 MHz the IOM-2 interface consists of three IOM-2 channels. The last octet of an IOM-2 frame includes the S/G and the BAC bit (chapter 2.3.1.1, page 31). Either or both bits can be used in various applications including

- the D-channel arbitration in a PBX via an ELIC on the linecard
- the synchronization of a base station in radio in the local loop (RLL) or wireless PBX applications

The S/G is always written and never read by the IEC-Q TE. Its value depends on the last received EOC-command and on the status of the BAC bit.The processing mode for the S/G bit is selected via bits SWST:BS, SWST:SGL and ADF:CBAC according to **table 18**. A detailed description of the S/G bit in all modes is provided in **Appendix B**.

Table 18 S/G Processing Mode

SWST:		ADF:	Description (X is don't care)	Application
BS	SGL	CBAC		
0	0	x	S/G bit always "0"	(default)
0	1	0	S/G bit always "1"	S/G and BAC are handled by other devices than the IEC-Q TE
0	1	1	S/G bit set to "1" continously with EOC 25_H received, reset to "0" with EOC 27_H received BAC bit controlls S/G-bit, upstream D-channel not affected	ELIC on linecard, Interframe fill of terminals contains zeroes (e.g. '01111110')
1	0	x	S/G bit set to "1" for 4 IOM-frames with EOC 25_H receivced, automatically reset to "0" after that	Synchronizaiton of base station, e.g. IBMC or MBMC
1	1	0	S/G bit set to "1" continously with EOC 25_H receivced, reset to "0" with EOC 27_H received	
1	1	1	S/G bit set to "1" continously with EOC 25_H receivced, reset to "0" with EOC 27_H received BAC bit controlls S/G bit and upstream D-channel according to **table 19**.	ELIC on linecard, Interframe fill of terminals are 'ones'

2.7.1 Applications with ELIC on the Linecard (PBX)

The S/G bit on DOUT (downstream) and the BAC bit on DIN (upstream) can be used to allow D-channel arbitration similar to the operation of the Upn interface realised with the OCTAT-P and the ISAC-P TE. The basic function is as follows:

The PBX linecard using the ELIC assigns one HDLC controller to a number of terminals. As soon as one terminal *T* requests the D-channel, e.g. for signalisation, all other terminals receive a message indicating the D-channel to be blocked for them. The request is done with the BAC bit. At terminal *T* the BAC bit is set and the IEC-Q TE transfers the need for the D-channel to the LT-side. There, the HDLC-controller is assigned to the appropriate IOM-channel. Once this is done and indicated to the terminal by means of the S/G bit, the terminal begins to send D-channel messages.

Note that this procedure is somewhat different from the operation of the OCTAT/ISAC-P TE. There, the beginn of the upstream D-channel data transfer itself indicates the need for the HDLC-controller. This implies that any other terminal, that incidentally sent a HDLC-message the same time, can be stopped before the message is lost in case the HDLC-controller is not available. The U-interface featured by the IEC-Q TE is not able to transfer the available/blocked information often enough to ensure this. Hence, it is necessary to indicate a D-channel access by the terminal in advance. "In advance" actually means about 14 ms.

Giving MON-0 25_H at the LT during transparent operation will cause the D-channel access at the NT-side to be on "STOP". As one EOC-message is transmitted via the EOC-channel once every 6 ms, the S/G bit on IOM-2 can be set in 6 ms intervals.

If the 4 channel LT chip set PEB 24911 (DFE-Q) is used in the LT, a PEB 20550 (ELIC) can arbitrate the D-channel via the C/I command as known from the OCTAT-P and QUAT-S devices. Please refer to the PEB 24911 Data Sheet for detailed information on this.

The BAC bit together with the EOC-messages received from the LT control the S/G bit and the upstream D-channel according to the **table 19.**

Table 19 Control Structure of the S/G Bit and of the D-Channel

BAC bit of last IOM-frame	S/G bit 1 = stop 0 = go	D-channel upstream
0	reflects last received EOC message after falling edge after delay TD1 (1.5 ms and two EOC-frames)	tied to "0"
1	1	set transparent with first "0" in D-channel

D-Channel Request by the Terminal

Figure 31 illustrates the request for the HDLC-controller by the terminal. The start state is BAC = 1 at DIN after TD1 has expired. That causes the S/G bit to be set to the stop position.

BAC = 1 received on DIN sets the S/G bit on DOUT to the stop position ("1") at the next IOM-frame. When the terminal requests access to the HDLC-controller in the ELIC it sets the BAC-bit at DIN of it's IEC-Q TE to "0". That causes the D-channel data upstream to be tied to "0" and the S/G-bit to be set to "1". The ELIC receives the zeros and reacts by assigning the HDLC-controller to this very terminal. This is indicated via the change of C/I code downstream at the LT side resulting in the S/G bit to be set to "0" ('go') after delay TD1 (see below for the explanation of TD1 and TD2).

The IEC-Q TE will continue to send "0" upstream in the D-channel until the actual HDLC data arrives at DIN.The HDLC-frame itself, marked by the first "0" in the D-channel will reset the D-channel back to transparent. This allows to have arbitrary delays between the S/G bit going to "0" and the D-channel being used without the risk of loosing the HDLC-controller by sending an abort request consisting of all "1".

At the end of the HDLC-frame the BAC bit is reset to "1" again by the layer-2 controller (e.g. SMARTLINK; ICC). This causes the S/G bit to be set to "1" in the next IOM frame which stops a possible second HDLC-frame that could not be processed in the ELIC anymore.

TD1 and TD2

The delays TD1 and TD2 (see **figure 31**) have the following reasons: TD2 is caused by the 6ms interval in which an EOC message can be transmitted on the Uko interface. As an EOC-message can start once every 6 ms and will take 6 ms to be transmitted, TD2 will be 12 ms in the worst case.

TD1 is at minimum 7.5 ms depending on the location of the superframe at the time the HDLC-controller is requested by the terminal. This delay is necessary because instead of receiving an EOC-message "go" as requested, the terminal could as well receive the EOC message "stop" because the HDLC-controller was assigned to an other subscriber just before .

Flags as interframe Fill

The influence to the upstream D-channel can be disabled while the control of the S/G-bit via EOC-messages and via the BAC bit still is given as described above by setting SWST:BS to "0", SWST:SGL to "1" and ADF:CBAC to "1". This is usefull when having a controlling device in the terminal, that is able to send the interframe timefill "flags".

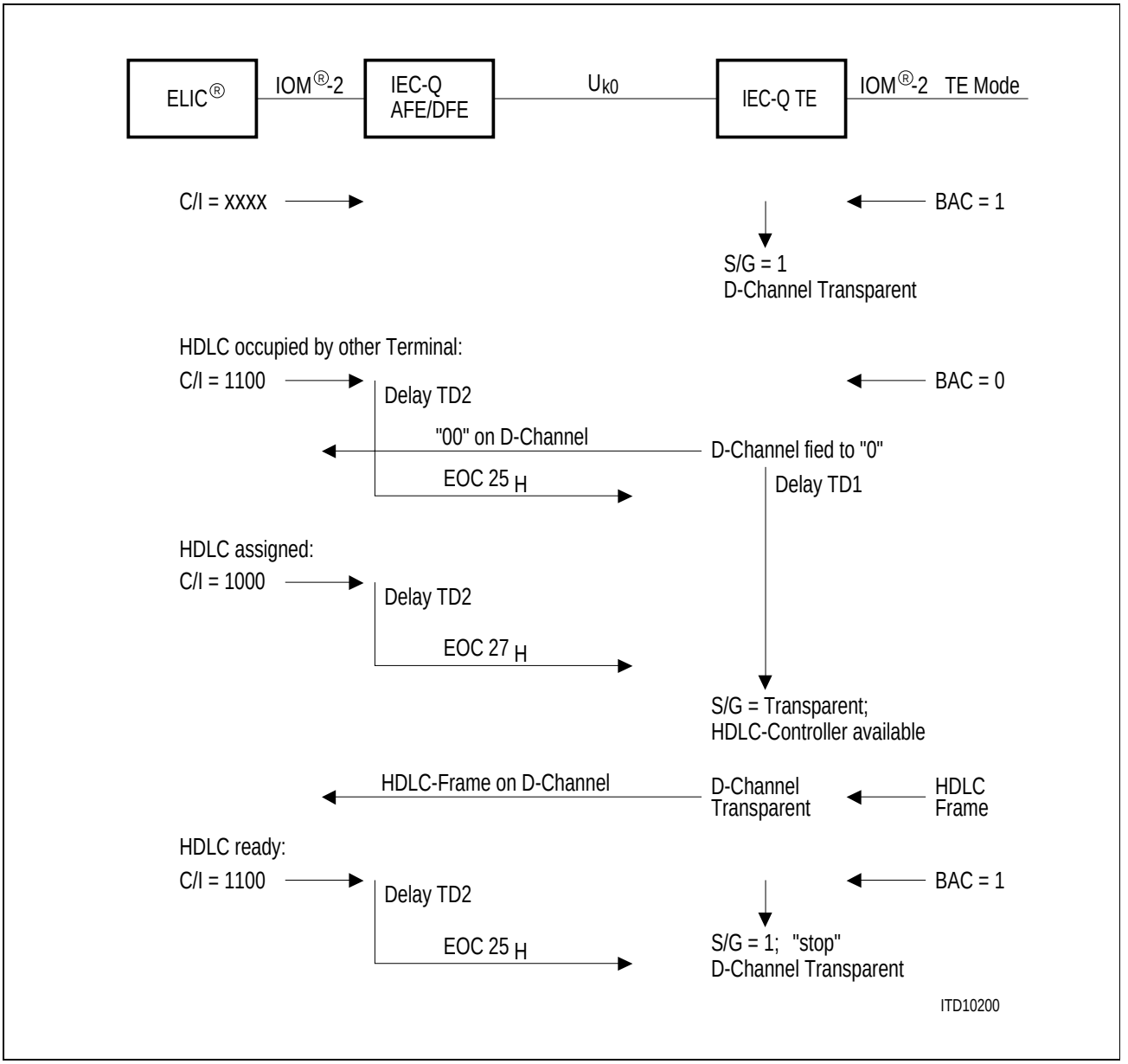


Figure 31 D-Channel Request by the Terminal

2.8 Reset

Important: This chapter applies only in µP mode.

Several resets are provided in the IEC-Q TE. Their effects are summarized in **table 20**.

Table 20 Reset

Reset	Condition	Effect	Pin $\overline{RST}$ active
Power-on	Power-on	Resets the state machine and all registers	yes
Hardware Reset	Pin $\overline{RES}$ = 0	Resets the state machine and all registers exept for STCR register	no
Watchdog	Watchdog expired	Resets no register and does not affect the state machine	yes
Software Reset	C/I = 0001	Resets the state machine and does not affect the registers	no

The IOM-2 clocks DCL and FSC as well as MCLk are delivered during reset (except for power-on).

The IEC-Q TE provides a low active reset output (pin $\overline{RST}$) which is controlled by a power-on reset and the watchdog timer. The watchdog is enabled by setting the SWST:WT bit to “1”. Default after hardware reset of SWST:WT is "0". Please refer to page 39 for information on how to use the watchdog timer.

Figure 32 illustrates the reset sources that have an impact on pin $\overline{RST}$.

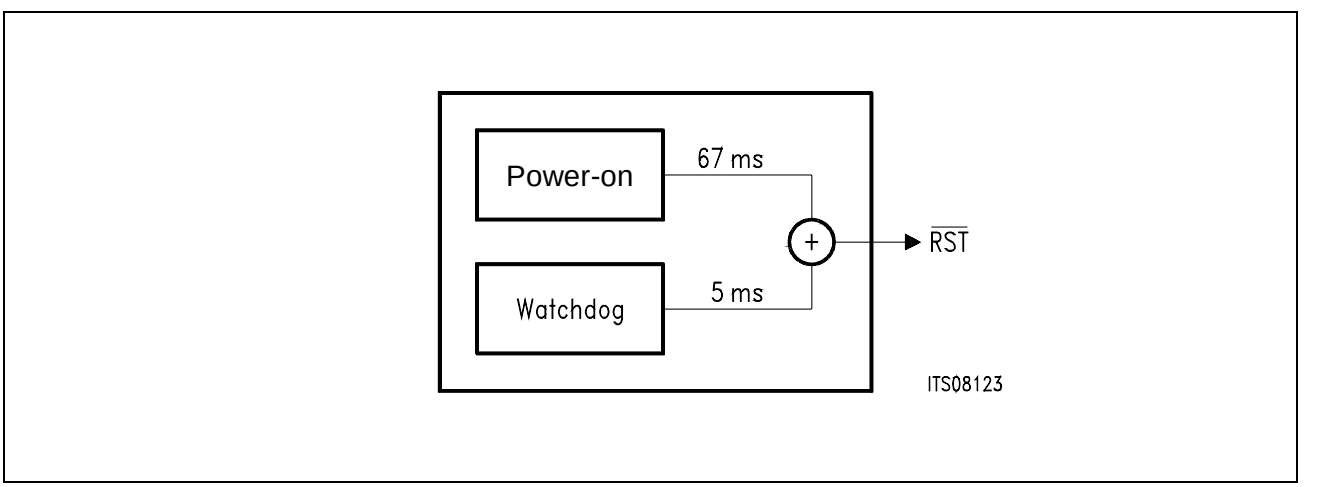


Figure 32 Reset Sources

2.9 Power Controller Interface

Important: This chapter applies only in stand-alone mode.

A power controller interface is implemented in the PSB 21911 to provide comfortable access to peripheral circuits which are not connected directly to the microprocessor . Because this interface was specifically designed to support the ISDN Exchange Power Controller IEPC (PEB 2025) it is referred to as “Power Controller Interface”. Despite this dedication to the IEPC, the controller interface is just as suited for other general-purpose applications.

Interface Bits (PCD, PCA, PCRD, PCWR, INT)

The interface structure is adapted to the register structure of the IEPC. It consists of three data bits PCD0 ... 2, two address bits PCA0,1, read and write signals PCRD and PCWR respectively as well as an interrupt facility INT.

The address bits are latched, they may therefore in general interface applications be used as output lines. For general interface inputs each of the three data bits is suitable. Read and write operations are performed via MON-8 commands. Three inputs and two outputs are thus available to connect external circuitry.

The interrupt pin is edge sensitive. Each change of level at the pin INT will initiate a C/I-code “INT” (0110_B) lasting for four IOM-frames. Interpretation of the interrupt cause and resulting actions need to be performed by the control unit.

Table 21 lists all MON-8- and C/I-commands that are relevant to the power controller interface.

Table 21 MON-8 and C/I-Commands

Channel	Code	Function
MON-8	WCI	Write to interface. Address and data is contained in the MON-command. The address is latched, data is not latched.
MON-8	RCI	Read from interface at specified address. Address is latched and the current value of the data port is read. The result is returned to the user with MON-8 “ACI”.
MON-8	ACI	Answer from interface. After a RCI-request the value of three data bits at the specified address is returned.
C/I	INT	Interrupt. After a change of level has been observed, the C/I-code “INT” is issued for 4 IOM-frames. Note the special timing of the interrupt signals described on page 96.

Communication with the power controller interface is established with local Monitor messages (MON-8) on IOM-2. The following two-byte messages are matched to the IEPC-power controller status register read and write operations but can be used in general, too.

MON-8 **WCI** **Write Controller Interface**

1	0	0	0	0	0	0	0

0	1	1	D0	D1	D2	A0	A1

MON-8 **RCI** **Read Controller Interface**

1	0	0	0	0	0	0	0

0	1	0	–	–	–	A0	A1

MON-8 **ACI** **Answer Controller Interface**

1	0	0	0	0	0	0	0

D0	D1	D2	–	–	–	–	–

After the receipt of a MON-8-command the IEC-Q TE will set the address/data bits and generate a read or write pulse.

The address bits are latched, and the output is stable until it is overwritten by a new dedicated MON-8-command. All data lines are connected to an internal pull-up resistor.

The initial value on the address lines after a soft or hardware reset is (11_B).

Interrupt

For every change at the input pin “INT”, the IEC-Q TE will transmit a C/I-channel code (0110_B), INT, in 4 successive IOM-2-frames. The input condition of the “INT” pin is sampled every 4 IOM-2-frames. An interrupt indication must therefore be applied to pin “INT” for at least 4 IOM-2-frames.

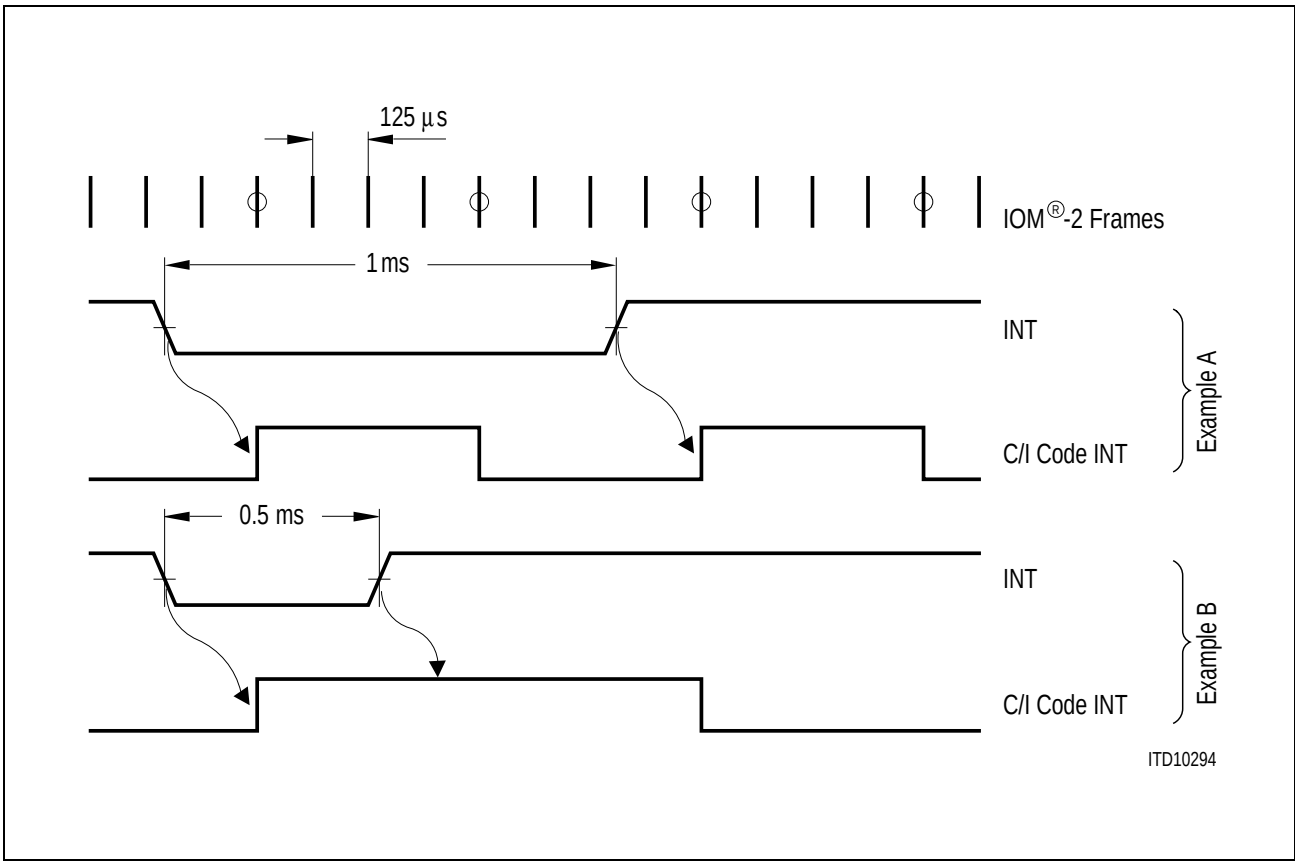


Figure 33 Sampling of Interrupts

3 Operational Description

3.1 C/I Channel Programming

Important: This chapter applies only in µP mode.

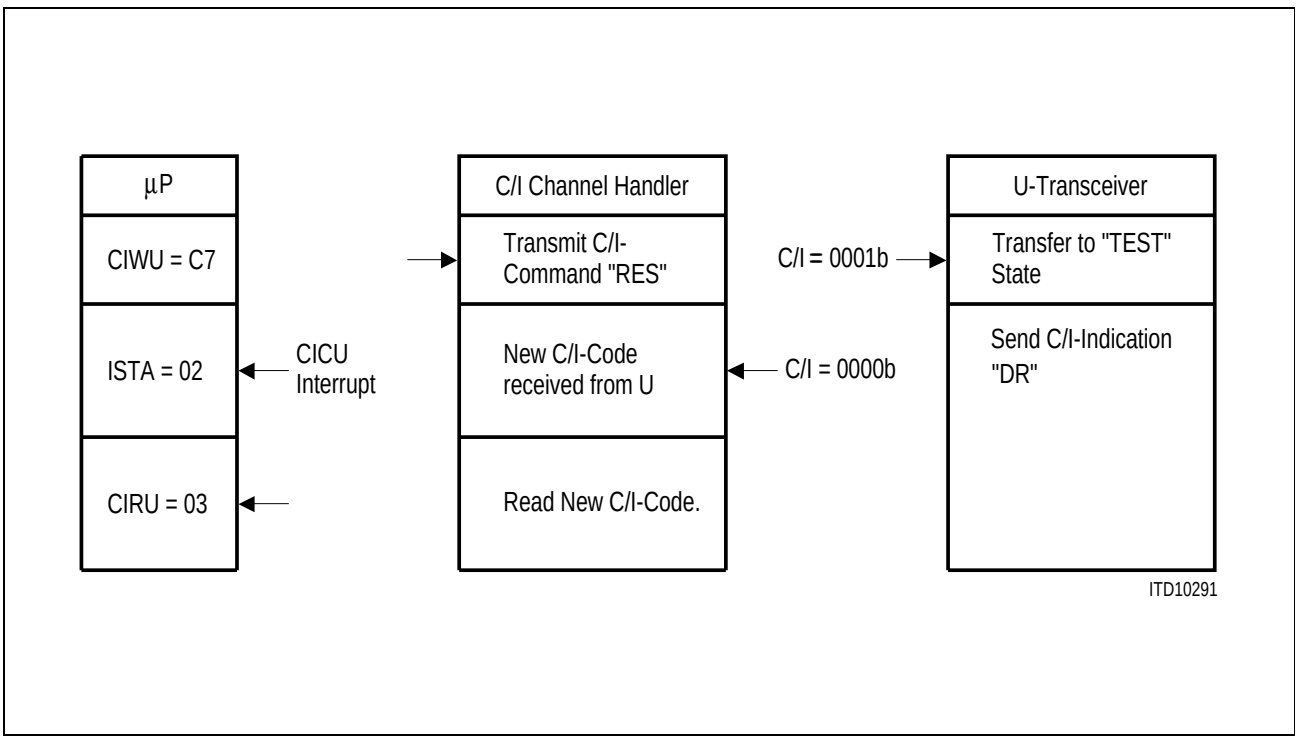


Figure 34 Example: C/I-Channel Use (all data values hexadecimal)

3.2 Monitor Channel Programming

Important: This chapter applies only in µP mode.

The example on **page 99** illustrates the read-out of the transceiver's identification number (ID). It consists of the transmission of a two-byte message from the control unit to the transceiver in IOM channel 0. The transceiver acknowledges the receipt by returning a two-byte long message in the monitor channel. The procedure is absolutely identical for Monitor channel 1.

The µP starts the transfer procedure after having confirmed that the monitor channel is inactive. The first byte of monitor data is loaded into the transmit register MOX. Via the Monitor Control Register MOCR monitor interrupts are enabled and control of the MX-bit is handed over to the IEC-Q TE. Then transmission of the first byte begins. The U-transceiver reacts to a low level of the MX-bit by reading and acknowledging the monitor channel byte automatically. On detection of the confirmation, the IEC-Q TE issues a monitor interrupt to inform the µP that the next byte may be sent. Loading the second byte into the transmit register results in an immediate transmission (timing is controlled by IEC-Q TE). The U-transceiver receives the second byte in the same manner as before. When transmission is completed, the U-transceiver sends "End of Message" (MX-bit high).

It is assumed that a monitor command was sent that needs to be answered by the U-transceiver (e.g. read-out of a register). Therefore, the U-transceiver commences to issue a two-byte confirmation after an End-of-Message indication from the IEC-Q TE has been detected. The IEC-Q TE notifies the µP via interrupt when new monitor data has been received. The processor may then read and acknowledge the byte at a convenient instant. When confirmation has been completed, the U-transceiver sends "EOM". This generates a corresponding interrupt in the IEC-Q TE. By setting the MR-bit to high, the monitor channel is inactive, the transmission is finished.

Example: Monitor Channel Transmission and Reception

Basic Configuration, IOM-2 Clocks must be active

```
w   STCR =  0x15      // TE Mode, EOC Auto Mode
w   SWST =  0x06      // Access to C/I and Monitor channel
w   ADF2 =  0x48      // Monitor access to U-transceiver
```

Transmission

```
r   MOSR =  0x00      // Transmission inactive (MAC = 0)
w   MOX  =  0x80      // Mon-8 Command
w   MOCR =  0x30      // Transmit Command
r   ISTA =  0x01      // Monitor MDA Interrupt
r   MOSR =  0x28      // Ackn. Indication
w   MOXR =  0x00      // Access to Register 0
r   ISTA =  0x01      // Monitor MDA Interrupt
r   MOSR =  0x28      // Ackn. Indication
```

Reception

```
w   MOCR =  0x80      // Enable Receive of Monitor Message
r   ISTA =  0x08      // Monitor MDR Interrupt
r   MOSR =  0x80      // Data Received
r   MOR  =  0x80      // Value read Monitor 8 Command Ind.
w   MOCR =  0xC0      // Acknowledge Reading
r   ISTA =  0x08      // Monitor MDR Interrupt
r   MOSR =  0x80      // Data Received
r   MOR  =  0x03      // Data from Register 0 (Identification)
r   ISTA =  0x08      // Monitor MDR Interrupt
r   MOSR =  0x40      // EOM received
w   MOCR =  0x80      // Enable Interrupts.
```

3.3 Layer 1 Activation/Deactivation

Table 22 shows all U-interface signals as defined by ANSI.

Table 22 U-Interface Signals

Signal	Synch. Word (SW)	Superframe (ISW)	2B + D	M-Bits
NT –> LT				
TN [1)]	± 3	± 3	± 3	± 3
SN0	no signal	no signal	no signal	no signal
SN1	present	absent	1	1
SN2	present	absent	1	1
SN3	present	present	1	normal
SN3T	present	present	normal	normal
LT –> NT				
TL [1)]	± 3	± 3	± 3	± 3
SL0	no signal	no signal	no signal	no signal
SL1	present	absent	1	1
SL2	present	present	0	normal
SL3 [2)]	present	present	0	normal
SL3T	present	present	normal	normal
Test Mode				
SP [3)]	no signal	no signal	± 3	no signal

Notes: [1)] Alternating ± 3 symbols at 10 kHz

[2)] Must be generated by the exchange

[3)] Alternating ± 3 single pulses of 12.5 µs duration spaced by 1.5 ms

Complete Activation Initiated by LT

Figure 35 depicts the procedure if the activation has been initiated by the exchange side.

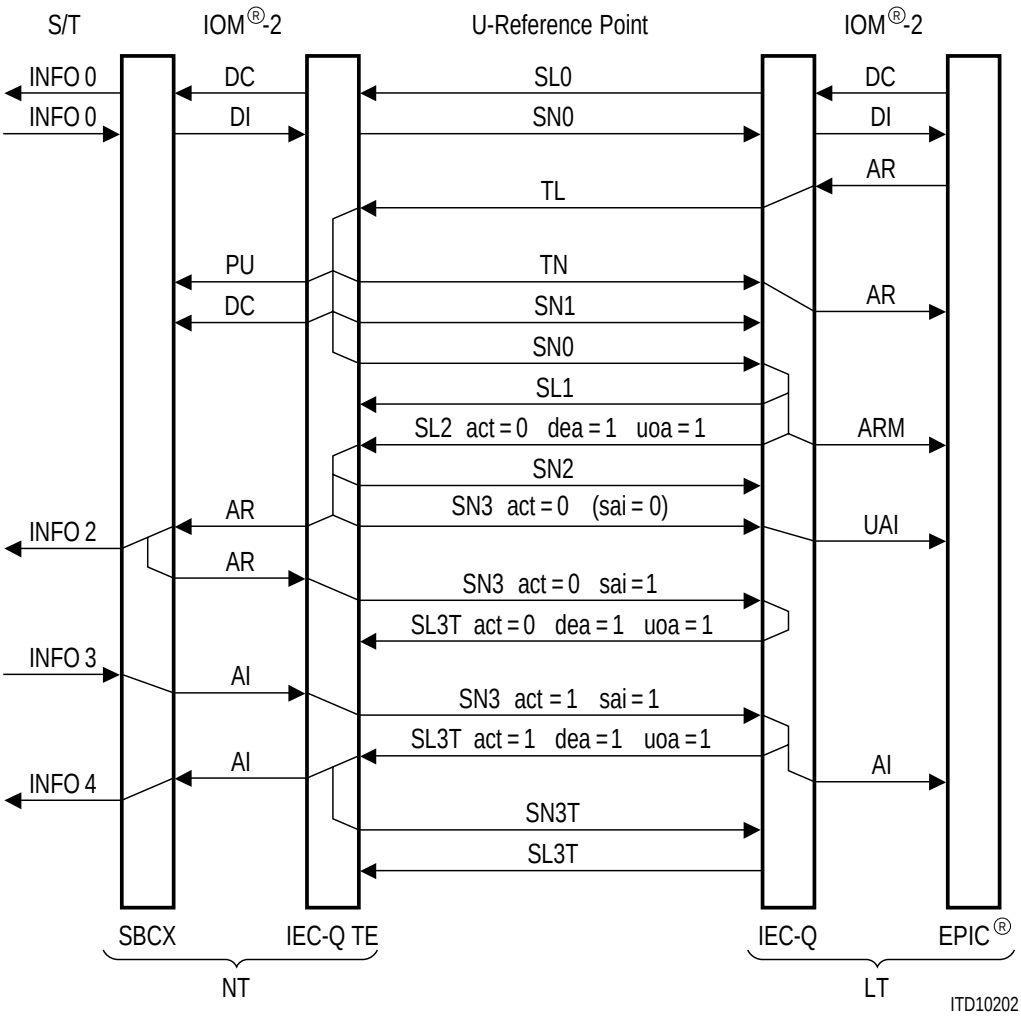


Figure 35 Complete Activation Initiated by LT

Complete Activation Initiated by TE

Figure 36 depicts the procedure if the activation has been initiated by the terminal side.

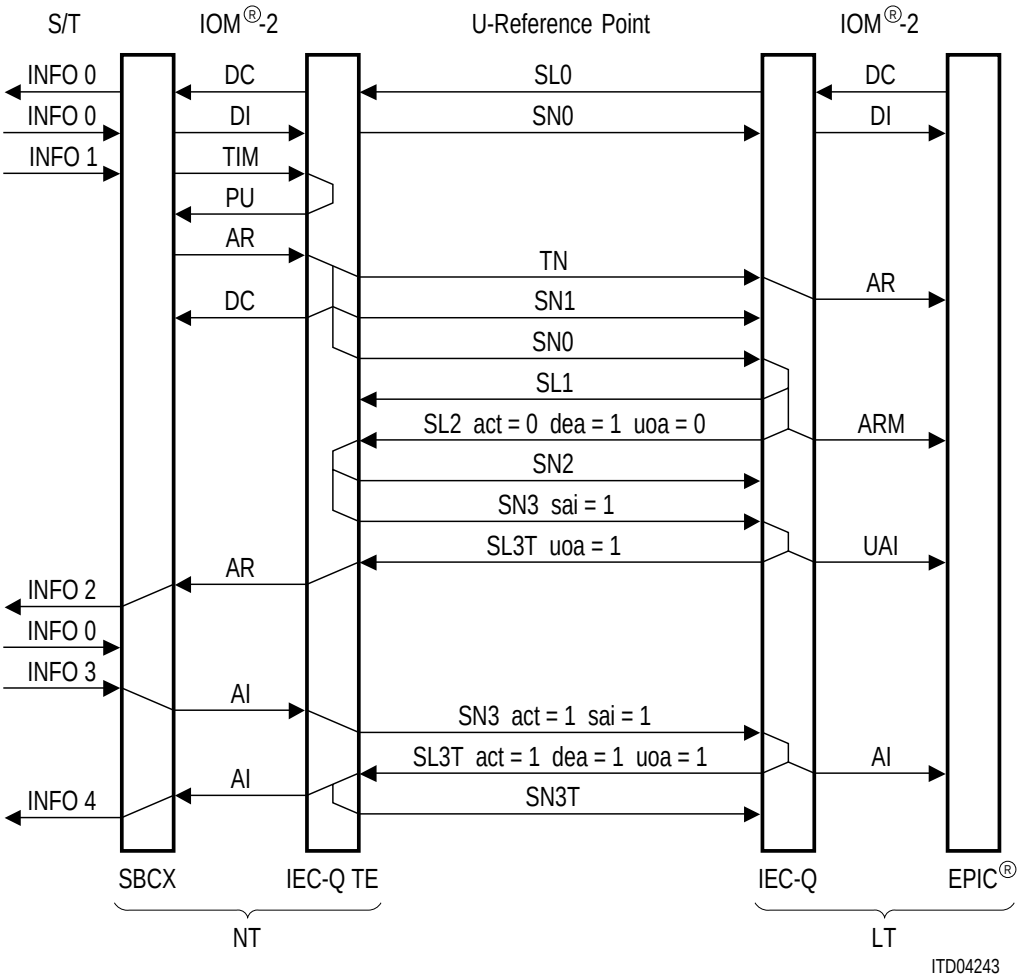


Figure 36 Complete Activation Initiated by TE

Complete Deactivation

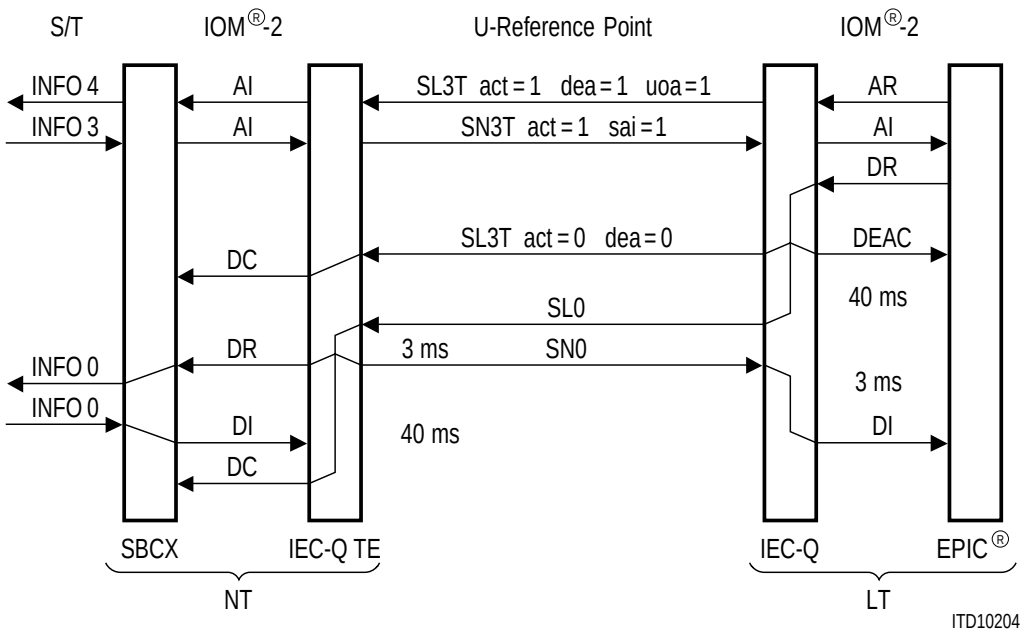


Figure 37 Complete Deactivation

Partial Activation (U Only)

The IEC-Q TE is in the “Synchronized 1” state (see state machine) after a successful partial activation. IOM-2-clocks DCL and FSC are issued. On DOUT the C/I-message “DC” as well as the LT-user data is sent.

While the C/I-messages “DI” (1111_B) or “TIM” (0000_B) are received on DIN, the IEC-Q TE will transmit “SAI” = (0) upstream. Any other code results in “SAI” = (1) to be sent. On the U-interface the signal SN3 (i.e. 2B + D = (1)) will be transmitted continuously regardless of the data on DIN.

The LT will transmit all user data transparently downstream (signal SL3T). In case the last C/I-command applied to DIN was “UAR”, the LT retains activation control when an activation request comes from the terminal (confirmation with C/I = “AR” required, see **page 106 (case 1**). With C/I “DC” applied on DIN, TE initiated activations will be completed without the necessity of an exchange confirmation (**page 107 (case 2)**).

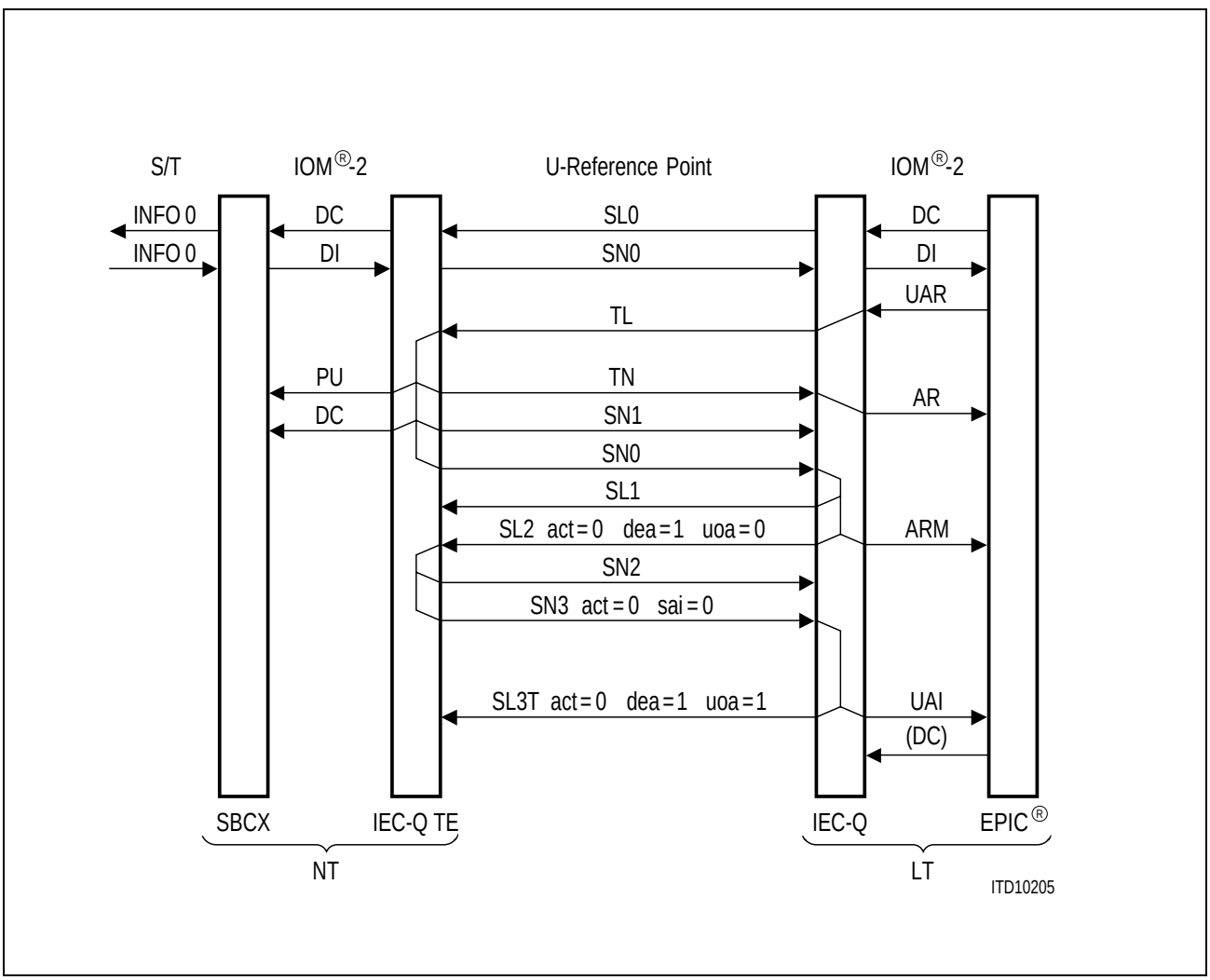


Figure 38 U Only Activation

Activation Initiated by LT with U Active

The S-interface is activated from the exchange with the command “AR”. Bit “UOA” changes to (1) requesting S-interface activation.

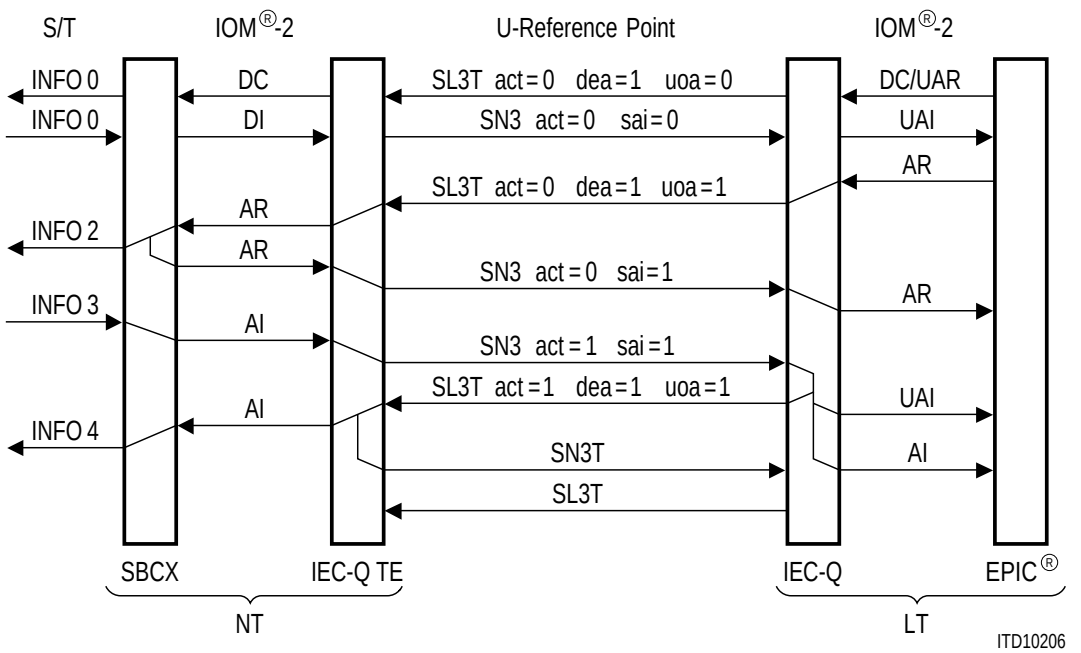


Figure 39 LT Initiated Activation with U-Interface Active

Activation Initiated by TE with U Active

The TE initiates complete activation with INFO 1 leading to “SAI” = (1). Case 1 requires the exchange side to acknowledge the TE-activation by sending C/I = “AR”, Case 2 activates completely without any LT-confirmation.

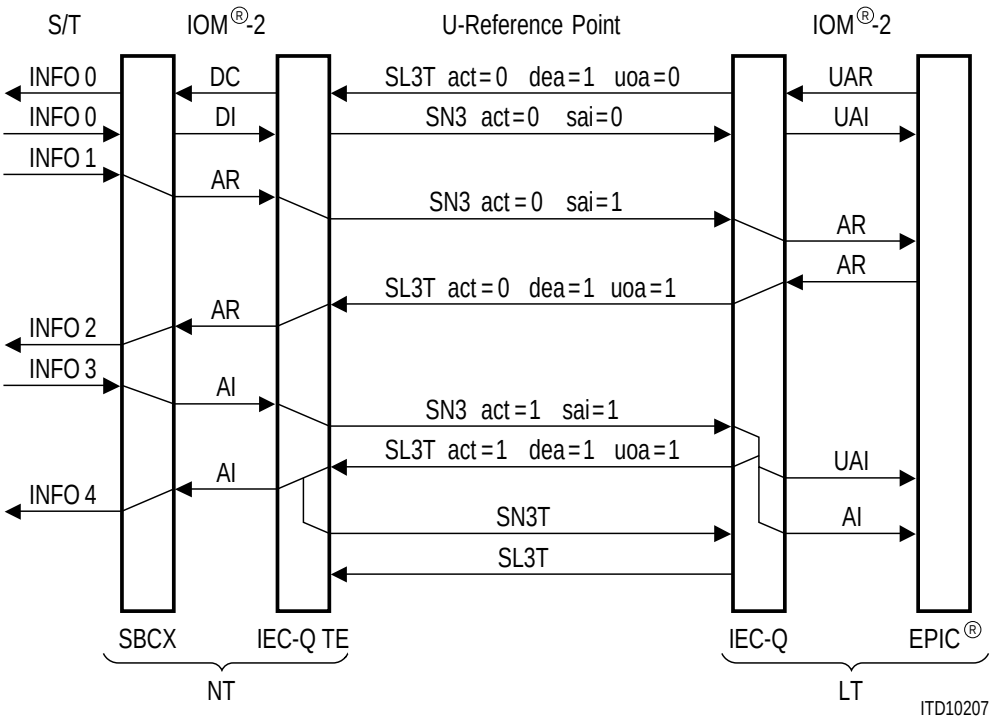


Figure 40 TE-Activation with U Active and Exchange Control (case 1)

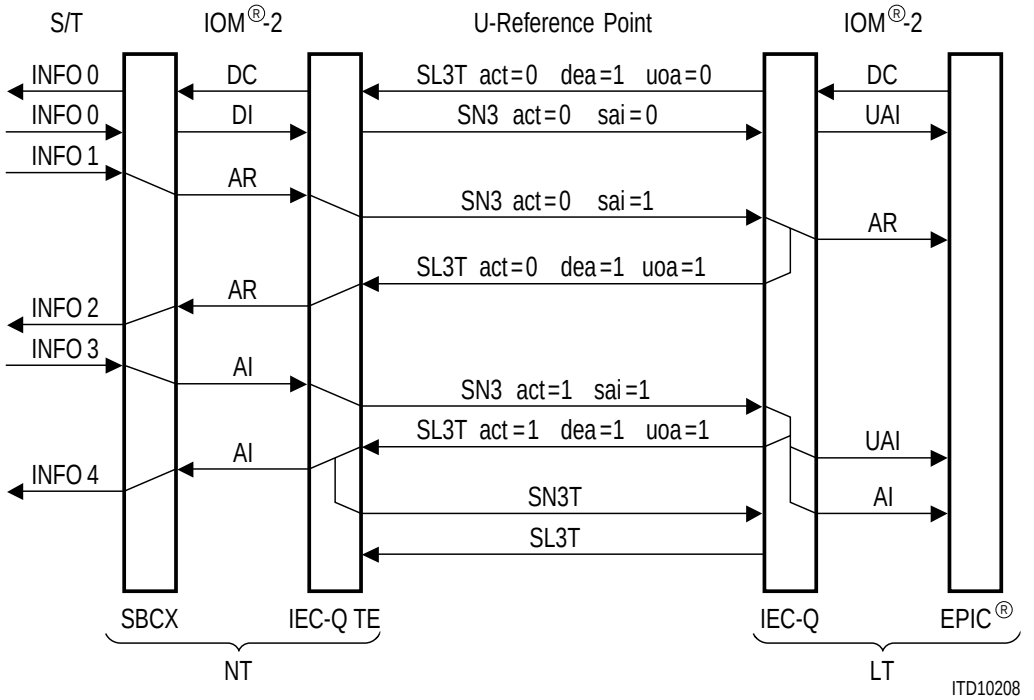


Figure 41 TE-Activation with U Active and no Exchange Control (case 2)

Deactivating S/T-Interface Only

Deactivation of the S-interface only is initiated from the exchange by setting the “UOA” bit = (0).

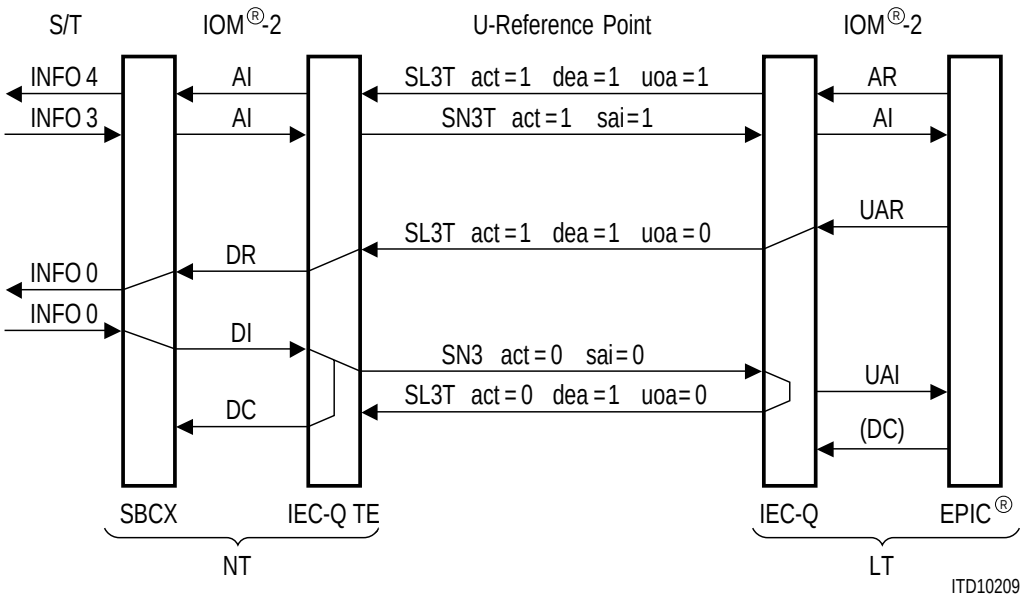


Figure 42 Deactivation of S/T Only

3.4 External Circuitry

3.4.1 Power Supply Blocking Recommendation

The following blocking circuitry is suggested.

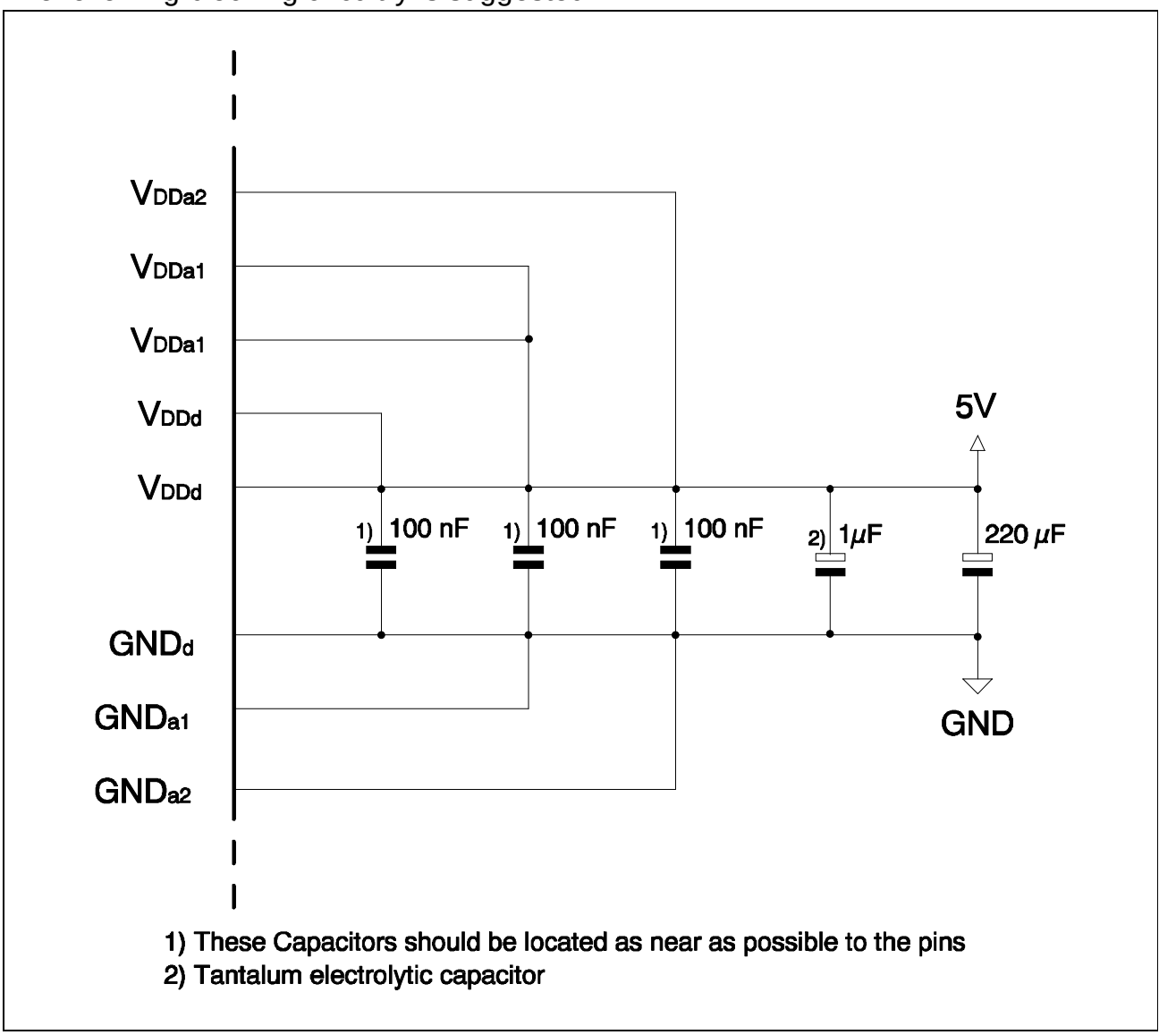


Figure 43 Power Supply Blocking

3.4.2 U-Interface

The hybrid suggested for the PSB 21911 IEC-Q TE is identical to the hybrid recommended for the PEB 2091 IEC-Q.

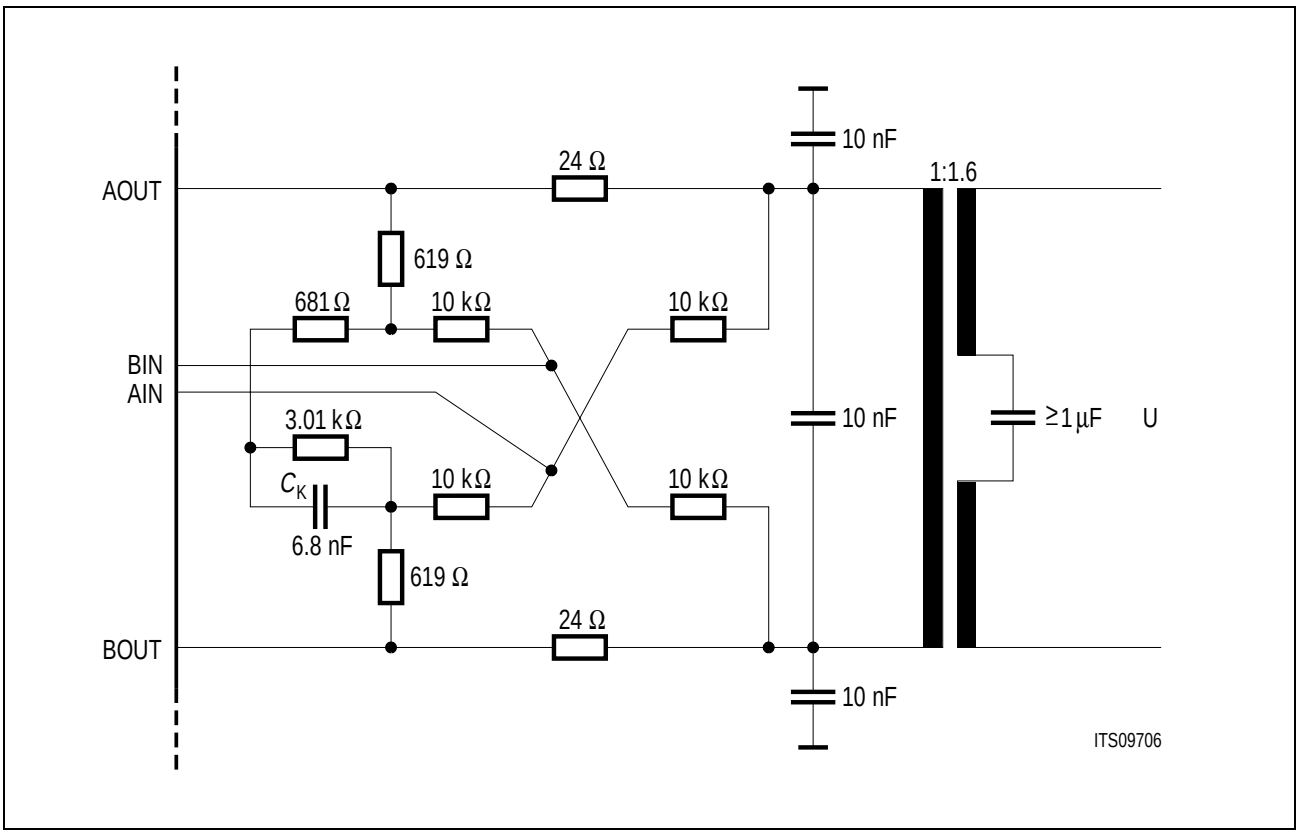


Figure 44 U-Interface Hybrid Circuit

Note: To achieve optimum performance all capacitors of the hybrid should be MKT. Ceramic capacitors are not recommended.

3.4.3 Oscillator Circuit

Figure 45 illustrates the recommended oscillator circuit. A crystal or an oszillator signal may be used.

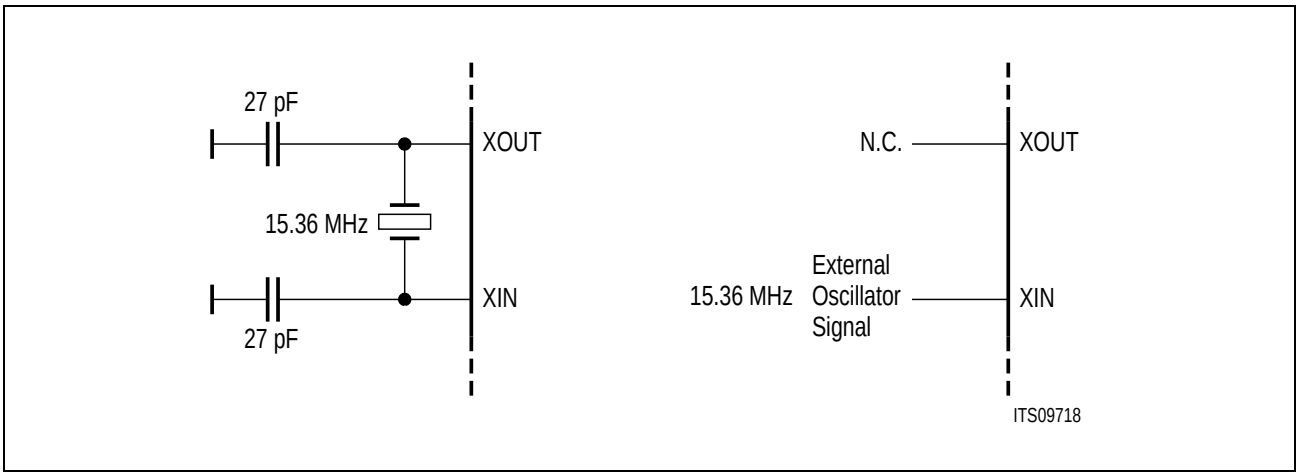


Figure 45 Crystal Oscillator or External Clock Source

Crystal Parameters

Frequency:	15.36 MHz
Load capacitance:	20 pF +/- 0.3pF
Frequency tolerance:	60 ppm
Resonance resistance:	20 Ω
Max. shunt capacitance:	7 pF
Oszillator mode:	fundamental

External Oscillator

Frequency:	15.36 MHz
Frequency tolerance:	80 ppm

4 Register Description

Important: This chapter applies only in µP mode.

The setting of the IEC-Q TE in µP mode and the transfer of data is programmed with registers. The address map and a register summary are given in **table 23** and in **table 24,** respectively:

Table 23 Register Address Map

Address (hex)	Read		Write	
	Name	**Description**	**Name**	**Description**
0	ISTA	Interrupt Status Register	MASK	Interrupt Mask register
1			STCR	Status Control Register
2	MOR	Read Monitor data	MOX	Write Monitor data
3	DRU	Read D from U	DWU	Write D to U
4			ADF2	Additional Features Reg. 2
5	reserved for the test mode (must not be used in normal operation)			
6	RB1U	Read B1 from U	WB1U	Write B1 to U
7	RB2U	Read B2 from U	WB2U	Write B2 to U
8	RB1I	Read B1 from IOM-2	WB1I	Write B1 to IOM-2
9	RB2I	Read B2 from IOM-2	WB2I	Write B2 to IOM-2
A	MOSR	Monitor Status Register	MOCR	Monitor Control Register
B	DRI	Read D from IOM-2	DWI	Write D to IOM-2
C	CIRU	Read C/I-code from U	CIWU	Write C/I-code to U
D	CIRI	Read C/I-code from IOM-2	CIWI	Write C/I-code to IOM-2
E			ADF	Additional Features Reg.
F			SWST	Switch Status Register

Table 24 Register Summary

Address	7	6	5	4	3	2	1	0	Name	
0_H	D	CICI	CICU	SF	MDR	B1	B2	MDA	ISTA	R
0_H	D	CICI	CICU	SF	MDR	B1	B2	MDA	MASK	W
1_H	TEST1	TEST2	MS2	MS1	MS0	TM1	TM2	AUTO	STCR	W
2_H									MOR	R
2_H									MOX	W
3_H									DRU	R
3_H									DWU	W
4_H	TE1	MTO	DOD		MIN				ADF2	W
6_H									RB1U	R
6_H									WB1U	W
7_H									RB2U	R
7_H									WB2U	W
8_H									RB1I	R
8_H									WB1I	W
9_H									RB2I	R
9_H									WB2I	W
A_H	MDR	MER	MDA	MAB	MAC				MOSR	R
A_H	MRE	MRC	MXE	MXC					MOCR	W
B_H									DRI	R
B_H									DWI	W
C_H	0	0	C/I	C/I	C/I	C/I	1	1	CIRU	R
C_H	1	1	C/I	C/I	C/I	C/I	1	1	CIWU	W
D_H	C/I	C/I	C/I	C/I	C/I	C/I	1	1	CIRI	R
D_H	C/I	C/I	C/I	C/I	C/I	C/I	1	1	CIWI	W
E_H	WTC2	WTC1	PCL1	PCL0			BCL	CBAC	ADF	W
F_H	WT	B1	B2	D	CI	MON	BS	SGL	SWST	W

4.1 Interrupt Structure

The cause of an intrerrupt is determinded by reading the Interrupt Status Register (ISTA). In this register, 7 interrupt sources can be directly read. Interrupt bits are cleared by reading the corresponding registers. ISTA:D is cleared after DRI and DRU have been read. ISTA:B1 is cleared after RB1I and RB1U have been read. ISTA:B2 is cleared after RB2I and RB2U have been read etc. ISTA:CICI is cleared after CIRI is read, ISTA:CICU is cleared after CIRU is read. ISTA:SF indicates a superframe marker received from the U-interface. It is cleared when the ISTA register has been read. Pin $\overline{INT}$ is set to "0" if one bit of ISTA changes from "0" to "1", except for the bit masked in the MASK register. The MASK register allows to prevent an interrupt to actually influence the $\overline{INT}$ pin. Setting the bits of MASK that correspond to the bits of ISTA to "1" masks the bits, that is, the bits are still set in ISTA, but they do not contribute to the input of the NOR-function on the interrupt bits which sets the $\overline{INT}$ pin. The interrupt structure is illustrated in **figure 46**:

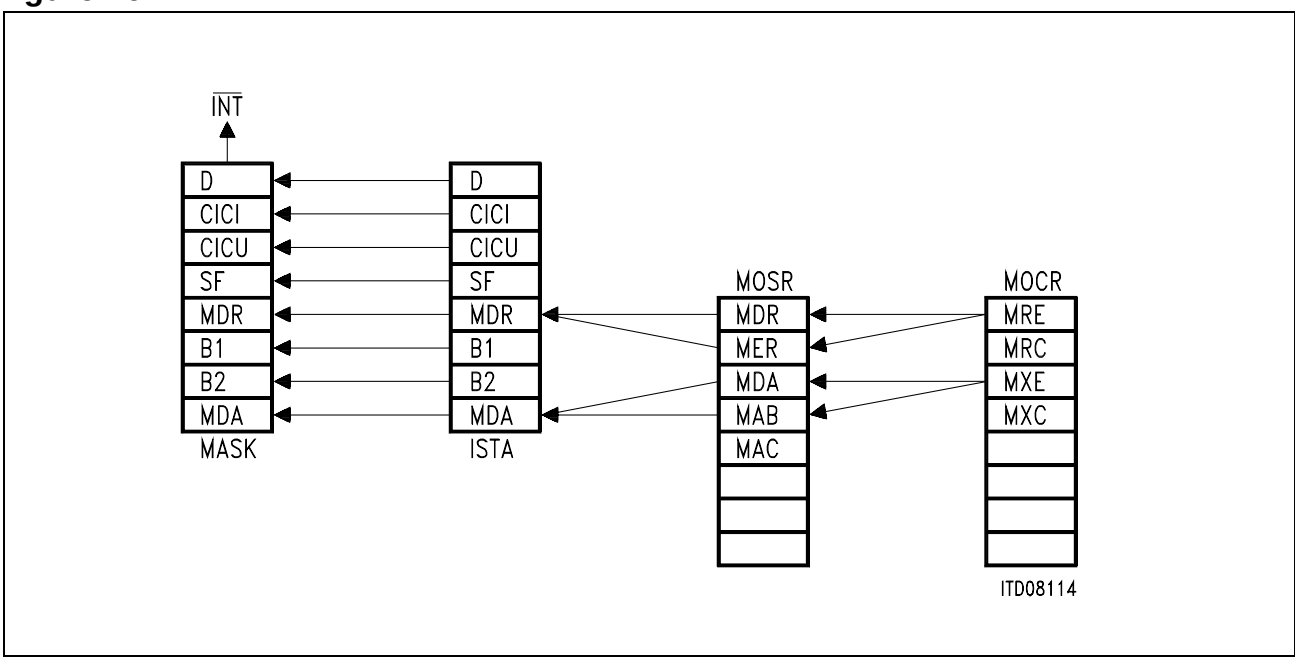


Figure 46 Interrupt Structure

4.1.1 Monitor-Channel Interrupt Logic

The Monitor Data Receive (MDR) and the Monitor End of Reception (MER) interrupt status bits have two enable bits, Monitor Receive Interrupt Enable (MRE) and MR-bit Control (MRC). The Monitor channel Data Acknowledged (MDA) and Monitor channel Data Abort (MAB) interrupt status bits have a common enable bit Monitor Interrupt Enable (MXE).

MRE prevents the occurrence of the MDR status, including when the first byte of a packet is received. When MRE is active ("1") but MRC is inactive, the MDR interrupt status is generated only for the first byte of a receive packet. When both MRE and MRC are active, MDR is generated and all received Monitor bytes - marked by a low edge in MX bit - are stored. Additionally, an active MRC enables the control of the MR handshake bit according to the Monitor channel protocol.

4.2 Registers

ISTA-Register **Read** **Address 0_H**

The Interrupt Status Register (ISTA) generates an interrupt for the selected channel. Interrupt bits are cleared by reading the corresponding register.

Default: 00_H

7							0	
D	CICI	CICU	SF	MDR	B1	B2	MDA	0_H

D: D-channel Interrupt

D = 1 indicates an interrupt that 8 bits D-channel data have been updated.

D = 0 occurs after DRI and DRU have been read.

CICI: C/I-channel Interrupt

CICI = 1 indicates a change in the C/I-channel on IOM-2.

CICI = 0 occurs after CIRI is read.

CICU: C/I-channel Interrupt

CICU = 1 indicates a change in the C/I-channel coming from the U-interface.

CICU = 0 occurs after CIRU is read.

SF: Superframe Marker

SF = 1 indicates a superframe marker received from the U-interface.

SF = 0 occurs when the ISTA-Register has been read.

MDR: Monitor Data Receive Interrupt

MDR = 1 indicates an interrupt after the MOSR:MDR or the MOSR:MER bits have been activated.

MDR = 0 indicates the inactive interrupt status.

B1: B1-channel Interrupt

B1 = 1 indicates an interrupt every time B1-channel bytes arrive.

B1 = 0 occurs after RB1I and RB1U have been read.

B2: B2-channel Interrupt

B2 = 1 indicates an interrupt every time B2-channel bytes arrive.

B2 = 0 occurs after RB2I and RB2U have been read.

MDA: Monitor Data Transmit Interrupt

MDA = 1 indicates an interrupt after the MOSR:MDA or the MOSR:MAB bits have been activated.

MDA = 0 indicates the inactive interrupt status.

MASK-Register **Write** **Address 0_H**

The Interrupt Mask Register (MASK) can selectively mask each interrupt source in the ISTA register by setting to "1" the corresponding bit.

Default: FF_H

7							0	
D	CICI	CICU	SF	MDR	B1	B2	MDA	0_H

D: D-channel mask

D = 1 prevents an interrupt ISTA:D to actually influence the $\overline{INT}$ pin.

D = 0 disables the function described above.

CICI: CICI-channel mask

CICI = 1 prevents an interrupt ISTA:CICI to actually influence the $\overline{INT}$ pin.

CICI = 0 disables the function described above.

CICU: CICU-channel mask

CICU = 1 prevents an interrupt ISTA:CICU to actually influence the $\overline{INT}$ pin.

CICU = 0 disables the function described above.

SF: Superframe marker mask

SF = 1 prevents an interrupt ISTA:SF to actually influence the $\overline{INT}$ pin.

SF = 0 disables the function described above.

MDR: Monitor data receive mask

MDR = 1 prevents an interrupt ISTA:MDR to actually influence the $\overline{\text{INT}}$ pin.

MDR = 0 disables the function described above.

B1: B1-channel mask

B1 = 1 prevents an interrupt ISTA:B1 to actually influence the $\overline{\text{INT}}$ pin.

B1 = 0 disables the function described above.

B2: B2-channel mask

B2 = 1 prevents an interrupt ISTA:B2 to actually influence the $\overline{\text{INT}}$ pin.

B2 = 0 disables the function described above.

MDA: Monitor data transmit mask

MDA = 1 prevents an interrupt ISTA:MDA to actually influence the $\overline{\text{INT}}$ pin.

MDA = 0 disables the function described above.

STCR-Register **Write** **Address 1_H**

The Status Control Register (STCR) selects the operating modes of the IEC-Q TE as given in table.

Default: 04_H

7							0	
0	0	MS2	MS1	MS0	TM1	TM2	AUTO	1_H

Bit 7: reserved
Set to '0' for future compatibility.

Bit 6: reserved
Set to '0' for future compatibility.

MS2: Mode Selection 2
Selects operation mode according to the table below.

MS1: Mode Selection 2
Selects operation mode according to the table below.

MS0: Mode Selection 2
Selects operation mode according to the table below.

	Mode Selection			**Output Pins U Synchronized**		
Mode	**Bit MS2**	**Bit MS1**	**Bit MS0**	**DCL OUT**	**CLS OUT**	**Super-frame-marker**
NT	0	0	0	512	7680	no
NT	1	0	0	512	7680	yes
NT-Auto	0	0	1	512	7680	no
TE	0	1	0	1536	7680	no
TE	1	1	0	1536	7680	yes
reserved	others					

TM1: Test-Mode-Bit 1

This bit determines, in combination with STCR:TM2, the operation modes. See table below.

TM2: Test-Mode-Bit 2

This bit determines, in combination with STCR:TM1, the operation modes. See table below.

Test-Mode	TM1	TM2
Normal Mode	1	0
Send Single-Pulses	1	1
Data-Through	0	1

AUTO: Selection between auto- and transparent mode

AUTO = 1 sets the automode for EOC channel processing.

AUTO = 0 sets the transparent mode for EOC channel processing.

Note: The STCR-register is only reset after a power-on. Please refer also to table 20 on page 93.

ADF2-Register **Write** **Address 4_H**

Additional Features Register 2 (ADF2).

Default: 08_H

7							0	
TE1	MTO	DOD		MIN				4_H

TE1: Terminal Equipment Channel 1

TE1 = 1 enables the IEC-Q TE to write Monitor data on DOUT to the MON1 channel instead of the MON0 channel and to write 6-bit C/I indications on DOUT into the C/I-channel 1.

TE1 = 0 enables the normal TE operations where the IEC-Q TE addresses only IOM-2 channel 0.

MTO: Monitor Procedure Timeout

MTO = 1 disables the internal 6ms Monitor timeout.

MTO = 0 enables the internal 6ms Monitor timeout.

DOD: Dout Open Drain

DOD = 1 selects pin DOUT to be open drain.

DOD = 0 selects pin DOUT to be tristate.

MIN: Monitor-In-Bit

MIN = 1 combined with the SWST:MON = “1“ and ADF2:TE1 = “0“ bits, enables the controller to access the core of the IEC-Q TE.

MIN = 0 combined with the SWST:MON = “1“ and ADF2:TE1 = “0“ bits, enables the controller to access the IOM-2 interface directed out of the IEC-Q TE (see also page 85).

MOSR-Register **Read** **Address A_H**

The Monitor Status Register (MOSR) indicates the status of the Monitor channel.

Default: 00_H

7							0	
MDR	MER	MDA	MAB	MAC				A_H

MDR: Monitor Channel Data Received Interrupt

MDR = 1 generates an interrupt status after the receiving device has stored the contents of the MOX register in the MOR register.

MDR = 0 inactive interrupt status

MER: Monitor Channel End of Reception Interrupt

MER = 1 is generated after two consecutive inactive MX bits (end of message) or as a result of a handshake procedure error.

MER = 0 indicates that the transmission is running.

MDA: Monitor Channel Data Acknowledged

MDA = 1 results after a Monitor byte is acknowledged by the receiving device.

MDA = 0 occurs when the receiver waits for an acknowledge of the Monitor bit.

MAB: Monitor Channel Data Abort

MAB = 1 indicates that during a transmission the receiver aborted the process by sending an inactive (“1“) MR bit value in two consecutive frames.

MAB = 0 indicates that the transmission is running properly and that no abort request has been activated.

MAC: Monitor Channel Active

MAC = 1 indicates a transmission on the Monitor channel.

MAC = 0 indicates that the transmitter is inactive, i.e. ready for a transmission.

MOCR-Register **Write** **Address A_H**

The Monitor Control Register (MOCR) allows to program and control the Monitor channel as described in the section 4.1.1.

Default: 00_H

7							0	
MRE	MRC	MXE	MXC					A_H

MRE: Monitor Receive Interrupt Enable

MRE = 1 enables the Monitor data receive (MDR) interrupt status bit; MRE = 1 enables the Monitor data receive (MDR) and the Monitor end of reception (MER) interrupt status bits.

MRE = 0 masks the MDR and the MER bits.

MRC: Monitor Channel Receive Control

MRC = 1 enables the control of the MR bit internally by the IEC-Q TE according to the Monitor channel protocol.

MRC = 0 enforces a “1“ (inactive state) in the Monitor channel receive (MR) bit.

MXE: Monitor Transmit Interrupt Enable

MXE = 1 combined with the MXC bit tied to “1“ enable the Monitor channel data acknowledged (MDA) and the Monitor channel data abort (MAB) interrupt status bits.

MXE = 0 masks the MDA and the MAB bits.

MXC: Monitor Channel Transmit Control

MXC = 1 enables the control of the MX bit internally by the IEC-Q TE according to the Monitor channel protocol.

MXC = 0 enforces a “1“ (inactive state) in the Monitor channel transmit (MX) bit.

CIRU-Register **Read** **Address C_H**

The Read C/I-code from U Register (CIRU) reads the C/I-code from the U-transceiver.

Default: 03_H

7							0	
0	0	C/I	C/I	C/I	C/I	1	1	C_H

7., 6. bits: Set to “0“.

5.-2. bits: Contain the C/I-indication coming from the U-transceiver.

1., 0. bits: Set to “1“.

CIWU-Register **Write** **Address C_H**

The Write C/I-code to U Register (CIWU) writes the C/I-code to the U-transceiver.

Default: $C3_H$

7							0	
1	1	C/I	C/I	C/I	C/I	1	1	C_H

7., 6. bits: Set to “1“.

5.-2. bits: Contain the C/I-code going to the U-transceiver.

1., 0. bits: Set to “1“.

CIRI-Register **Read** **Address D_H**

The Read C/I-code from IOM-2 Register (CIRI) reads the C/I-code from the IOM-2 interface.

Default: 03_H

7							0	
C/I	C/I	C/I	C/I	C/I	C/I	1	1	D_H

7., 6. bits: ADF2:TE1 = 1 indicates that the C/I-channel 1 in the TE mode can be accessed and that the C/I-channel on IOM-channel 0 is passed transparently from the IEC-Q TE to the IOM-2. The two bits contain C/I-code.

ADF:TE1 = 0 sets the normal mode. The two bits are set to “0“.

5.-2. bits: Contain the C/I-command coming from the IOM-2.

1., 0. bits: Set to “1“.

CIWI-Register **Write** **Address D_H**

The Write C/I-code to IOM-2 Register (CIWI) writes the C/I-code to the IOM-2 interface.

Default: $C7_H$

7							0	
C/I	C/I	C/I	C/I	C/I	C/I	1	1	D_H

7., 6. bits: These bits are the MSBs of the 6-bit wide C/I code in IOM-2 channel 1 if ADF2:TE1 = 1.

If ADF2:TE1 = 0 these two bits have no effect. They should however be set to 1 for future compatibility.

5.-2. bits: Contain the C/I-code going to the IOM-2.

1., 0. bits: Set to “1.

ADF-Register **Write** **Address E_H**

Additional Features Register (ADF).

Default: 14_H

7							0	
WTC2	WTC1	PCL1	PCL0			BCL	CBAC	E_H

WTC2, **WTC1:** Watchdog Controller

The bit patterns “10“ and “01“ has to be written in WTC1 and WTC2 by the enabled watchdog timer within 132ms. If it fails to do so, a reset signal of 5ms at pin $\overline{RST}$ is generated.

PCL1, **PCL0:** Prescaler

The clock frequency on MCLK is selected by setting the bits according to the table below:

PCL1	PCL0	Frequency at MCLK (MHz)
0	0	7.68
0	I	3.84
I	0	1.92
I	I	0.96

Bit 2: Reserved

Set to 0 for future compatibility.

BCL: Bit Clock

BCL = 1 changes the DCL-output into the bit-clock-mode.

BCL = 0 gives the doubled bit clock on the DCL-output.

CBAC: Control BAC

Operates in combination with SWST:SGL and SWST:BS bits to control the S/G bit and the BAC bit. For the functional description see **Table 18 on page 89**.

SWST-Register **Write** **Address F_H**

The Switch Status Register (SWST) selects the switching directions of the processor interface (PI).

Default: 00_H

7							0	
WT	B1	B2	D	CI	MON	BS	SGL	F_H

WT: Watchdog Timer

WT = 1 enables the watchdog timer (page 39).

WT= 0 disables the watchdog timer.

B1: B1-channel processing

B1 = 1 enables the microprocessor to access B1-channel data between IOM-2 and the U-interface.

B1 = 0 disables the function described above.

B2: B2-channel processing

B2 = 1 enables the microprocessor to access B2-channel data between IOM-2 and the U-interface.

B2 = 0 disables the function described above.

D: D-channel processing

D = 1 enables the microprocessor to access D-channel data between IOM-2 and U-interface.

D = 0 disables the function described above.

CI: C/I-channel processing

CI = 1 enables the microprocessor to access C/I-commands and indications between IOM-2 and U-interface.

CI = 0 disables the function described above.

MON: Monitor-channel processing

MON = 1 enables the microprocessor to access Monitor-channel messages at IOM-2 and at the U-interface.

MON = 0 disables the function described above.

BS: BS bit

Operates in combination with SWST:SGL and ADF:CBAC bits to control the S/G bit and the BAC bit. For the functional description see **Table 18 on page 89**.

SGL: Stop/Go

Operates in combination with SWST:BS and ADF:CBAC bits to control the S/G bit and the BAC bit. For the functional description see **Table 18 on page 89**.

B-Channel Access Registers

Register	Value after reset (hex)	Function	Address (hex)
WB1U	00	write B1-channel data to U-interface	6
RB1U	00	read B1-channel data from U-interface	6
WB1I	00	write B1-channel data to IOM-2	8
RB1I	00	read B1-channel data from IOM-2	8
WB2U	00	write B2-channel data to U-interface	7
RB2U	00	read B2-channel data from U-interface	7
WB2I	00	write B2-channel data to IOM-2	9
RB2I	00	read B2-channel data from IOM-2	9

D-Channel Access Registers

Register	Value after reset (hex)	Function	Address (hex)
DWU	FF	write D-channel data to U-interface	3
DRU	FF	read D-channel data from U-interface	3
DWI	FF	write D-channel data to IOM-2	B
DRI	FF	read D-channel data from IOM-2	B

Monitor-Channel Access Registers

Register	Value after reset (hex)	Function	Address (hex)
MOX	FF	Monitor data transmit register	2
MOR	FF	Monitor data receive register	2

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_{DD}	$-0.3 < V_{DD} < 7.0$	V
Input voltage	V_I	$-0.3 < V_I < V_{DD} + 0.3$ (max. 7)	V
Output voltage	V_O	$-0.3 < V_O < V_{DD} + 0.3$ (max 7)	V
Max. voltage applied at U-Interface	V_S	$-0.3 < V_S < V_{DD} + 0.3$ (max. 7)	V
Max. voltage between GNDA1 (GNDA2) and GNDD	V_S	$\pm$ 250	mV
Storage temperature	T_{stg}	– 65 to 125	°C
Ambient temperature PSB 21911 PSF 21911	 T_A T_A	 0 to 70 – 40 to 85	 °C °C
Thermal resistance (system-air) (system-case)	 $R_{th\ SA}$ $R_{th\ SC}$	 40 9	 K/W K/W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may affect device reliability.
This is a stress rating only and functional operation of the device under those conditions or at any other condition beyond those indicated in the operational conditions of this specification is not implied.
It is not implied, that more than one of those conditions can be applied simultaneously.

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse as outlined in the following figure.

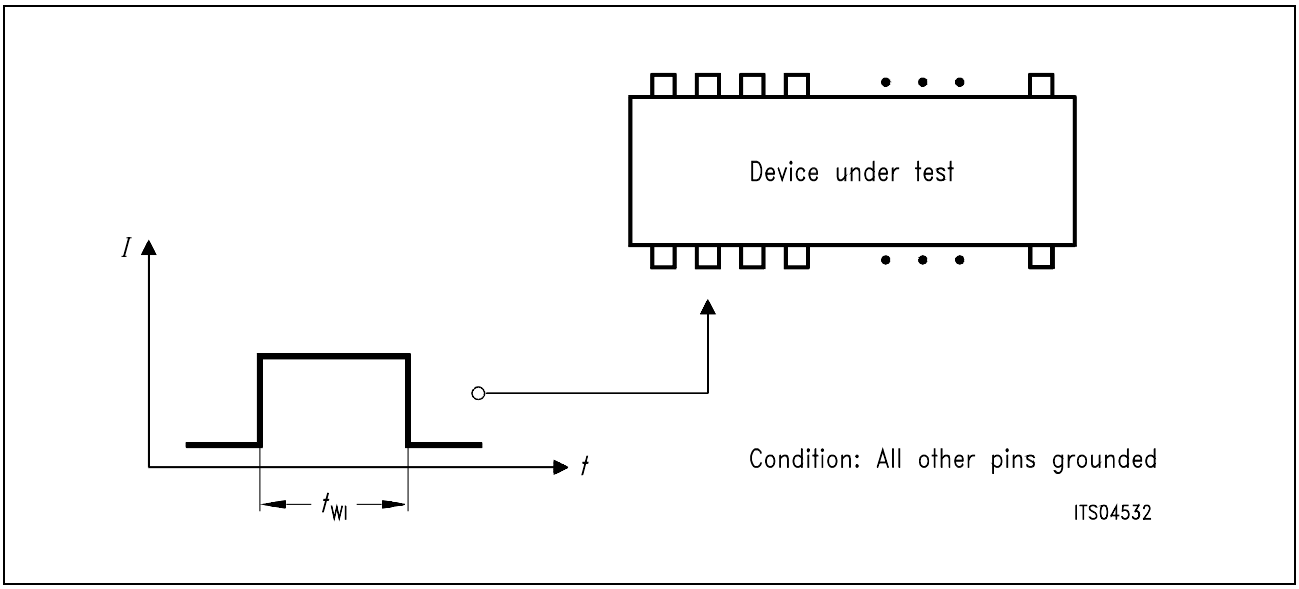


Figure 47 Test Condition for Maximum Input Current

U-Transceiver Input Current

The destruction limits for AOUT, BOUT, AIN and BIN are given in **Figure 48**.

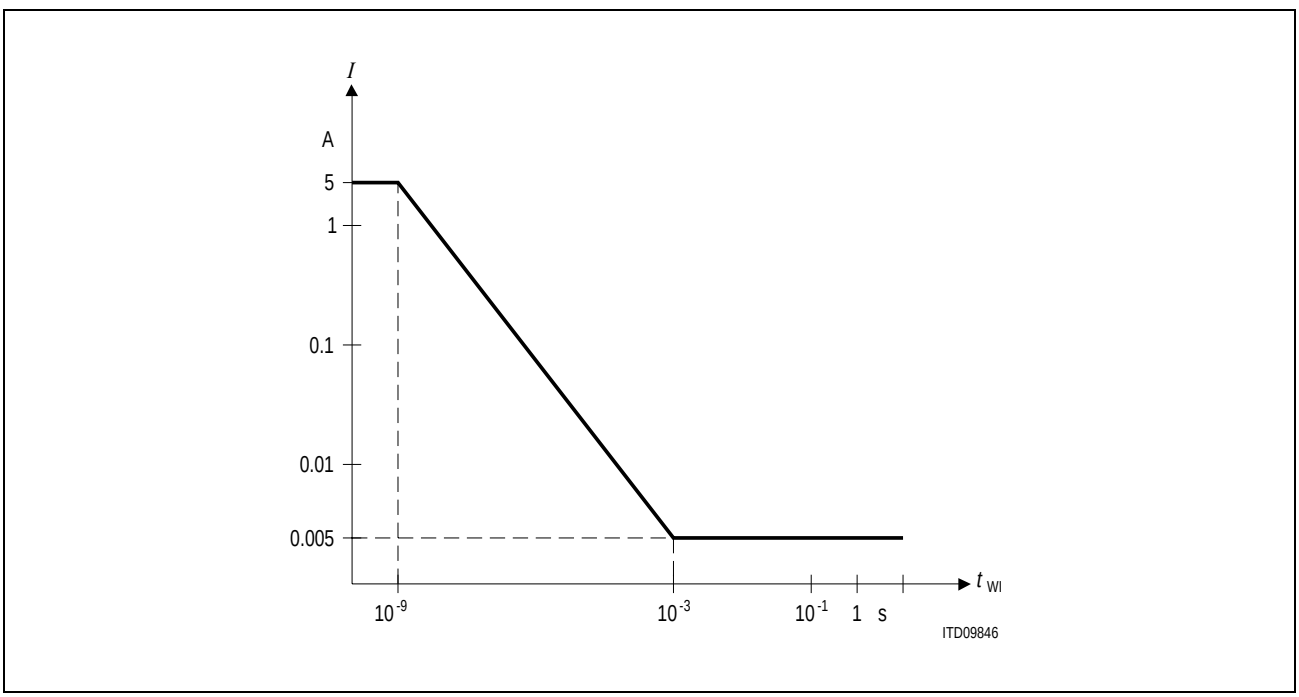


Figure 48 U-Transceiver Input Current

5.2 Power Consumption

All measurements with random 2B + D data in active states.

Mode	Test Conditions	Limit Values		Unit
		typ.	max.	
Power up	5.00 V, open outputs 98 Ω load at AOUT/BOUT	53	59	mA
NT-Power down	5.00 V, open outputs 98 Ω load at AOUT/BOUT Temperature ≥ 0°C	4.7	9	mA
	5.00 V, open outputs 98 Ω load at AOUT/BOUT Temperature < 0°C	6.5	11	mA

5.3 DC Characteristics

VDD = 4.75 to 5.25 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
H-level input voltage	V_{IH}	2.0	V_{DD} + 0.3	V	
L-level input voltage	V_{IL}		0.8	V	
L-level input leakage current for all pins except for PIN #11, #14, #15	I_{IL}	– 10		µA	V_I = GNDd[1)]
H-level input leakage current for all pins except for PIN #11, #14, #15	I_{IH}		10	µA	V_I = VDDd[1)]
L-level input leakage current of PIN #11 (XIN)	I_{IL}	– 40		µA	V_I = GNDd[1)]
H-level input leakage current of PIN #11 (XIN)	I_{IH}		40	µA	V_I = VDDd[1)]
L-level input leakage current of PIN #14, #15 (AIN, BIN)	I_{IL}	– 70		µA	V_I = GNDd[1)]
H-level input leakage current of PIN #14, #15 (AIN, BIN)	I_{IH}		70	µA	V_I = VDDd[1)]
L-level input leakage current for pins with pull-up resistors	I_{ILPU}	– 100	100	µA	V_I = GNDd[1)]
H-level input leakage current for pins with pull-up resistors	I_{IHPU}	– 10	10	µA	V_I = VDDd[1)]
L-level input leakage current for pins with pull-down resistors	I_{ILPD}	– 30	30	µA	V_I = GNDd[1)]
H-level input leakage current for pins with pull-down resistors	I_{IHPD}		500	µA	V_I = VDDd[1)]
H-level output voltage for all outputs except DOUT	V_{OH1}	2.4		V	I_{OH1} = 0.4 mA [1)]
H-level output voltage for DOUT	V_{OH2}	3.5		V	I_{OH2} = 6 mA[1)]
L-level output voltage for all outputs except DOUT	V_{OL1}		0.4	V	I_{OL1} = 2 mA[1)]
L-level output voltage for DOUT	V_{OL2}		0.5	V	I_{OL1} = 7 mA[1)]
Input capacitance DIN, PS1, PS2, DCL, FSC (input) DOUT (open)	C_{IN}		10	pF	

Note: [1)] Inputs at VDDd/GNDd

U-transceiver Characteristics

	Limit Values			Unit
	min.	typ.	max.	
Receive Path				
Signal / (noise + total harmonic distortion)[1]	60	65		dB
DC-level at AD-output	45	50	55	%[4]
Threshold of level detect	4	20	28	mV
Input impedance AIN/BIN	50			kΩ
Transmit Path				
Signal / (noise + total harmonic distortion) [2]	65	70		dB
Output DC-level	2.05	2.375	2.6	dB
Offset between AOUT and BOUT			35.5	mV
Signal amplitude [3]	3.10	3.20	3.30	V
Output impedance AOUT/BOUT: Power-up Power-down		 2 6	 4 12	 Ω Ω

Note:
1) Test conditions: 1.3 Vpp antisemetric sine wave as input on AIN/BIN with long range (low, critical range).
2) Interpretation and test conditions: The sum of noise and total harmonic distortion, weighted with a low pass filter 0 to 80 kHz, is at least 65 dB below the signal for an evenly distributed but otherwise random sequence of + 3, + 1, – 1, – 3.
3) The signal amplitude measured over a period of 1 min. varies less than 1%.
4) The percentage of the “1“-values in the PDM-signal.

Pin Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V; f_C = 1 MHz

Pin	Parameter	Symbol	Limit Values		Unit
			min.	max.	
All pins except XIN, XOUT	Pin capacitance	C_{IO}		7	pF
XIN, XOUT	Pin capacitance	C_{IO}		5	pF

Supply voltages

VDD_d = + 5 V ± 0.25 V
VDD_a1-2 = + 5 V ± 0.25 V

The maximum sinusoidal ripple on VDD_a1-2 is specified in the following figure:

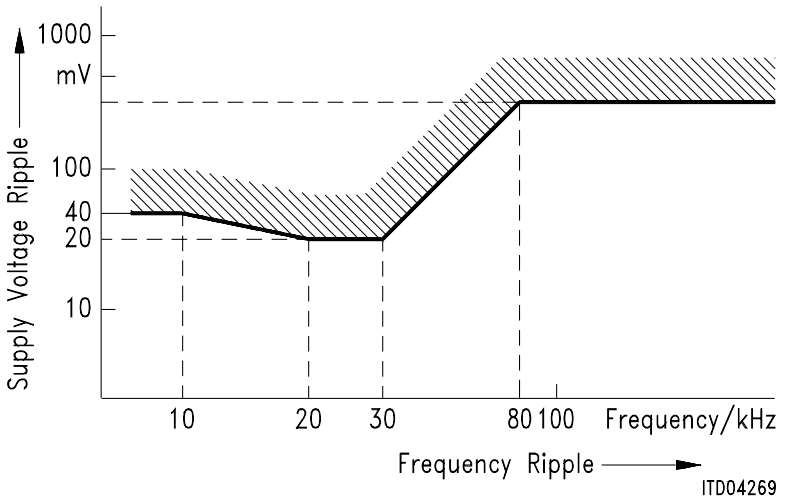


Figure 49 Maximum Sinusoidal Ripple on Supply Voltage

5.4 AC Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown in **figure 50.**

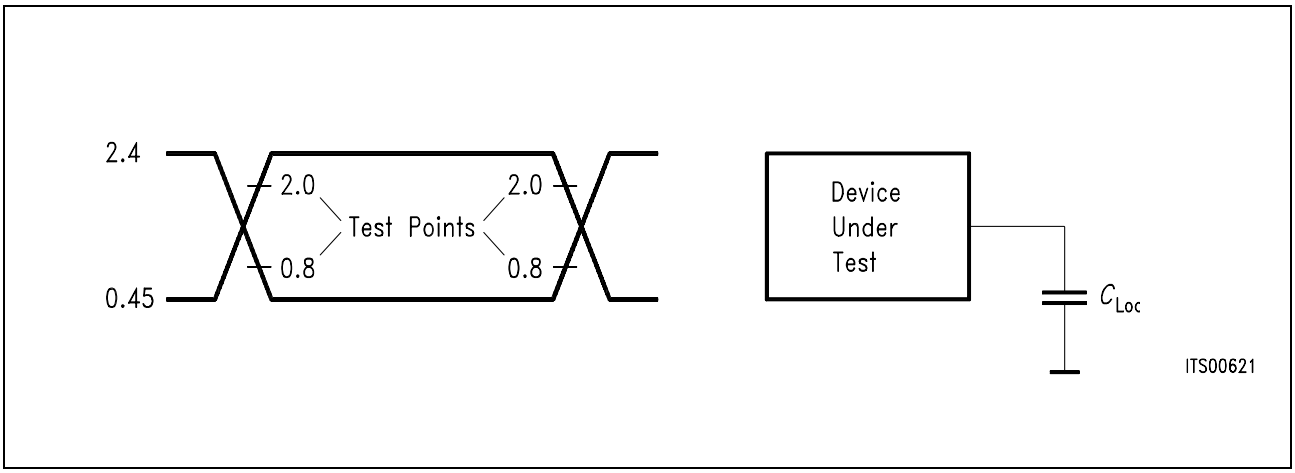


Figure 50 Input/Output Waveform for AC Tests

5.4.1 Parallel Microprocessor Interface Timing

Siemens/Intel Bus Mode

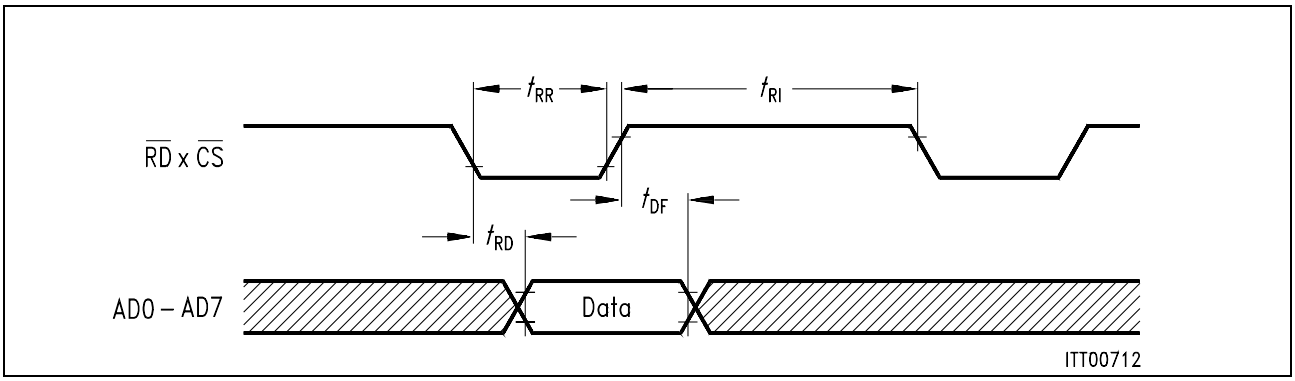


Figure 51 Siemens/Intel Read Cycle

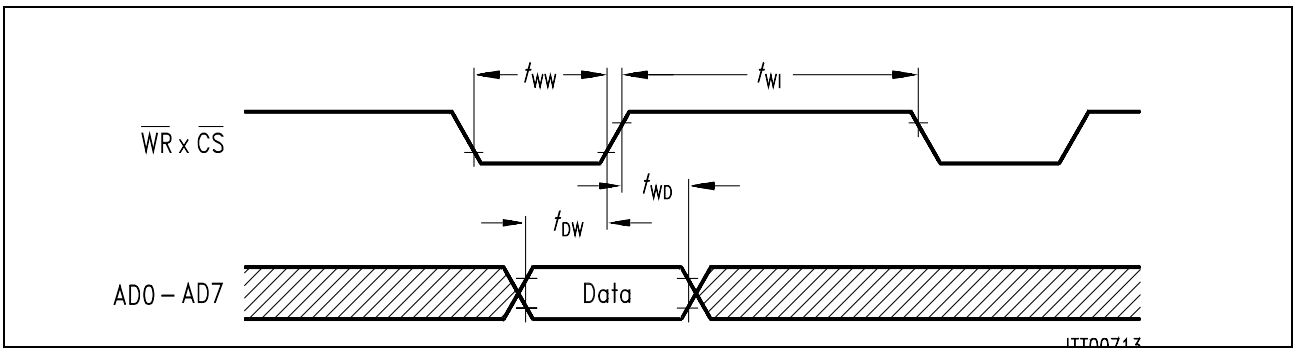


Figure 52 Siemens/Intel Write Cycle

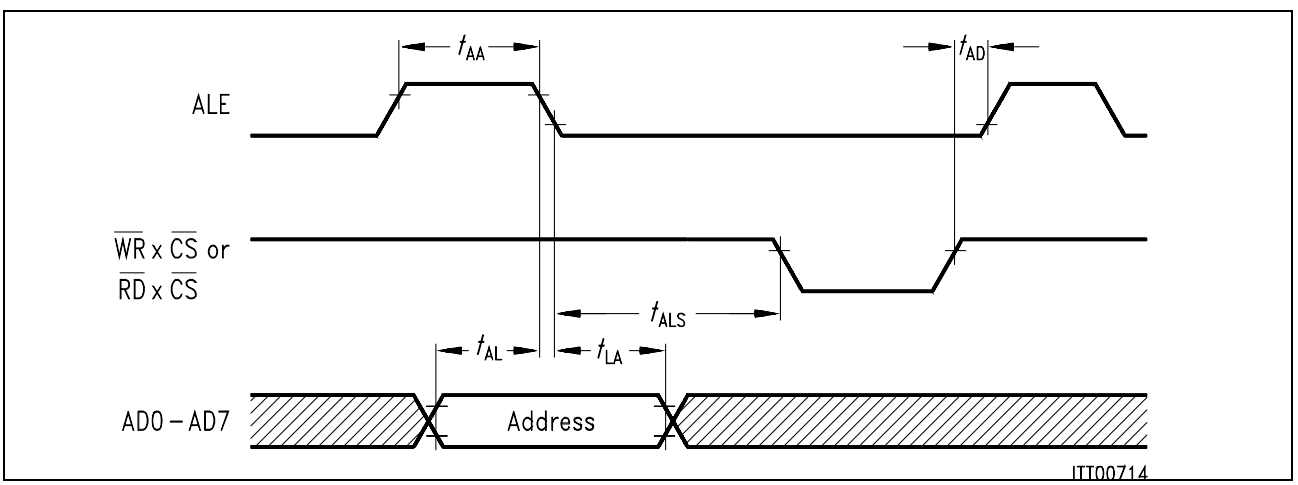


Figure 53 Siemens/Intel Multiplexed Address Timing

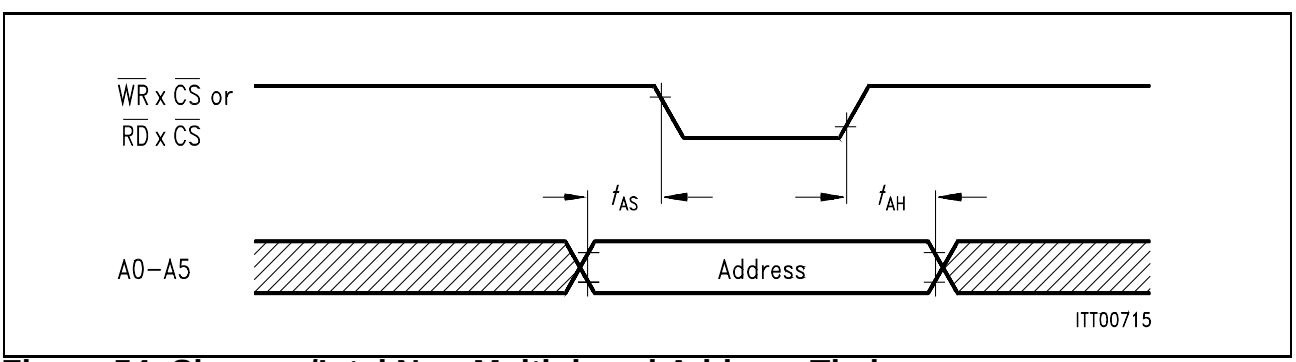


Figure 54 Siemens/Intel Non-Multiplexed Address Timing

Motorola Bus Mode

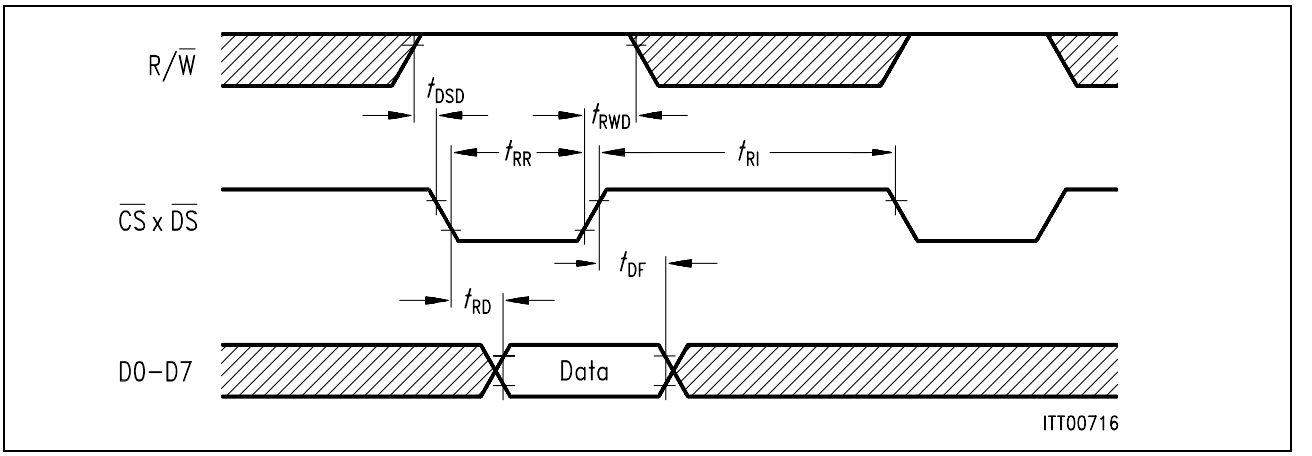


Figure 55 Motorola Read Timing

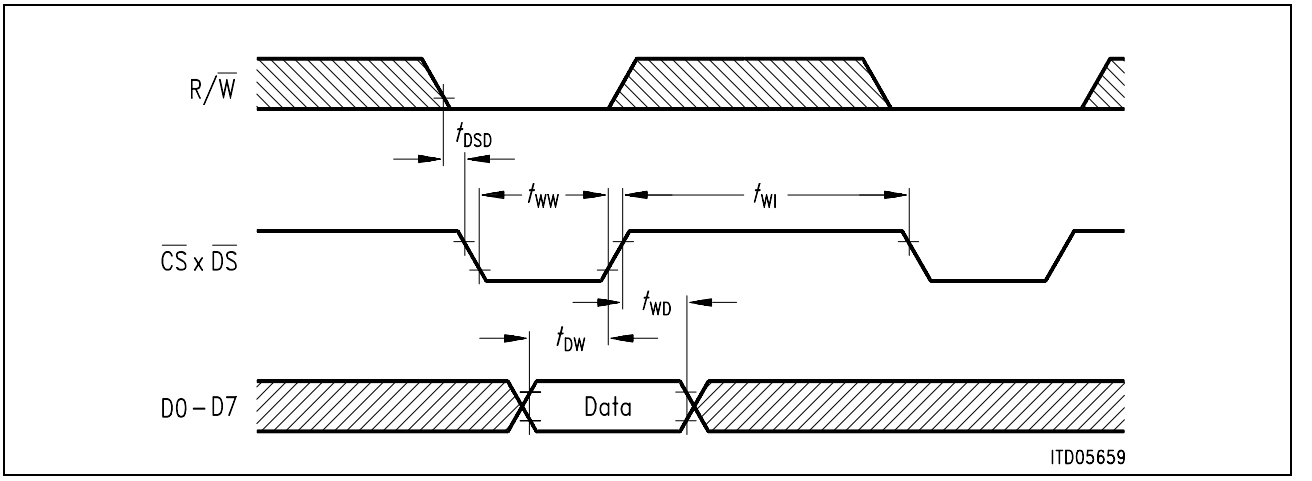


Figure 56 Motorola Write Cycle

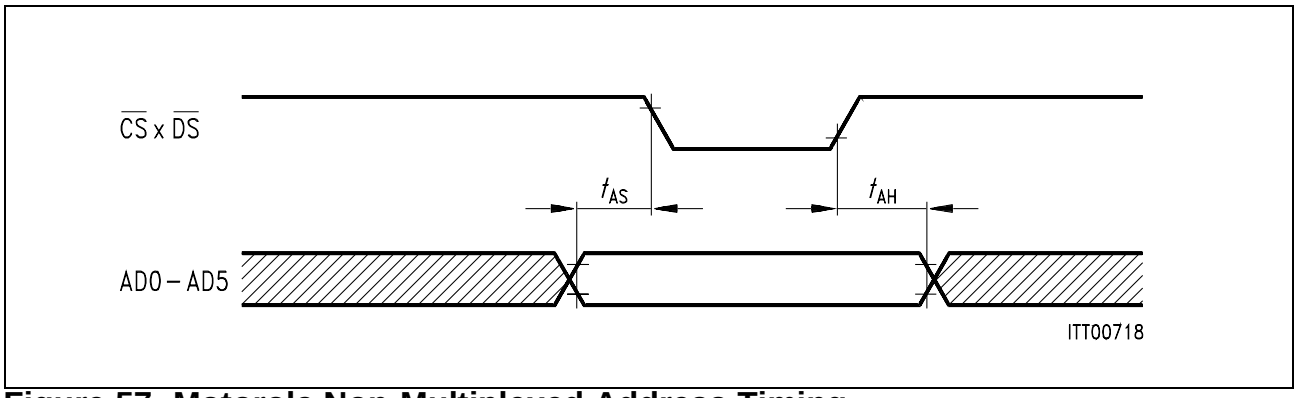


Figure 57 Motorola Non-Multiplexed Address Timing

Microprocessor Interface Timing

C_{Load} = 50pF

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	60		ns
Address setup time to ALE	t_{AL}	20		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time	t_{AS}	35		ns
Address hold time	t_{AH}	0		ns
ALE guard time	t_{AD}	70		ns
$\overline{DS}$ delay after R/$\overline{W}$ setup	t_{DSD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	280		ns
Data output delay from $\overline{RD}$	t_{RD}		280	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{W}$ pulse width	t_{WW}	280		ns
Data setup time to $\overline{W}$ x $\overline{CS}$	t_{DW}	170		ns
Data hold time $\overline{W}$ x $\overline{CS}$	t_{WD}	10		ns
$\overline{W}$ control interval	t_{WI}	70		ns

5.4.2 Serial Microprocessor Interface Timing

The following 2 figures describe the read/write cycles and the corresponding address timing for the serial microprocessor interface:

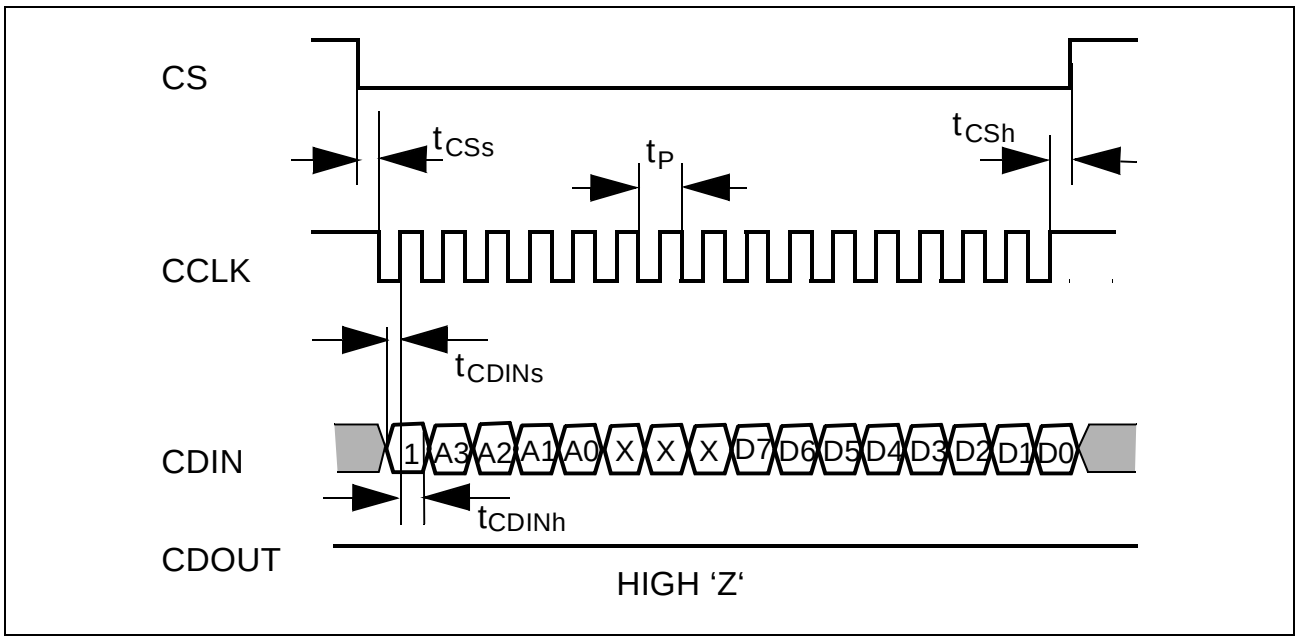


Figure 58 Serial µP Interface Mode Write

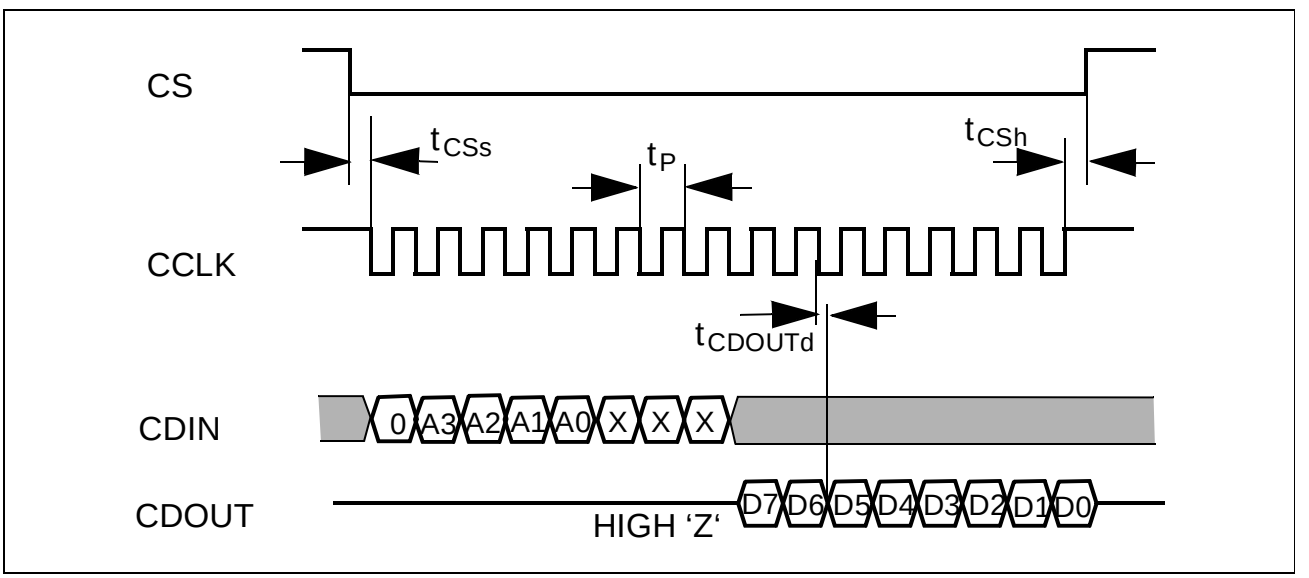


Figure 59 Serial µP Interface Mode Read

Table 25 Timing Characteristics (serial µP interface mode)

C_{Load} = 50pF

Parameter	Symbol	min.	max.	unit
Clock period	t_P	130		ns
Chip Select setup time	t_{CSs}	0		ns
Chip Select hold time	t_{CSh}	20		ns
CDIN setup time	t_{CDINs}	40		ns
CDIN hold time	t_{CDINh}	40		ns
CDOUT data out delay	t_{CDOUTd}		30	ns

5.4.3 IOM®-2 Interface Timing

5.4.3.1 NT Mode

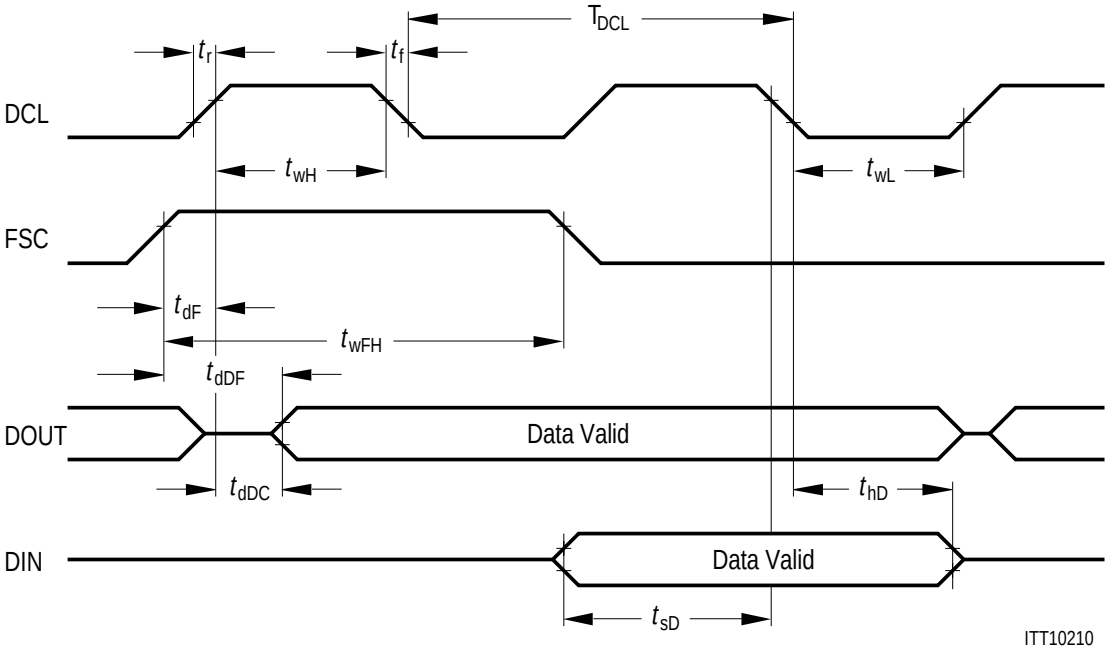


Figure 60 IOM®-2 Timing in NT Mode

Table 26 IOM®-2 in NT Mode

Parameter	Signal	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Data clock rise/fall	DCL	t_R, t_F			30	ns	C_L = 25 pF
Clock period [1]		T_{DCL}	1875	1953	2035	ns	C_L = 25 pF
Pulse width [1] high/low		t_{wH} t_{wL}	850	960	1105	ns	
Clock period [2]		T_{DCL}	565	651	735	ns	C_L = 25 pF
Pulse width [2] high/low		t_{wH} t_{wL}	200	310	420	ns	
Frame width high [4]	FSC	t_{wFH}		T_{DCL}			C_L = 25 pF
Frame width high [5]	FSC	t_{wFH}		$2 \times T_{DCL}$			C_L = 25 pF
Frame synch. rise/ fall		t_R, t_F			30	ns	C_L = 25 pF
Frame advance		t_{dF}	0	65	130	ns	C_L = 25 pF
Data out	DOUT	t_F			200	ns	C_L = 150 pF (R = 1 kΩ to V_{DD}, open drain)
Data out		t_R, t_F			150	ns	C_L = 150 pF (tristate)
Data delay clock [3]		t_{dDC}			100	ns	C_L = 150 pF
Data delay frame [3]		t_{dDF}			150	ns	C_L = 150 pF
Data sample delay	DIN	t_{sD}	t_{wH} + 20			ns	
Data hold		t_{hD}	50			ns	

Notes:

[1] 256 kbit/s (DCL = 512 kHz)

[2] 768 kbit/s (DCL = 1.523 MHz)

[3] The point of time at which the output data will be valid is referred to the rising edges of either FSC (t_{dDF}) or DCL (t_{dDC}). The rising edge of the signal appearing last (normally DCL) shall be the reference.

[4] FSC marking superframe

[5] FSC marking non-superframe

Power Controller Interface (Stand-Alone mode only)

Figures 61 and **62** depict the timing for read and write operations.

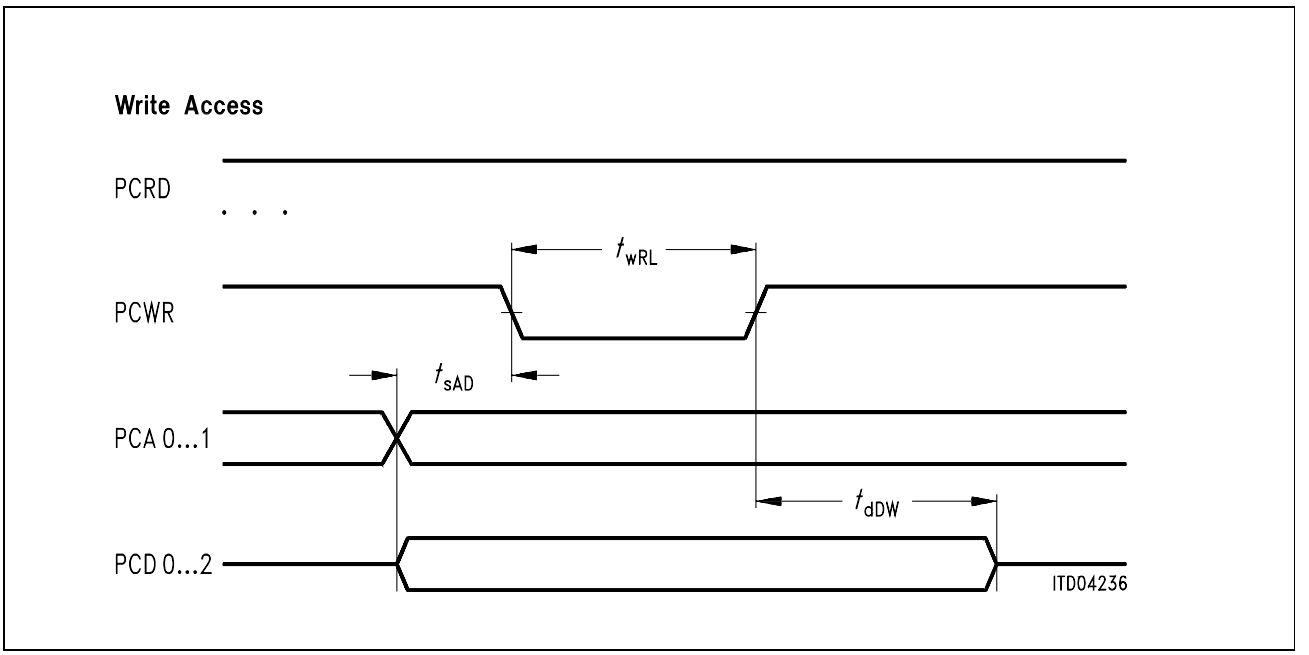


Figure 61 Dynamic Characteristics of Power Controller Write Access

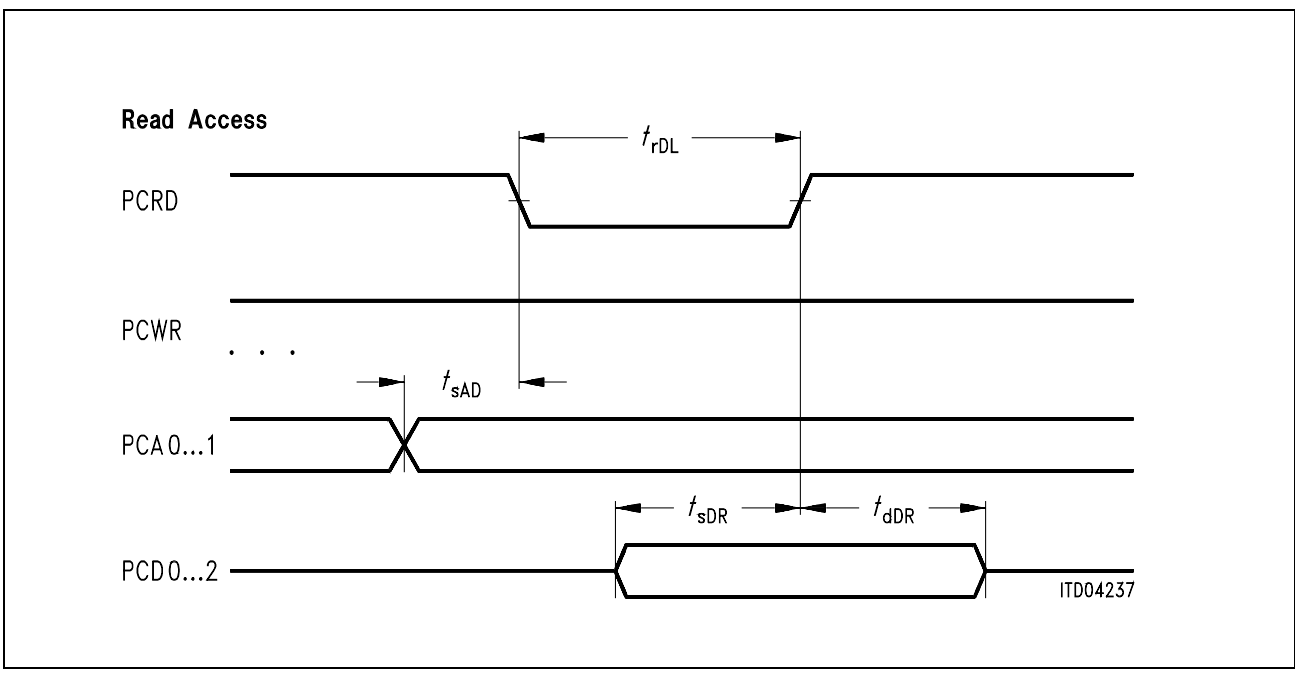


Figure 62 Dynamic Characteristics of Power Controller Read Access

Table 27 Power Controller Interface Dynamic Characteristics

C_{Load} = 25pF

Parameter	Signal	Symbol	Limit Values			Unit
			min.	typ.	max.	
Write clock rise/fall	PCWR	$t_{R,}\ t_F$			30	ns
Write with low		t_{wRL}		$4 \times T_{DCL}$		ns
Address set-up	PCA0 … 1	t_{sAD}		$2 \times T_{DCL}$		ns
Data delay write	PCD0 … 2	t_{dDW}		$2 \times T_{DCL}$		ns
Data delay read		t_{dDR}	130			ns
Set-up data read		t_{sDR}	130			ns
Read clock rise/fall	PCRD	$t_{R,}\ t_F$			30	ns
Read width		t_{rDL}		$4 \times T_{DCL}$		ns

Reset

Table 28 Reset Timing

Parameter	Symbol	Limit Values	Unit	Test Conditions
		min.		
Power-on Reset Active low state	t_{RST}	67	ms	
Watchdog Reset Active low state	t_{RST}	5	ms	
Reset at pin $\overline{RES}$ Active low state	t_{RST}	10	ns	

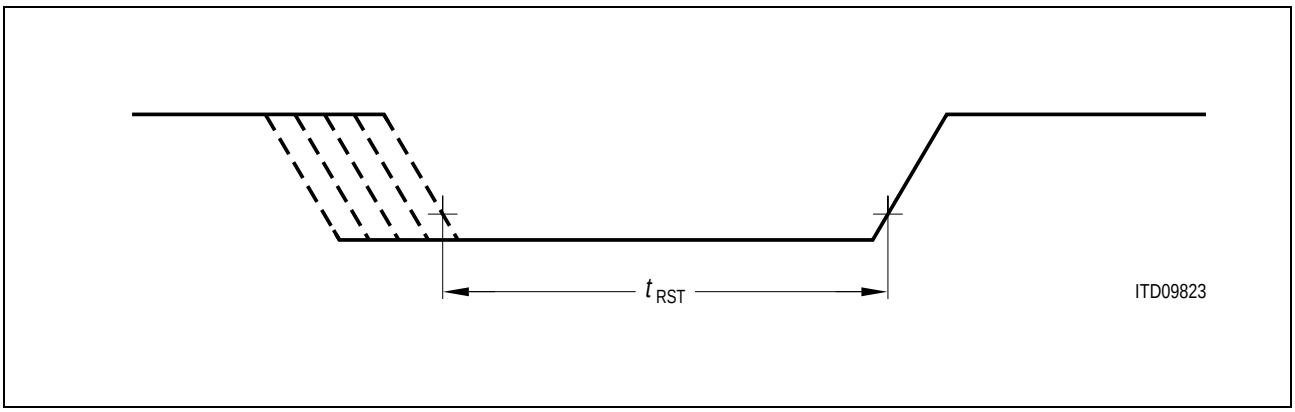
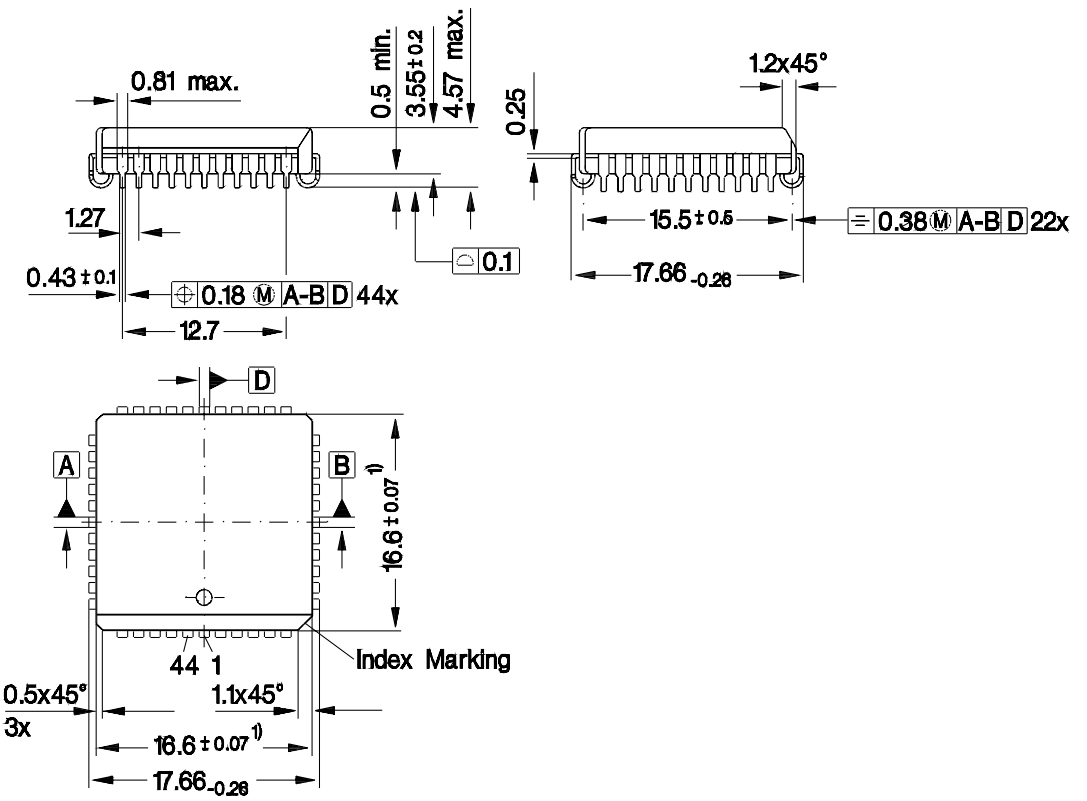


Figure 63 Reset Signal

6 Package Outlines

Plastic Package, P-LCC-44
(Metric Quad Flat Package)



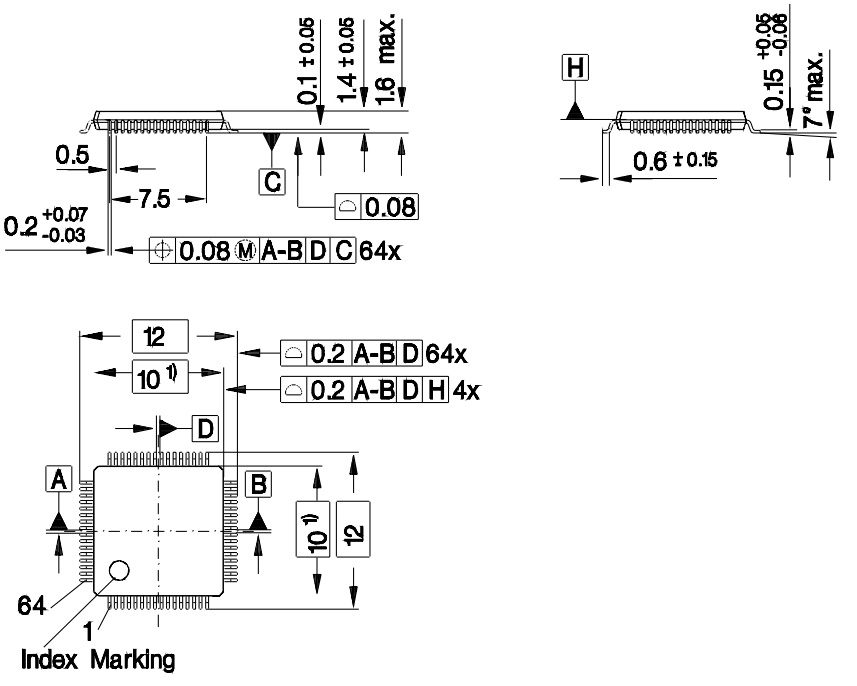
1) Does not include plastic or metal protrusion of 0.15 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book 'Package Information'.

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, T-QFP-64
(Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book 'Package Information'.

SMD = Surface Mounted Device

Dimensions in mm

7 External Component Sourcing

The following tables contain transformers and crystals recommended by different manufacturers for use with Siemens ICs. No manufacturer can be recommended over another.

Transformers marked with *) have been tested at Siemens Semiconductors and have shown positive test results.

This list is not complete. It contains a few examples of devices offered by different manufacturers. Most manufacturers offer a variety of components with different parameters. For latest information please contact the manufacturers directly or visit their web pages where available.

Note: There may also exist other manufacturers than those included in the list.

Table 29 U-Transformer Information

Part Number	**Comments**	**Contacts (Phone)**	**Fax**
APC			www.apcisdn.com
APC42954	2kV, RM8, PTH	EU: +44 1634 2905-88 SEA: +852 2410-2731 US: (201) 368 17-50	-91 -2518 -04
APC42963S	2kV, RM6, SMD		
APC131...	incl. hybrid and MLT		
PulseEngineering			www.pulse.com
PE-65575	2kV	EU: +44 14834-28877 SEA: +886 78-213141 US: (619) 674 8100	-16011 -419707 -8262
PE-68669	3kV, reinforced		
PE-68670	3kV, Low bit error rate		
S+MComponents			www.siemens.de/pr
V409	2kV, RM6, SMD	EU: +49 89 6362 4265 SEA: +65 744-7768 US: (908)-906 4300	 -6992 -632 2830
V832	2kV, RM8, PTH		
W144	4kV, RM8, PTH		
SchottCorporation			
		US: (615)-889-8800	

Table 29 U-Transformer Information (cont'd)

Part Number	**Comments**	**Contacts (Phone)**	**Fax**
Vacuumschmelze			www.vacuumschmelze.de
T60403 -M6290-X054	2kV	EU: +49 6181 38-2673 SEA: +65 84-04 880 US: (405) 943 9651	-2780 -26 607 -949 2967
-M6290-X058	2kV/4kV; Low bit error rate		
-M6276-X...	2kV; SMD		
TDK			
		EU: +49 2192 487-0	
Valor			www.valorinc.com
		EU: +44 1727-8248-75 SEA: +852 2 953-1000 US: (619) 537-2500	-98 -1333 -2525
Vogt			www.vogt-electronic.com
544 03 006 00	2kV, PTH	EU: +49 8591 17-0 SEA: +86 21 6251-2227 US: (914) 921-6900	-240 -4489 -6381

Table 30 Crystal Information

Part Number	Comments	Contacts (Phone)	Fax
FrischerElectronic			
		EU: +49 9131-33007	
KVG			
		EU: +49 7263 648-0	
NDK			
		J: (03)-460-2111 US: (408) 255-0831	
Saronix			
		US: (415) 856-6900	
Tele Quarz			
		EU: +49 7268 8010	

8 Glossary

A/D	Analog-to digital
ADC	Analog-to digital converter
AGC	Automatic gain control
AIN	Differential U-interface input
ANSI	American National Standardization Institute
ARCOFI	Audio ringing codec filter
AOUT	Differential U-interface output
B	64-kbit/s voice and data transmission channel
BCL	Bit clock
BIN	Differential U-interface input
BOUT	Differential U-interface output
C/I	Command/Indicate (channel)
CCITT	Comité Consultatif International des Téléphones et Télégraph
CCRC	Corrupted CRC
CRC	Cyclic redundancy check
D	16-kbit/s data and control transmission channel
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DCL	Data clock
DD	Data downstream
DT	Data through test mode
DU	Data upstream
EC	Echo canceller
EOC	Embedded operations channel
EOM	End of message
ETSI	European Telephone Standards Institute
FEBE	Far-end block error
FIFO	First-in first-out (memory)
FSC	Frame synchronizing clock
GND	Ground
HDLC	High-level data link control
ICC	ISDN-communications controller
IEC-Q	ISDN-echo cancellation circuit conforming to 2B1Q-transmission code
IOM-2	ISDN-oriented modular 2nd generation
INFO	U- and S-interface signal as specified by ANSI/ETSI
ISDN	Integrated services digital network
ISW	Inverted synchronization word
LB	Loop back
LBBD	Loop-back of B- and D-channels
LSB	Least significant bit
LT	Line termination
MON	Monitor channel command
MSB	Most significant bit
MR	Monitor read bit
MTO	Monitor procedure timeout
MX	Monitor transmit bit

NCC	Notify of corrupt CRC
NEBE	Near-end block error
NT	Network termination
OSI	Open systems interconnection
PLL	Phase locked loop
PS	Power supply status bit
PSD	Power spectral density
PTT	Post, telephone, and telegraph administration
PU	Power-up
RCC	Request corrupt CRC
RCI	Read Power Controller Interface
RMS	Root mean square
RP	Repeater
S/T	Two-wire pair interface
SBCX	S/T-bus interface circuit extended
SICOFI	Signal processing codec filter
SLIC	Subscriber line interface circuit
SSP	Send single pulses (test mode)
ST	Self test
SW	Synchronization word
TE	Terminal equipment
TL	Wake-up tone, LT side
TN	Wake-up tone, NT side
TP	Test pin
U	Single wire pair interface
UTC	Unable to comply
2B1Q	Transmission code requiring 80-kHz bandwidth

Appendix A: Jitter on IOM-2

The output jitter on the IOM-2 clocks FSC and DCL/BCL may be higher than in versions 4.3 and older. The jitter on pin CLS is the same as in versions 4.3 and older. This does not contradict any norm or specification. However in jitter sensitive applications the system performance should be rechecked.

For PCM-2 applications - as depicted in the IEC-Q V4.3 User's Manual 02.95 on page 44 - it is not recommended to use the IEC-Q TE V5.2 together with version 3.0 of SICOFI-2 (PEB/F 2260). This is due to the somewhat different behavior of this SICOFI-2 version from earlier versions (see Delta Sheet, May 1996, of the PEB/F 2260).
Instead, it is recommended to use the PEB 2091 IEC-Q in NT-PBX mode for PCM-2 applications with the PEB/F 2260. The application with IEC-Q and SICOFI-2 is described in the IEC-Q V5.2 Errata Sheet 09.97 on page 6ff.

Appendix B:S/G Bit Control State Machine

The state machine of the S/G bit control in TE mode is given in the following state diagrams. The values in the state diagrams are to be interpreted as follows:

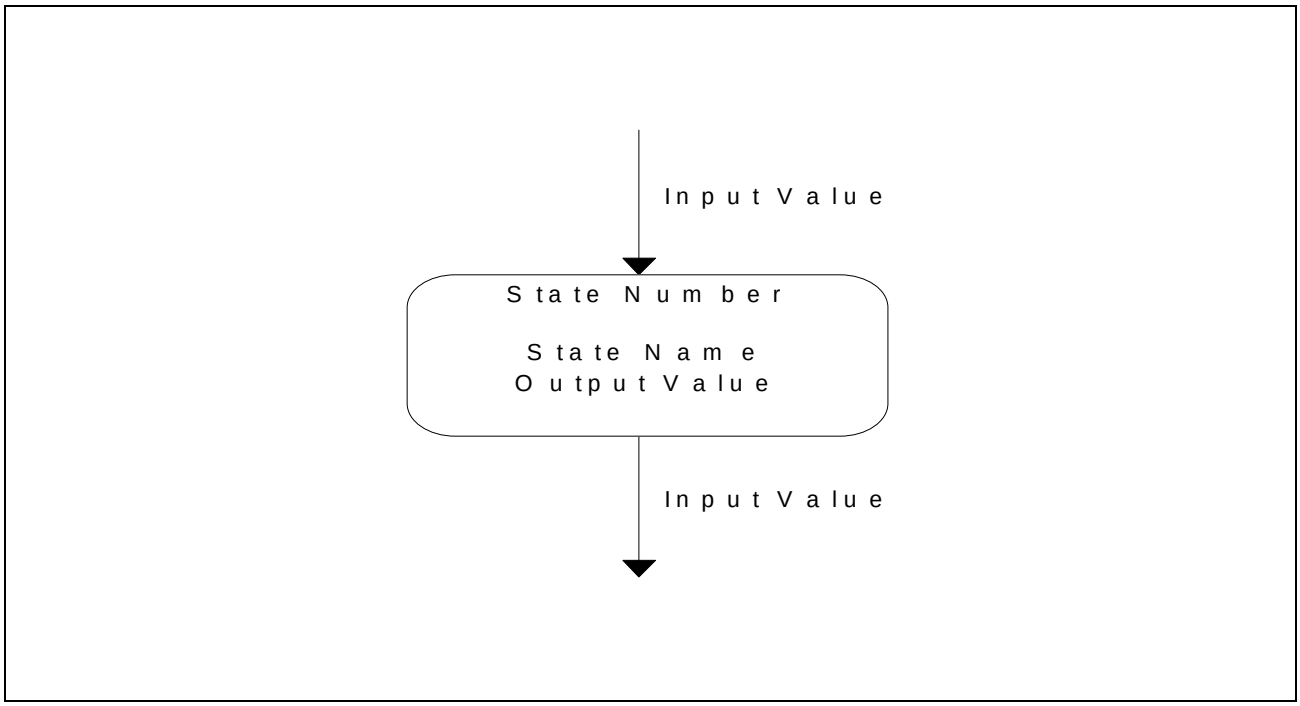


Figure 64 S/G Bit State Machine Notation

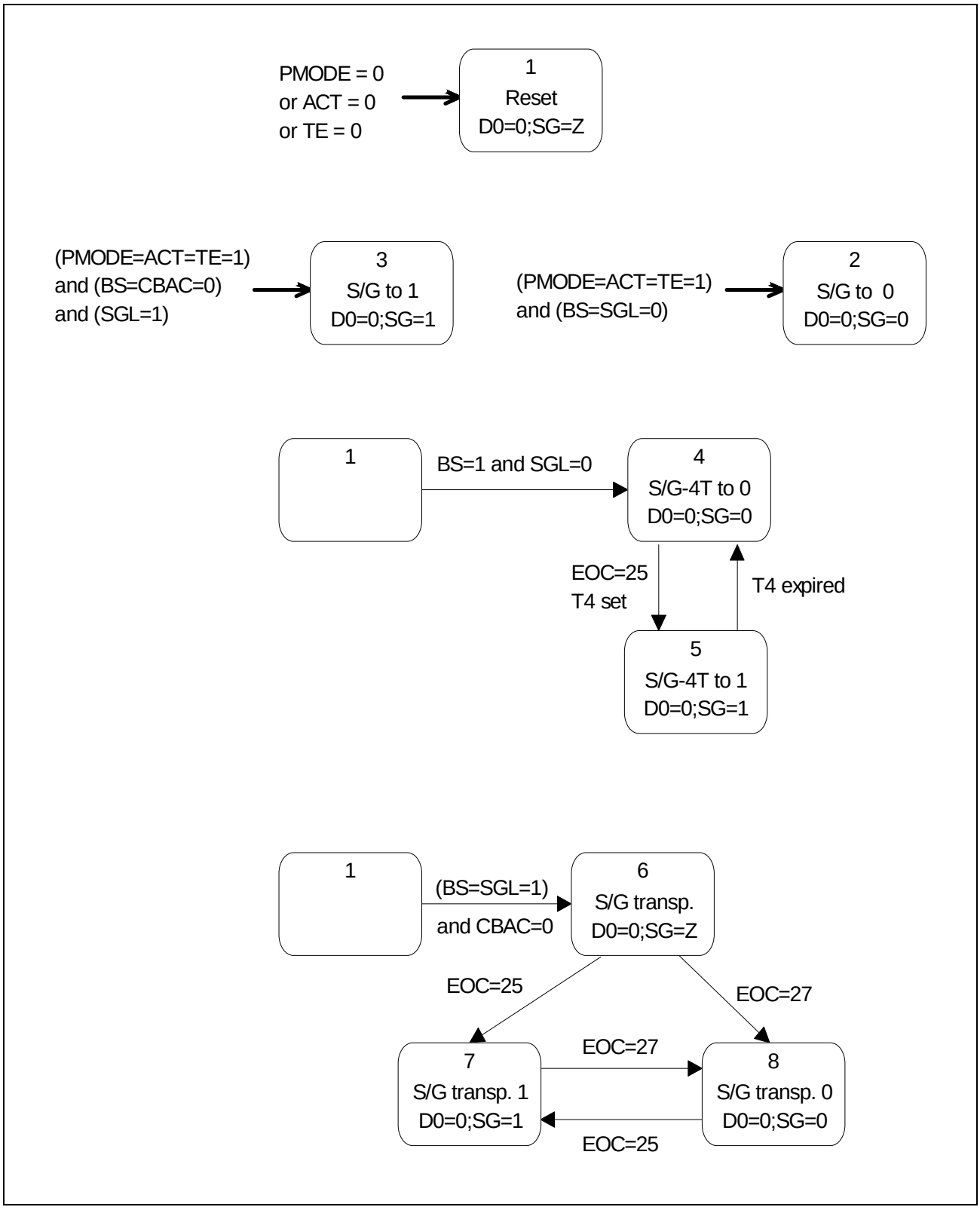


Figure 65 State machine (part 1)

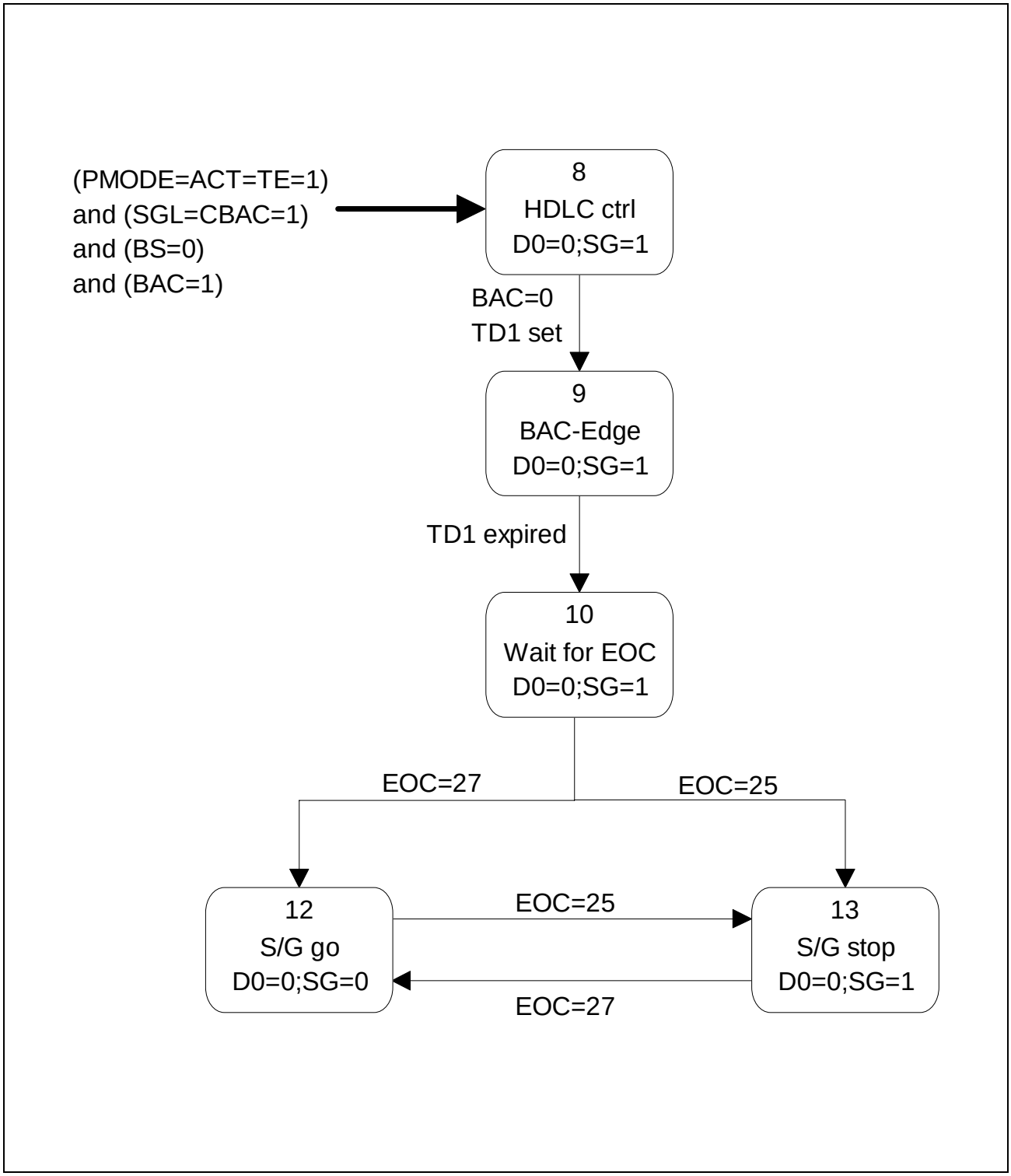


Figure 66 State machine (part 2)

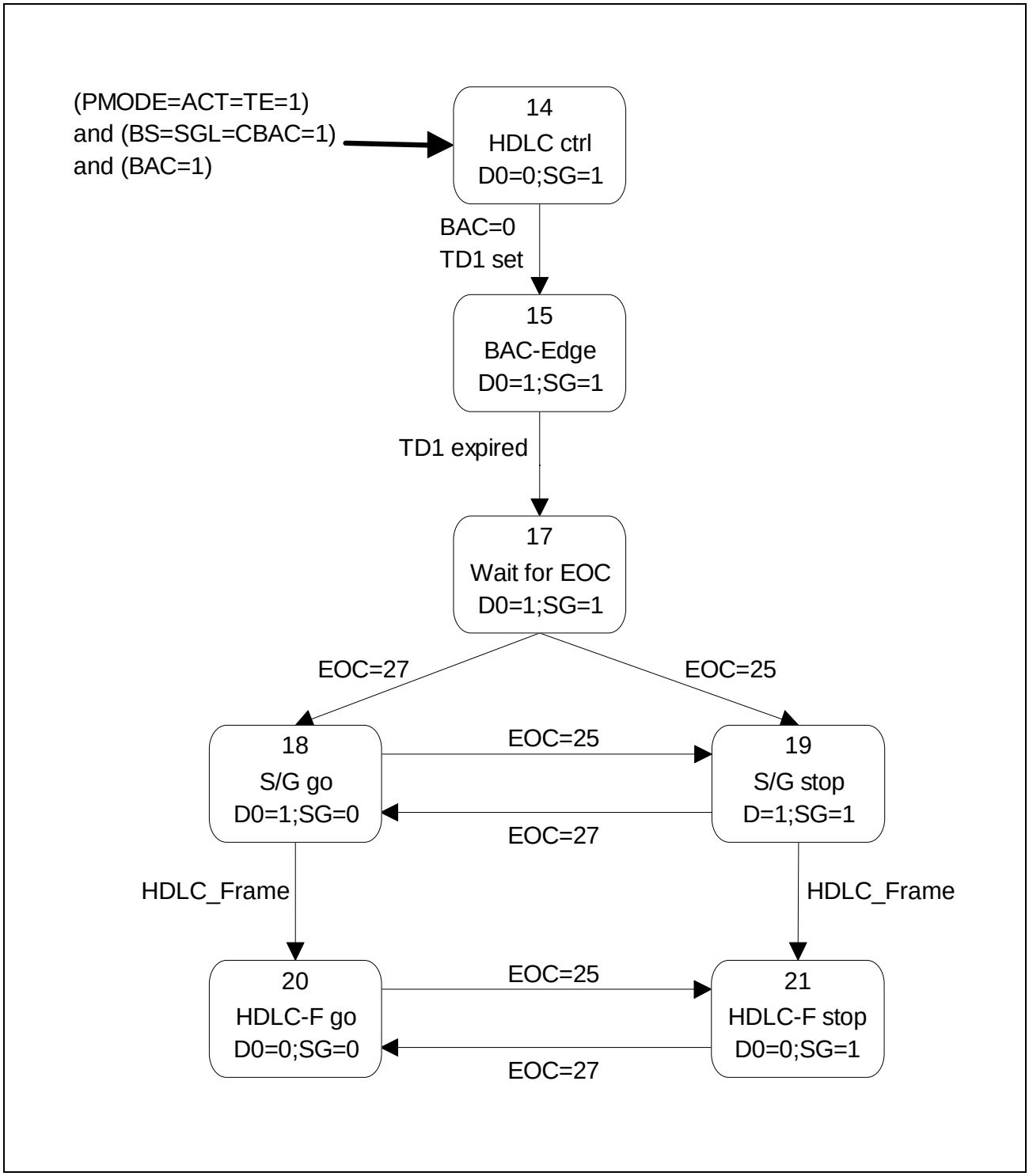


Figure 67 State machine (part 3)

Table 31 State Machine Input Signals

No.	Signal name	Description
1	PMODE	Corresponds to the PMODE pin. Set to "1" (only) in the microprocessor mode
2	TE	This input is set to "1" (only) in the TE mode
3	ACT	"1" on this input indicates receiver synchronization (e.g. in the Transparent state, see IEC-Q V4.3 User‘s Manual 02.95, page 175).
4	BS	SWST:BS bit.
5	SGL	SWST:SGL bit.
6	CBAC	ADF:CBAC bit.
7	EOC=25	This input indicates that the EOC code 25h (stop) was received on the U interface.
8	EOC=27	This input indicates that the EOC code 27h (go) was received on the U interface.
9	T1 set	A 500 micro seconds timer is enabled.
10	T1 expired	The 500 micro seconds timer (see 9) has expired.
11	TD1 set	The timer TD1 is enabled. This timer depends on the position of the EOC frame in the currently received U data. It varies between 7.5 and 15 ms.
12	TD1 expired	The timer TD1 has expired. This timer depends on the position of the EOC frame in the currently received U data. It varies between 7.5 and 15 ms.
13	BAC	BAC bit on DIN. This is bit no. 27 positioned in the third IOM slot

Table 32 State Machine Output Signals

No.	Signal name	Description
1	SG	Value of the S/G bit on DOUT. The S/G bit is bit no. 27 in the third slot on DOUT. SG=Z Means that the SG bit has the value high Z
2	D0	Sets the D channel upstream to "0" if active ("1")

Appendix C:Quick Reference Guide

This chapter contains tables and figures often required when working with the PSB 21911. For additional technical information please refer to the relevant chapter.

U-Transceiver State Diagram

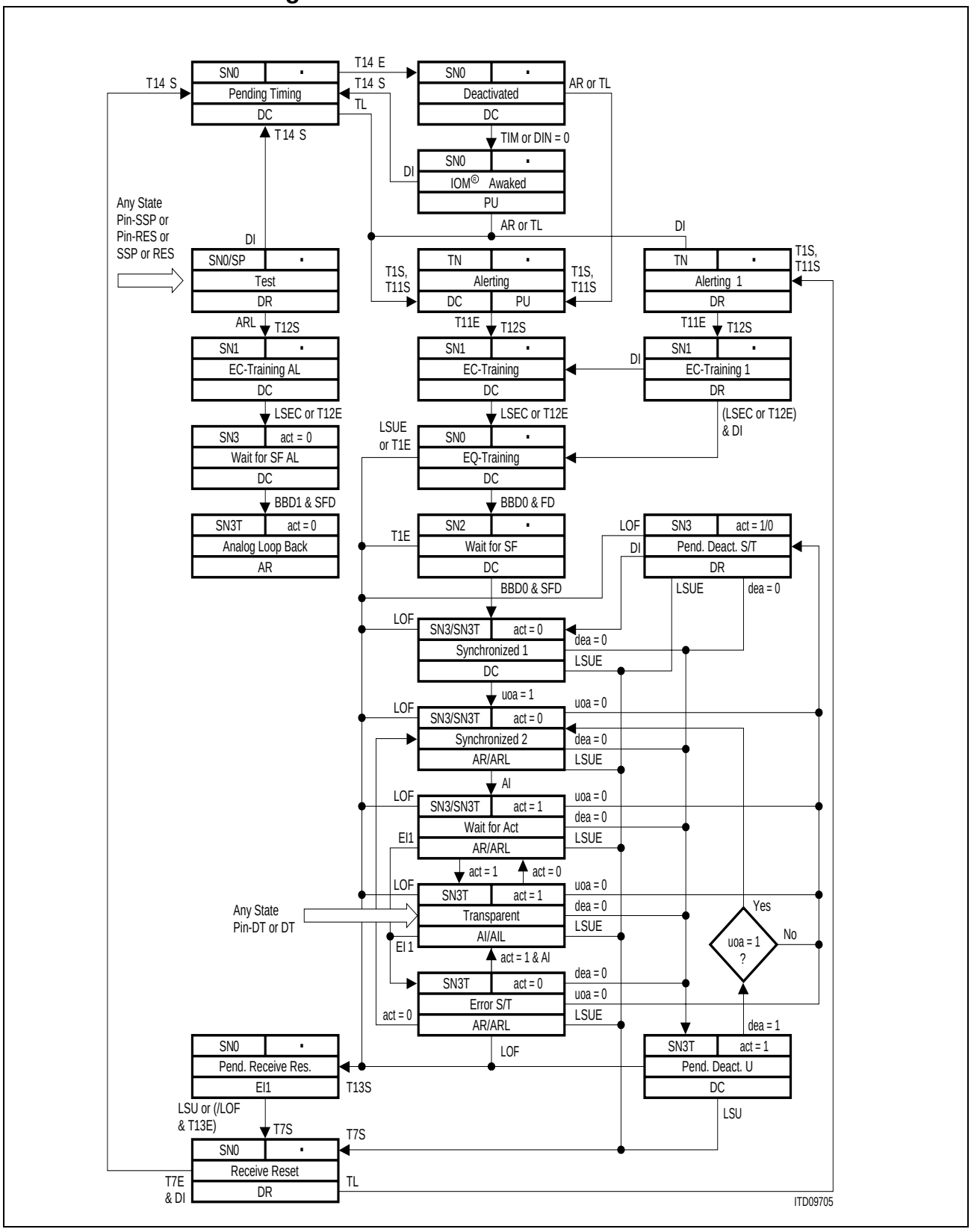


Figure 68 U-Transceiver State Diagram

Table 33 U-Transceiver C/I Codes

Code	NT-Mode	
	IN	OUT
0000	TIM	DR
0001	RES	–
0010	–	–
0011	–	–
0100	EI1	EI1
0101	SSP	–
0110	DT	INT
0111	–	PU
1000	AR	AR
1001	–	–
1010	ARL	ARL
1011	–	–
1100	AI	AI
1101	–	–
1110	–	AIL
1111	DI	DC

AI	Activation Indication	EI1	Error Indication 1
AR	Activation Request	INT	Interrupt
ARL	Activation Request Local Loop	PU	Power-Up
DC	Deactivation Confirmation	RES	Reset
DI	Deactivation Indication	SSP	Send-Single-Pulses test mode
DR	Deactivation Request	TIM	Timing request
DT	Data-Through test mode		