MW3753MAE

8mm (1/2 inch) 768H CCD Area Image Sensor

■ Overview

The MW3753MAE is a 8mm (1/2 inch) Interline Transfer CCD (IT-CCD) solid state image sensor device.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal read out. The electronic shutter function has made possible an exposure time of 1/10000 seconds. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and low smear.
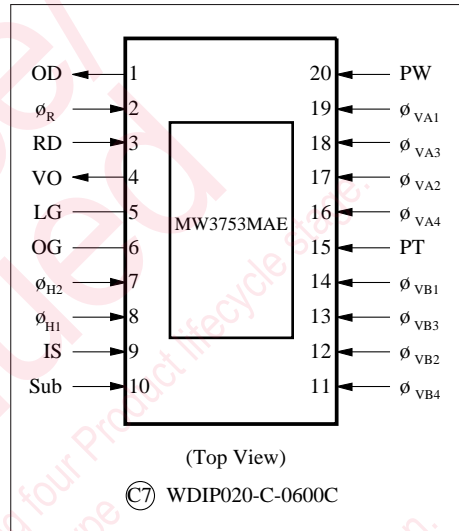
This device has a total of 410K pixels (816 horizontal × 495 vertical) and provides stable and clear images with a resolution of 560 horizontal TV-lines and 350 vertical TV-lines.

Type No.	Size	System	Color or B/W
MW3753MAE	8mm (1/2 inch)	(NTSC)	B/W

■ Features

- Total number of pixels: 816 (horizontal) × 495 (vertical)
- High sensitivity
- Low noise
- Broad dynamic range
- Low smear
- Low image lag
- Electronic shutter function present
- No image distortion
- Small size enables design of compact equipment
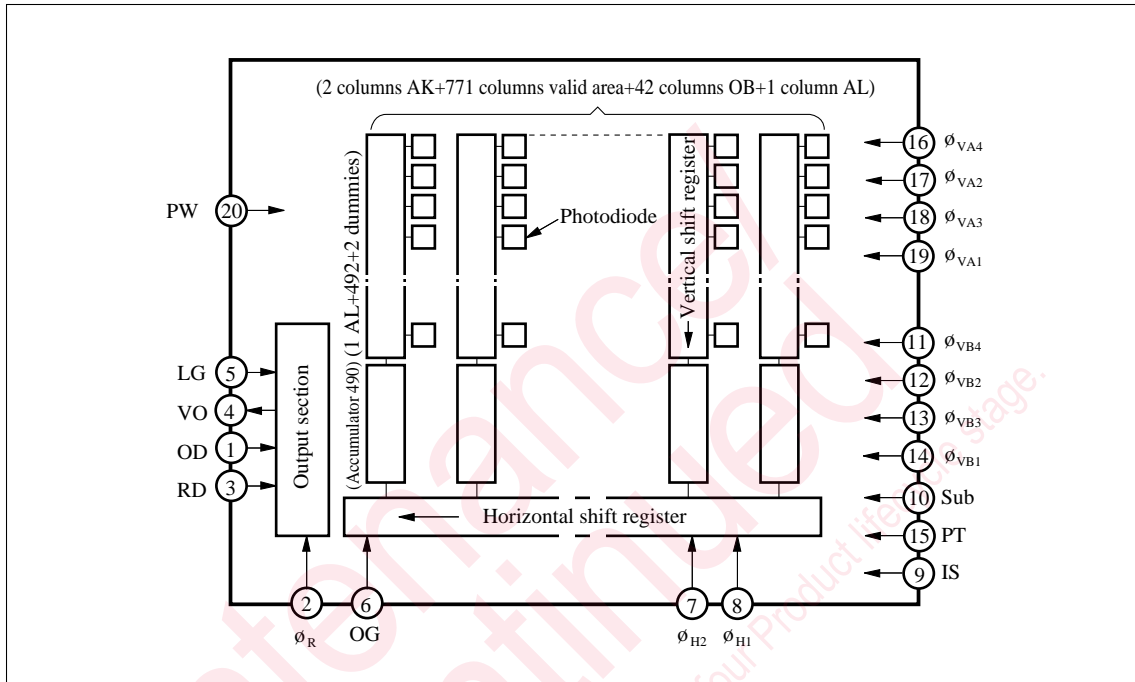- High reliability
- 20 Pin DIL ceramic package

■ Pin Assignments

OD	1	20	PW
ϕ_R	2	19	ϕ_{VA1}
RD	3	18	ϕ_{VA3}
VO	4	17	ϕ_{VA2}
LG	5	16	ϕ_{VA4}
OG	6	MW3753MAE	15	PT
ϕ_{H2}	7	14	ϕ_{VB1}
ϕ_{H1}	8	13	ϕ_{VB3}
IS	9	12	ϕ_{VB2}
Sub	10	11	ϕ_{VB4}

(Top View)

C7 WDIP020-C-0600C

■ Applications

- Cameras for commercial use

■ Block Diagram

■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	OD	Output drain	11	ϕ_{VB4}	Vertical shift register clock pulse (B4)
2	ϕ_R	Reset pulse	12	ϕ_{VB2}	Vertical shift register clock pulse (B2)
3	RD	Reset drain	13	ϕ_{VB3}	Vertical shift register clock pulse (Bb3)
4	VO	Video output	14	ϕ_{VB1}	Vertical shift register clock pulse (B1)
5	LG	Output load transistor gate	15	PT	P-well for protection circuit
6	OG	Output gate	16	ϕ_{VA4}	Vertical shift register clock pulse (A4)
7	ϕ_{H2}	Horizontal register clock pulse (2)	17	ϕ_{VA2}	Vertical shift register clock pulse (A2)
8	ϕ_{H1}	Horizontal register clock pulse (1)	18	ϕ_{VA3}	Vertical shift register clock pulse (A3)
9	IS	Input source	19	ϕ_{VA1}	Vertical shift register clock pulse (A1)
10	Sub	Substrate	20	PW	P-well

■ Absolute Maximum Ratings and Operating Conditions

Parameter		Symbol	Rating		Operating condition			Unit
			min	max	min	typ	max	
Output drain voltage		V_{OD}	0	18	14.7	15.0	15.3	V
Reset pulse voltage	(P–P)	$V_{\phi R\ (P-P)}$	—	18	7.7	8.0	8.3	V
	(L)	$V_{\phi R\ (L)}$	0	—	2.7	3.0	3.3	V
Reset drain voltage		V_{RD}	0	18	14.7	15.0	15.3	V
Video output voltage		V_{VO}	—	—	—	—	—	V
Output load transistor gate voltage		V_{LG}	(Supplied internally)					V
Output gate voltage		V_{OG}	(Supplied internally)					V
Horizontal register	(H)	$V_{\phi H2\ (H)}$	—	18	4.7	5.0	5.3	V
lock pulse voltage (2)	(L)	$V_{\phi H2\ (L)}$	0	—	0	0	0.3	V
Horizontal register	(H)	$V_{\phi H1\ (H)}$	—	18	4.7	5.0	5.3	V
lock pulse voltage (1)	(L)	$V_{\phi H1\ (L)}$	0	—	0	0	0.3	V
Input source voltage		V_{IS}	0	18	14.7	15.0	15.3	V
Substrate voltage 1		$V_{Sub(1)}$ *	0	18	2.0	Adjust	14.0	V
Substrate voltage 2		$V_{Sub(2)}$ *	0	50	28.0	30.0	32.0	V
Vertical shift register	(M)	$V_{\phi VB4\ (M)}$	—	15	1.7	2.0	2.3	V
lock pulse (B4) voltage	(L)	$V_{\phi VB4\ (L)}$	−11	—	−9.3	−9.0	−8.7	V
Vertical shift register	(M)	$V_{\phi VB2\ (M)}$	—	15	1.7	2.0	2.3	V
lock pulse (B2) voltage	(L)	$V_{\phi VB2\ (L)}$	−11	—	−9.3	−9.0	−8.7	V
Vertical shift register	(M)	$V_{\phi VB3\ (M)}$	—	15	0	0	0.3	V
lock pulse (B3) voltage	(L)	$V_{\phi VB3\ (L)}$	−11	—	−9.3	−9.0	−8.7	V
Vertical shift register	(M)	$V_{\phi VB1\ (M)}$	—	15	0	0	0.3	V
lock pulse (B1) voltage	(L)	$V_{\phi VB1\ (L)}$	−11	—	−9.3	−9.0	−8.7	V
Protection P well voltage		V_{PT}	—	—	$\phi_{VL}-0.7$ — $\phi_{VL}-1.3$			V
Vertical shift register	(M)	$V_{\phi VA4\ (M)}$	—	15	1.7	2.0	2.3	V
lock pulse (A4) voltage	(L)	$V_{\phi VA4\ (L)}$	−9	—	−9.3	−9.0	−8.7	V
Vertical shift register	(M)	$V_{\phi VA2\ (M)}$	—	15	1.7	2.0	2.3	V
lock pulse (A2) voltage	(L)	$V_{\phi VA2\ (L)}$	−9	—	−9.3	−9.0	−8.7	V
Vertical shift register	(H)	$V_{\phi VA3\ (H)}$	—	18	15.7	16.0	16.3	V
lock pulse (A3) voltage	(M)	$V_{\phi VA3\ (M)}$	—	18	0	0	0.3	V
	(L)	$V_{\phi VA3\ (L)}$	−9	—	−9.3	−9.0	−8.7	V
Vertical shift register	(H)	$V_{\phi VA1\ (H)}$	—	18	15.7	16.0	16.3	V
lock pulse (A1) voltage	(M)	$V_{\phi VA1\ (M)}$	—	18	0	0	0.3	V
	(L)	$V_{\phi VA1\ (L)}$	−9	—	−9.3	−9.0	−8.7	V
P well voltage		V_{PW}	Reference voltage		—	0	—	V

Note 1) The initial setting of V_{Sub} shall be 8.0V and shall be adjusted to the minimum voltage at which no blooming or no overflow charge is caused at a light input of 200 times the standard value. The standard light input is the one when the exposure is done at an aperture of F/8 using a light source of 2856K and 920nt, and placing a color temperature conversion filter LB-40 (Hoya) and an IR cutting filter CAW-500S (t=2.5mm) in the light path.

Note 2) $V_{Sub(1)}$ is the DC component during normal operation.

$V_{Sub(2)}$ is the amplitude of the pulse added to $V_{Sub(1)}$ during electronic shutter operation.

The operation should be made with ($V_{Sub(1)}+V_{Sub(2)}$) less than or equal to 46V.

Also, the power supply impedance of V_{Sub} should be 100Ω or less.

∗ The absolute maximum rating of $V_{Sub(2)}$ is 50V and the maximum amplitude of the additional part of the voltage is 30V.

∗ Pins 5 and 6 should each be grounded by 0.047μF capacitors.
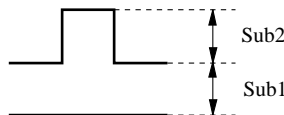
■ Optical Characteristics

Type No.	Color or B/W	Valid pixels		S/N typ. (dB)	Saturation output typ. (mV)	Sensitivity F8 typ. (mV)	Vertical smear Sm typ. (dB)	Image lag typ. (%)	Horizontal resolution typ. (TV-lines)	Vertical resolution typ. (TV-lines)
		H	V							
MW3753MAE	B/W	771	492	62	1700	750	−125	0	560	350

■ Graphs of Characteristics

CCD Spectral Characteristics

Wavelength (nm)
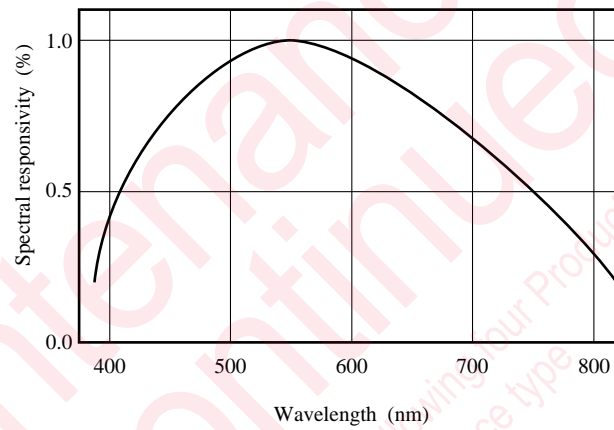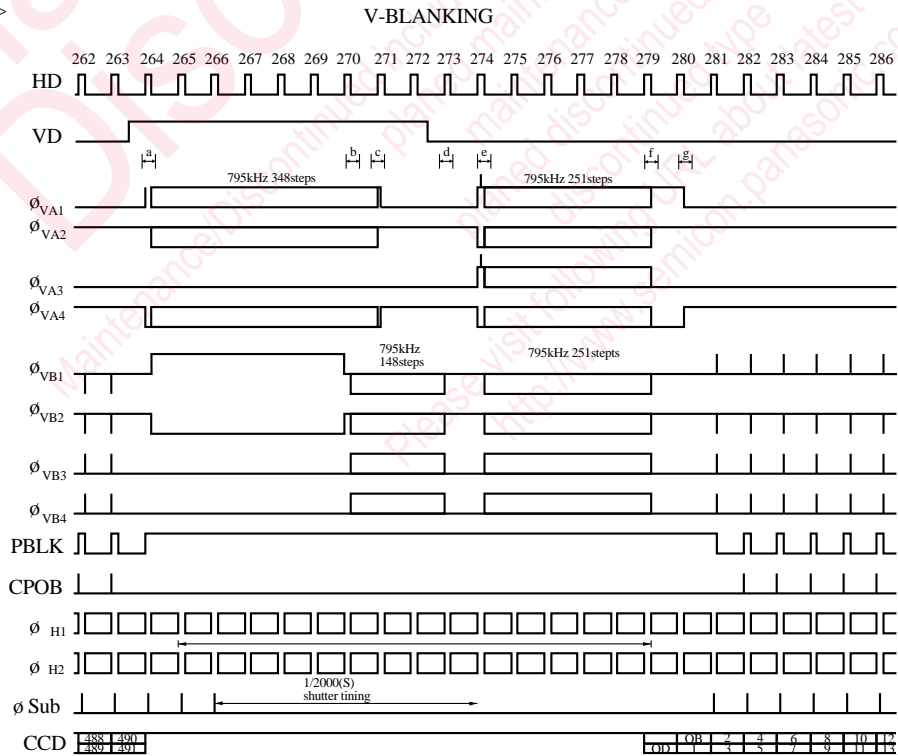
■ Example of Recommended Driving Pulses

< Field A >

V-BLANKING

< Field B >

V-BLANKING
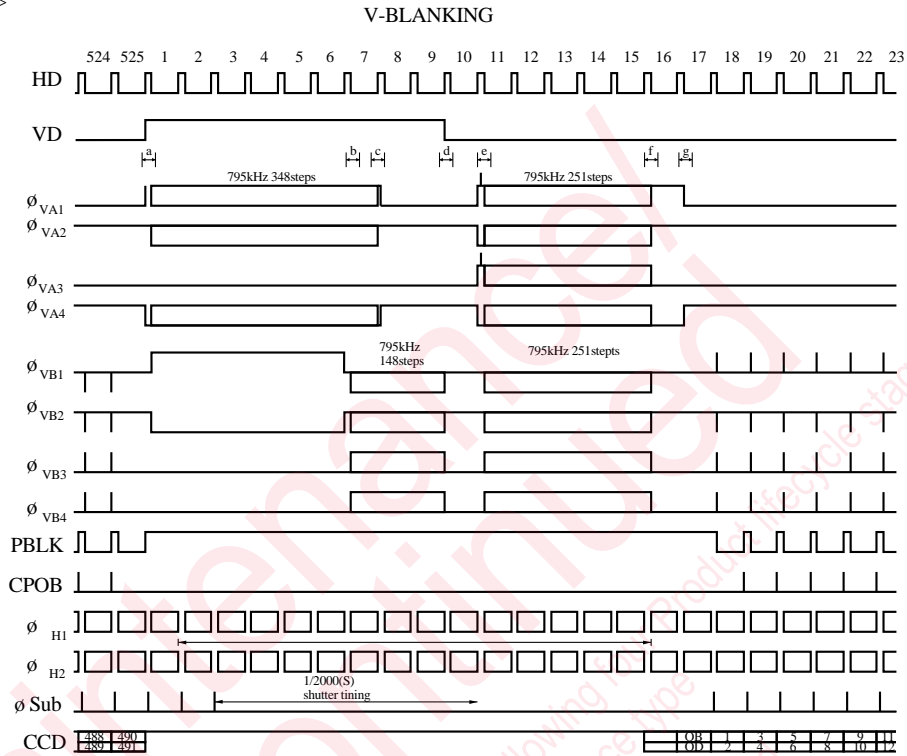
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