CLEAR LOGIC

CL7512AE

Laser Processed Logic Device Family

Key Features

- Laser Processed Logic Device (LPLD™) technology offers the ultimate combination of performance, flexibility, and low cost
- Functionally, architecturally, and electrically compatible with industry-standard Altera® MAX® 7000
- High Density
  - 10,000 Usable gates
  - 512 Macrocells
  - 212 Maximum user I/O pins
- Laser fuse technology provides very fast, dense interconnect routing
- Low current consumption
- Supports 3.3 volt operation
- Alpha particle immune

CL7000 Product Family Overview

Feature	CL7128A CL7128AE	CL7256A CL7256AE	CL7512A
Useable Gates	2,500	5,000	10,000
Macrocells	128	256	512
Logic array Blocks	8	16	32
Max user I/O pins	100	164	212
Speed Grades	-4, -5, -6, -7, -10, -12	-4, -5, -6, -7, -10, -12	-6, -7, -10, -12
Packages	84-Pin PLCC 100-Pin TQFP 100-Pin BGA 144-Pin TQFP	100-Pin TQFP 100-Pin BGA 144-Pin TQFP 208-Pin PQFP 256-Pin BGA	144-Pin TQFP 208-Pin PQFP 256-Pin BGA

7KA tbl 01A

Description

The Clear Logic CL7000 Laser Processed Logic Device (LPLD®) family offers the ultimate combination of performance, flexibility, and cost. This family is a system level second source to Altera MAX® 7000A products. For designs not requiring in-system reprogrammability, design verification can be performed using the programmable Altera devices, and Clear Logic LPLDs can be used for low cost, high volume production.

Clear Logic's innovative laser-based technology eliminates NRE costs, test vector development, ordering minimums and long lead times. No re-simulation or re-layout is required, as the device uses a cell-based, PLD-like architecture. Clear Logic's NoFault® technology ensures complete test coverage through the use of specialized testing modes which are transparent to the user.

The Clear Logic CL7000 Laser Processed Logic Device family is based upon a large array of macrocells. Each macrocell contains a logic array with five product terms, a product-term select matrix, and a configurable register. A group of sixteen macrocells forms a block. Laser-configured metal fuses implement logical functions and control signal routing.

Laser configuration provides reduced cost and enhanced performance. These inherent performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

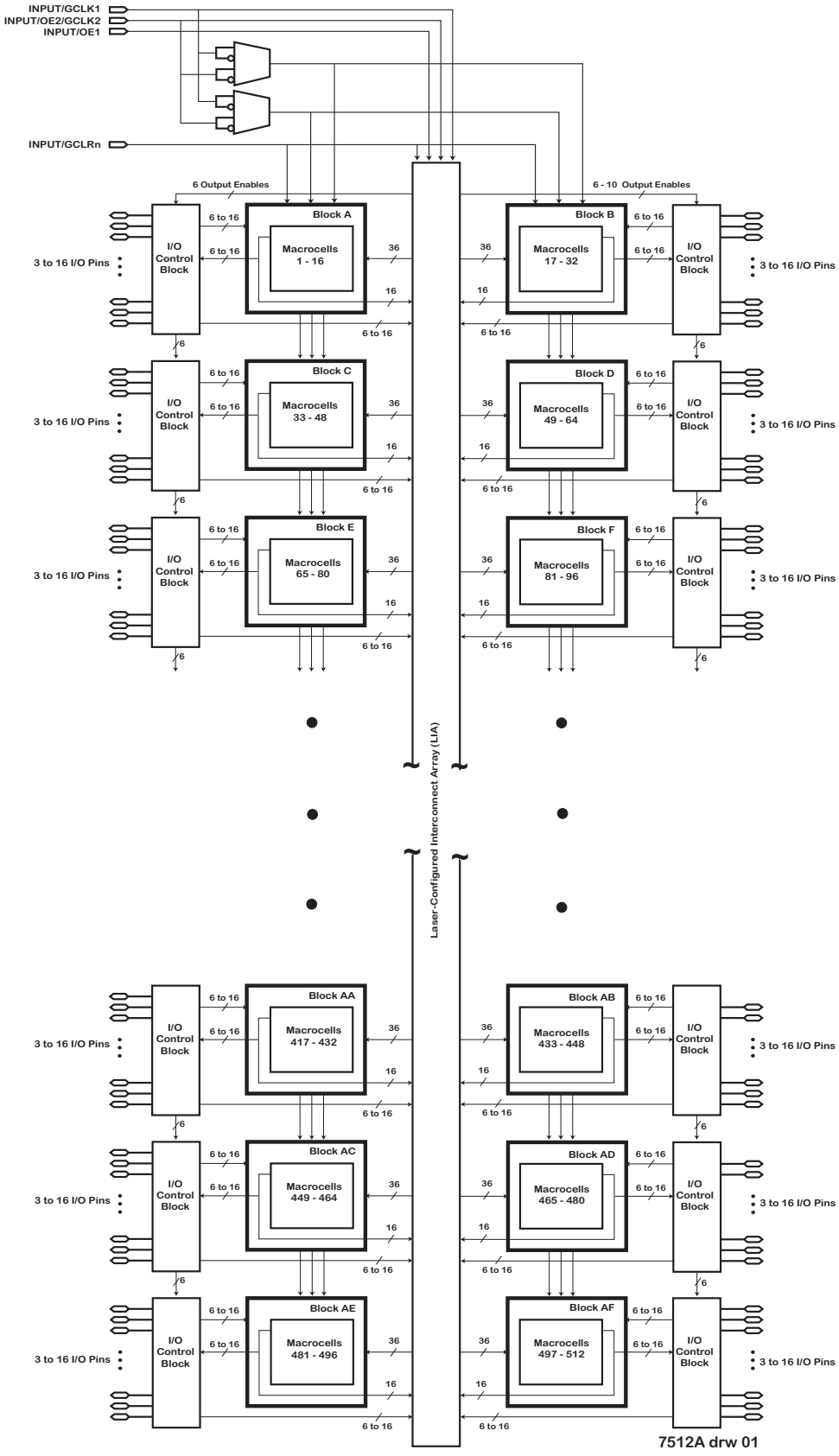
Additional Information

For further information on designing with the CL7000 LPLD family, please consult the following documents:

- AN-01: Requesting a First Article. This document provides instructions on how to submit a bitstream file for generation of first articles.
- AN-02: Clear Logic Packaging Guide. This document provides specifications and drawings for packages used by the CL7000 family.
- AN-09: CL7000 Technology White Paper. This document outlines the technologies employed by the CL7000 LPLD family.
- AN-10: Calculating CL7000 Power Consumption. This document provides guidelines for calculating power consumption based on design characteristics.
- AN-11: CL7000 Test Methodology. This document discribes how Clear Logic provides 100% stuck-at fault coverage.

- AN-12: CL7000 LPLD Timing and Function Compatability. This document shows how a seamless conversion from CPLD to ASIC can be achieve with no additional engineering with Clear Logic.

Block Diagram



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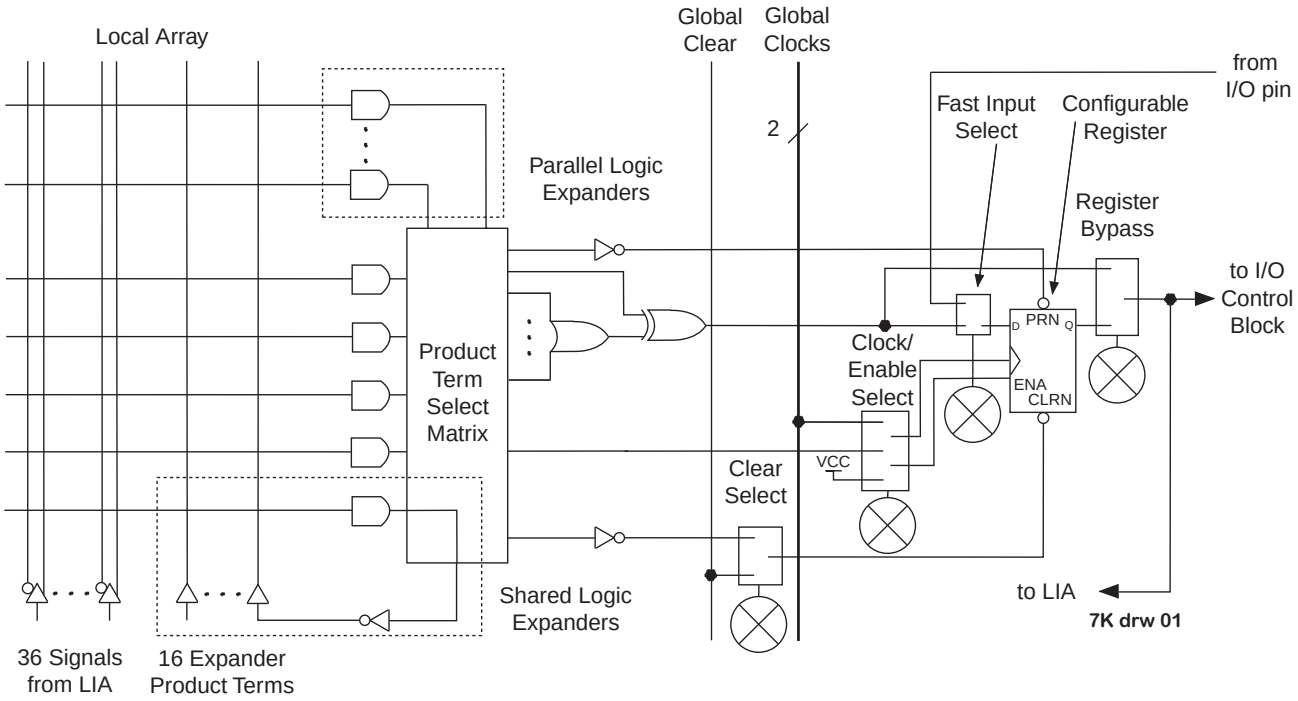
Macrocell Diagram



Pin Configuration

Pin Name	144 pin TQFP	208 pin PQFP	256 pin BGA	256 pin FBGA
INPUT/GCLK1	125	184	L1	D9
INPUT/GCLRn	127	182	K2	E8
INPUT/OE1	126	183	K1	E9
INPUT/OE2/GCLK2	128	181	K3	D8
TDI	4	176	A2	D4
TMS	20	127	B12	J6
TCK	89	30	V12	J11
TDO	104	189	Y2	D13
GNDINT	52, 57, 124, 129	75, 82, 180, 185	J20, K4, K18, L2, L17	A8, C9, G9, K8, P9
GND	3, 13, 17, 33, 59, 64, 85, 105, 135	14, 32, 50, 72, 94, 116, 134, 152, 174, 200	A1, B2, B19, B20, C3, C18, D4, D17, U4, U17, V3, V18, V19, W2, W19, Y1, Y20	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT	51, 58, 123, 130	74, 83, 179, 186	J1, J19, L4, M19, M20	B9, C8, G8, K9, P8
VCCIO	24, 50, 73, 76, 95, 115, 144	5, 23, 41, 63, 85, 105, 107, 125, 143, 165, 191, 207	C4, C17, D3, D5, D16, D18, E4, E17, T4, T17, U3, U5, U16, U18, V2, V4, V17	B3, B5, C14, E15, F11, G3, G7, G15, H9, J8, K10, L3, L6, M15, P14, T2, T3
NC (No Connect)	-	-	-	-
Total user I/O pins	**120**	**176**	**212**	**212**

7512A tbl 01

DC Electrical Specifications

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage, internal logic and input buffers		3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers 3.3 volt operation 2.5 volt operation		 3.0 2.3	 3.6 2.7	 V V
V_I	Input voltage		-0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient Operating temperature Commercial temperature range Industrial temperature range		 0 -40	 70 85	 °C °C
T_J	Ambient Operating temperature Commercial temperature range Industrial temperature range		 0 -40	 90 105	 °C °C
t_R	Input signal rise time			40	ns
t_F	Input signal fall time			40	ns
t_{RVCC}	V_{CC} rise time			100	ms

7KA tbl 02

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground	-0.5	4.6	V
V_I	DC input voltage[1]	With respect to ground	-2.0	5.8	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_A	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	Fineline BGA, PQFP, and TPFP packages, Under bias		135	°C

7KA tbl 03

DC Electrical Specifications cont.

DC Electrical Characteristics (over the operating range)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input Voltage		1.7	5.75	V
V_{IL}	Input LOW Voltage[1]		-0.5	0.8	V
V_{OH}	3.3-V high-level TTL output Voltage	I_{OH} = -8 mA DC, V_{CCIO} = 3.00 V	2.4		V
	3.3-V high-level CMOS output Voltage	I_{OH} = -0.1 mA DC, V_{CCIO} = 3.00 V	V_{CCIO}-0.2		V
	2.5-V high-level output Voltage	I_{OH} = -100 µA DC, V_{CCIO} = 2.30 V	2.1		V
		I_{OH} = -1 mA DC, V_{CCIO} = 2.30 V	2.0		
		I_{OH} = -2 mA DC, V_{CCIO} = 2.30 V	1.7		
V_{OL}	3.3-V high-level TTL output Voltage	I_{OH} = 8 mA DC, V_{CCIO} = 3.00 V		0.45	V
	3.3-V high-level CMOS output Voltage	I_{OH} = 0.1 mA DC, V_{CCIO} = 3.00 V		0.2	V
	2.5-V high-level output Voltage	I_{OH} = 100 µA DC, V_{CCIO} = 2.30 V		0.2	V
		I_{OH} = 1 mA DC, V_{CCIO} = 2.30 V		0.4	V
		I_{OH} = 2 mA DC, V_{CCIO} = 2.30 V		0.7	V
I_{IN}	Input Leakage Current	V_I = VCC or GND	-10	10	µA
I_{OZ}	Output Leakage Current	V_O = VCC or GND	-10	10	µA

7KA tbl 04

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

7KA tbl 05

AC Electrical Specifications

I/O Element Timing Parameters

			Speed: -6		Speed: -7		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C_L = 35 pF		6.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C_L = 35 pF		6.0		7.5	ns
t_{SU}	Global clock setup time		3.7		4.9		ns
t_H	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		ns
t_{FH}	Global clock hold time of fast input		0.5		0.0		ns
t_{CO1}	Global clock to output delay	C_L = 35 pF	1.0	3.3	1.0	4.5	ns
t_{CH}	Global clock high time		3.0		3.0		ns
t_{CL}	Global clock low time		3.0		3.0		ns
t_{ASU}	Array clock setup time		0.8		1.6		ns
t_{AH}	Array clock hold time		1.9		2.1		ns
t_{ACO1}	Array clock to output delay	C_L = 35 pF	1.0	6.2		7.8	ns
t_{ACH}	Array clock high time		3.0		3.0		ns
t_{ACL}	Array clock low time		3.0		3.0		ns
t_{CNT}	Minimum global clock period			6.4		8.4	ns
f_{CNT}	Maximum internal global clock frequency		156.3		119.0		MHz
t_{ACNT}	Minimum array clock period			6.4		8.4	ns
f_{ACNT}	Maximum internal array clock frequency		156.3		119.0		MHz

7Ka tbl 06B1

AC Electrical Specifications cont.

External Timing Parameters

			Speed: -10		Speed: -12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C_L = 35 pF		10.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C_L = 35 pF		10.0		12.0	ns
t_{SU}	Global clock setup time		6.6		7.8		ns
t_H	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C_L = 35 pF	1.0	5.9	1.0	7.1	ns
t_{CH}	Global clock high time		4.0		5.0		ns
t_{CL}	Global clock low time		4.0		5.0		ns
t_{ASU}	Array clock setup time		2.1		2.4		ns
t_{AH}	Array clock hold time		3.4		4.4		ns
t_{ACO1}	Array clock to output delay	C_L = 35 pF		10.4		12.5	ns
t_{ACH}	Array clock high time		4.0		5.0		ns
t_{ACL}	Array clock low time		4.0		5.0		ns
t_{CNT}	Minimum global clock period			11.2		13.3	ns
f_{CNT}	Maximum internal global clock frequency		89.3		75.2		MHz
t_{ACNT}	Minimum array clock period			11.2		13.3	ns
f_{ACNT}	Maximum internal array clock frequency		89.3		75.2		MHz

7KA tbl 06B2

AC Electrical Specifications cont.

Internal Timing Parameters[4]

Symbol	Parameter	Conditions	Speed: -6 Min	Speed: -6 Max	Speed: -7 Min	Speed: -7 Max	Unit
t_{IN}	Input pad and buffer delay			0.3		0.4	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.4	ns
t_{FIN}	Fast input delay			2.4		3.3	ns
t_{SEXP}	Shared expander delay			2.8		3.6	ns
t_{PEXP}	Parallel expander delay			0.5		0.8	ns
t_{LAD}	Logic array delay			2.5		3.7	ns
t_{LAC}	Logic control array delay			2.5		3.4	ns
t_{IOE}	Internal output enable delay			0.2		0.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		0.3		0.6	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		0.8		1.1	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		5.3		5.6	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		4.0		4.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		4.5		4.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C_L = 5 pF[3]		4.0		4.0	ns
t_{SU}	Register setup time		1.0		1.3		ns
t_H	Register hold time		1.7		2.4		ns
t_{FSU}	Register setup time of fast input		1.2		1.1		ns
t_{FH}	Register hold time of fast input		1.3		1.9		ns
t_{RD}	Register delay			1.6		2.1	ns
t_{COMB}	Combinatorial delay			1.6		1.5	ns
t_{IC}	Array clock delay			2.7		3.4	ns
t_{EN}	Register enable time			2.5		3.4	ns
t_{GLOB}	Global control delay			1.1		1.4	ns
t_{PRE}	Register preset time			2.3		3.9	ns
t_{CLR}	Register clear time			2.3		3.9	ns
t_{LIA}	LIA delay			1.3		1.3	ns

7KA tbl 07B1

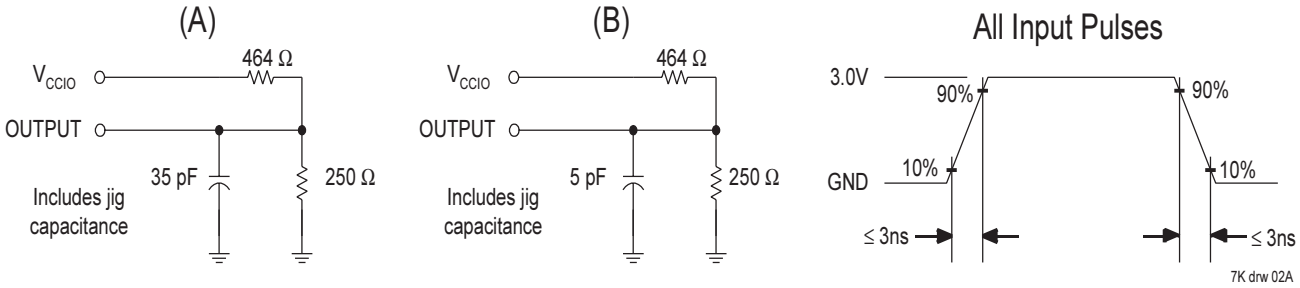
AC Electrical Specifications cont.

Internal Timing Parameters[4]

Symbol	Parameter	Conditions	Speed: -10 Min	Speed: -10 Max	Speed: -12 Min	Speed: -12 Max	Unit
t_{IN}	Input pad and buffer delay			0.6		0.7	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.7	ns
t_{FIN}	Fast input delay			3.7		4.1	ns
t_{SEXP}	Shared expander delay			4.9		5.9	ns
t_{PEXP}	Parallel expander delay			1.1		1.3	ns
t_{LAD}	Logic array delay			5.0		6.0	ns
t_{LAC}	Logic control array delay			4.6		5.6	ns
t_{IOE}	Internal output enable delay			0.0		0.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		0.7		0.9	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		1.2		0.4	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		5.7		5.9	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	C_L = 5 pF[3]		5.0		5.0	ns
t_{SU}	Register setup time		1.7		2.0		ns
t_{H}	Register hold time		3.8		4.8		ns
t_{FSU}	Register setup time of fast input		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.9		1.9		ns
t_{RD}	Register delay			2.8		3.3	ns
t_{COMB}	Combinatorial delay			2.0		2.4	ns
t_{IC}	Array clock delay			4.6		5.6	ns
t_{EN}	Register enable time			4.6		5.6	ns
t_{GLOB}	Global control delay			1.8		2.2	ns
t_{PRE}	Register preset time			5.2		6.2	ns
t_{CLR}	Register clear time			5.2		6.2	ns
t_{LIA}	LIA delay			1.7		2.0	ns

7KA tbl 07B2

AC Test Conditions



Notes to Tables

1. During transitions, inputs may undershoot to -2.0V for periods shorter than 20ns. Otherwise, minimum DC input voltage is 0.3V.

2. Typical values are at V_{CC} of 5.0 volts and ambient temperature of 25 ºC.

3. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.

4. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.

Revision History

11 Jan. 1999:	Created preliminary document.
31 July 1999:	Created full document.
13 Oct. 1999:	Corrected typographical error in AC Test Condition diagram (W changed to Ω) also corrected timing in 10ns External Timing Paramiters
1 Dec. 2000:	Updated application note reference.

Ordering Information

Part Number	Temperature Range	Package Type	Speed	Altera Equivalent
CL7512AETC144-15	Commercial	144-pin Thin QFP	-15	EPM7512AETC144-15
CL7512AETC144-10			-10	EPM7512AETC144-10
CL7512AETC144-7			-7	EPM7512AETC144-7
CL7512AETC144-6			-6	N/A
CL7512AEQC208-15		208-pin Plastic QFP	-15	EPM7512AEQC208-15
CL7512AEQC208-10			-10	EPM7512AEQC208-10
CL7512AEQC208-7			-7	EPM7512AEQC208-7
CL7512AEQC208-6			-6	N/A
CL7512AEQI208-10	Industrial		-10	EPM7512AEQI208-10
CL7512AEBC256-15	Commercial	256-pin Plastic BGA	-15	EPM7512AEBC256-15
CL7512AEBC256-10			-10	EPM7512AEBC256-10
CL7512AEBC256-7			-7	EPM7512AEBC256-7
CL7512AEBC256-6			-6	N/A
CL7512AEFC256-15		256-pin FBGA	-15	EPM7512AEFC256-15
CL7512AEFC256-10			-10	EPM7512AEFC256-10
CL7512AEFC256-7			-7	EPM7512AEFC256-7
CL7512AEFC256-6			-6	N/A

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