MCP2050

LIN Transceiver with Voltage Regulator

Features:

- The MCP2050 is compliant with:
  - LIN Bus Specifications Version 1.3, 2.1 and with SAE J2602-2
- Support Baud Rates Up to 20 kBaud
- 43V Load Dump Protected
- Maximum Continuous Input Voltage of 30V
- Wide LIN Compliant Supply Voltage, 6.0-18.0V
- Extended Temperature Range: -40 to +125°C
- Interface to PIC® EUSART and Standard USARTs
- Wake-Up on LIN Bus Activity or Local Wake Input
- LIN Bus Pin
  - Internal pull-up termination resistor and diode for slave node
  - Protected against V_{BAT} shorts
  - Protected against loss of ground
  - High current drive
- T_{XD} and LIN Bus Dominant Time-Out Function
- Two Low-Power Modes
  - Transmitter Off mode: 90 µA (typical)
  - Power Down mode: 4.5 µA (typical)
- Output Indicating Internal Reset State (POR or Sleep Wake)
- MCP2050 On-Chip Voltage Regulator
  - Output voltage of 5.0V or 3.3V with 70 mA capability and tolerances of ±3% over operating temperature range
  - Internal short-circuit current limit
  - Only external filter and load capacitors needed
- Programmable Windowed Watchdog Timer (WWDT)
  - External resistor programmable from 7 ms to 140 ms
  - Disabled by connecting the WWDTSELECT pin to V_{REG} or let the pin float
- Ratiometric Output of V_{BAT} Voltage Scaled to V_{REG}
- Automatic Thermal Shutdown
- High Electromagnetic Immunity (EMI), Low Electromagnetic Emission (EME)
- Robust ESD Performance: ±15 kV for L_{BUS} and V_{BB} pin (IEC61000-4-2)
- Transient Protection for L_{BUS} and V_{BB} Pins in Automotive Environment (ISO7637)
- Meets Stringent Automotive Design Requirements Including “OEM Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications”, Version 1.3, May 2012
- Multiple Package Options Including Small 5x5 QFN

Description:

The MCP2050 provides a bidirectional, half-duplex communication physical interface to meet the LIN bus specification Revision 2.1 and SAE J2602. The device incorporates a voltage regulator with 5V or 3.3V 70 mA regulated power supply output. The on-chip WWDT allows users to adjust the size of the reset window by using an external resistor. The ratiometric V_{BAT} pin scales down V_{BAT} to the range of V_{REG} so it can be monitored by an A/D converter.

The device has been designed to meet the stringent quiescent current requirements of the automotive industry and will survive +43V load dump transients, and double battery jumps.

MCP2050 family members:

- MCP2050-500, 14-pin, LIN driver with 5.0V regulator
- MCP2050-330, 14-pin, LIN driver with 3.3V regulator
- MCP2050-500, 20-pin QFN, LIN driver with 5.0V regulator
- MCP2050-330, 20-pin QFN, LIN driver with 3.3V regulator

LOCAL INTERCONNECT NETWORK

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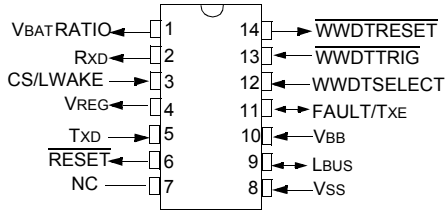
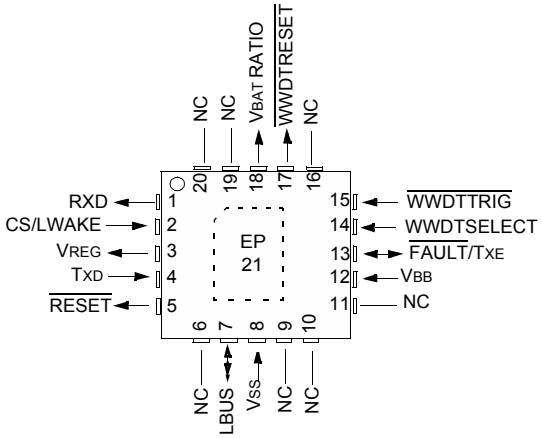
Package Types

MCP2050
PDIP, SOIC

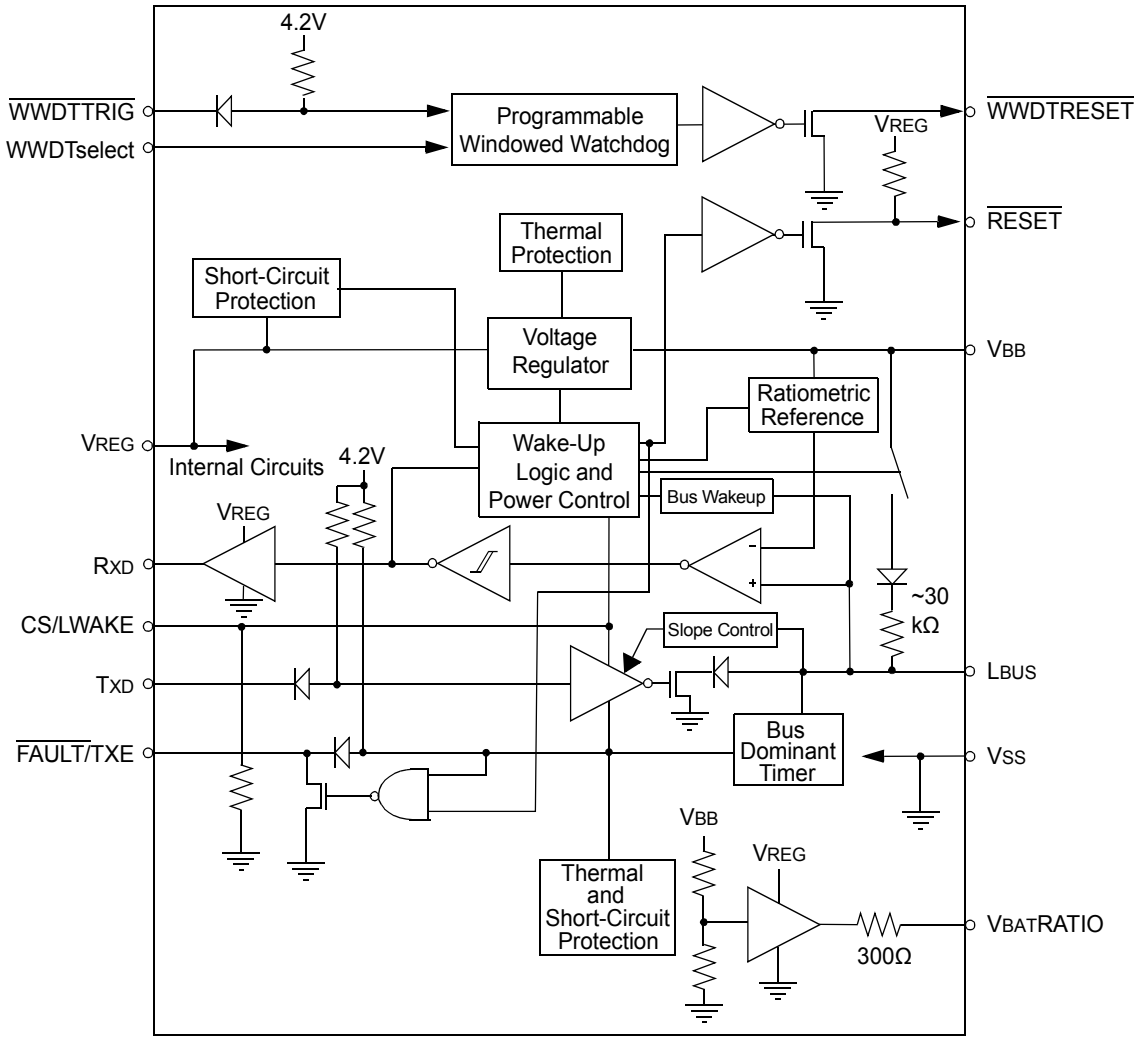


MCP2050
5 x 5 QFN*



* Includes Exposed Thermal Pad (EP), see Table 1-2.

Block Diagram



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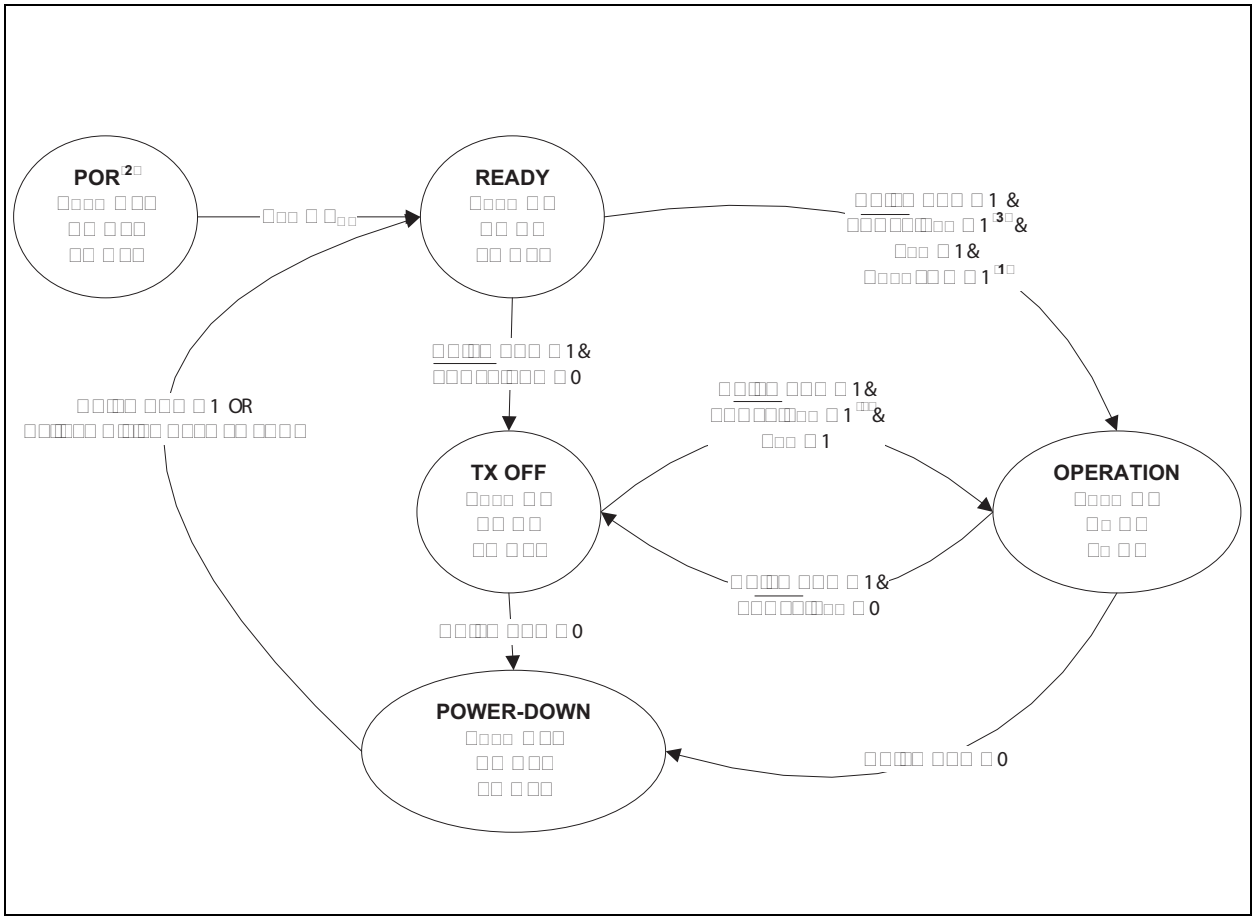
1.0 FUNCTION DESCRIPTION

The MCP2050 provides a physical interface between a microcontroller and a LIN half-duplex bus. It is intended for automotive and industrial applications with serial bus baud rates up to 20 kbaud. This device will translate the CMOS/TTL logic levels to LIN logic levels, and vice versa. The device offers optimum EMI and ESD performance; it can withstand high voltage on the LIN bus. The device supports two low-power modes to meet automotive industry power consumption requirements. The MCP2050 also provides a +5V or 3.3V 70 mA regulated power output.

1.1 Modes of Operation

The MCP2050 works in five modes: Power-On Reset mode, Power-Down mode, Ready mode, Operation mode, and Transmitter Off mode. For an overview of all operational modes, please refer to Table 1-1. For the operational mode transition, please refer to Figure 1-1.

FIGURE 1-1: STATE DIAGRAM



Note 1: VREG_OK: Regulator Output Voltage > 0.8VREG_NOM.

2: If the voltage on pin VBB falls below VOFF, the device will enter Power-On Reset mode from all other modes, which is not shown in the figure.

3: $\overline{\text{FAULT}}$/TXE = 1 represents input and no fault conditions. $\overline{\text{FAULT}}$/TXE = 0 represents input low or a fault condition. Refer to Table 1-3.

1.1.1 POWER-ON-RESET MODE

Upon application of V_{BB}, or whenever the voltage on V_{BB} is below the threshold of regulator turn-off voltage V_{OFF} (typically. 4.50V), the device enters Power-On Reset mode (POR). During this mode, the device maintains the digital section in a reset mode and waits until the voltage on pin V_{BB} rises above the threshold of regulator turn-on voltage V_{ON} (typically 5.75V) to enter into Ready mode. In Power-On-Reset mode, the LIN physical layer and voltage regulator are disabled, and $\overline{RESET}$ output is forced to low.

1.1.2 READY MODE

The device enters Ready mode from POR mode after the voltage on V_{BB} rises above the threshold of regulator turn-on voltage V_{ON} or from Power-Down mode when a remote or local wake-up event happens.

Upon entering Ready mode, the voltage regulator and receiver section of the transceiver are powered up. The transmitter remains in off state. The device is ready to receive data but not to transmit. In order to minimize the power consumption, the regulator operates in a reduced-power mode. It has a lower GBW product and thus is slower. However, the 70 mA drive capability is unchanged.

The device stays in Ready mode until the output of the voltage regulator has stabilized and the CS/LWAKE pin is high (‘1’).

1.1.3 OPERATION MODE

If V_{REG} is OK (V_{REG} > 0.8 V_{REG_NOM}), CS/LWAKE pin, $\overline{FAULT}/T_{XE}$ pin and T_{XD} pin are high, the part enters the Operation mode from either Ready or Transmitter Off mode.

In this mode, all internal modules are operational. The internal pull-up resistor between L_{BUS} and V_{BB} is connected only in this mode.

The device goes into the Power-Down mode at the falling edge on CS/$\overline{LWAKE}$; or to the Transmitter Off mode at the falling on $\overline{FAULT}/T_{XE}$ while CS/LWAKE stays high.

1.1.4 TRANSMITTER OFF MODE

In Transmitter Off mode, the receiver is enabled but the L_{BUS} transmitter is off. It is a lower-power mode.

In order to minimize the power consumption, the window watchdog timer is disabled and the regulator operates in a reduced-power mode. It has a lower GBW product and thus is slower. However, the 70 mA drive capability is unchanged.

The transmitter may be re-enabled whenever the $\overline{FAULT}/T_{XE}$ signal returns high, by removing the internal fault condition and the CPU returning the $\overline{FAULT}/T_{XE}$ high. The transmitter will not be enabled even if the $\overline{FAULT}/T_{XE}$ pin is brought high externally, when the internal fault is still present. However, externally forcing the $\overline{FAULT}/T_{XE}$ high, while the internal fault is still present, should be avoided since this will induce high current and power dissipation in the $\overline{FAULT}/T_{XE}$ pin.

The transmitter is also turned off whenever the voltage regulator is unstable or recovering from a fault. This prevents unwanted disruption of the bus during times of uncertain operation.

1.1.5 POWER-DOWN MODE

In Power-Down mode, the transceiver and the voltage regulator are both off. Only the Bus Wake-up section and the CS/LWAKE pin wake-up circuits are in operation. This is the lowest-power mode.

If any bus activity (e.g. a BREAK character) occurs during Power-Down mode, the device will immediately enter Ready mode and enable the voltage regulator. Then, once the regulator output has stabilized (approximately 0.3 ms to 1.2 ms) it goes to Operation mode. Refer to **Section 1.1.6 “Remote Wake-up”** for more details.

The part will also enter Ready mode from Power-Down mode, followed by Operation mode, if the CS/LWAKE pin becomes active high (‘1’).

1.1.6 REMOTE WAKE-UP

The remote wake-up sub module observes the L_{BUS} in order to detect bus activity. In Power-Down mode, normal LIN recessive/dominant threshold is disabled, and the LIN bus Wake-Up Voltage Threshold $V_{WK(LBUS)}$ is used to detect bus activities. Bus activity is detected when the voltage on the L_{BUS} falls below the LIN bus Wake-Up Voltage Threshold $V_{WK(LBUS)}$ (approximately 3.4V) for at least t_{BDB} (a typical duration of 80 µs) followed by a rising edge. Such a condition causes the device to leave Power-Down mode

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TABLE 1-1: OVERVIEW OF OPERATIONAL MODES

State	Transmitter	Receiver	Internal Wake Module	Voltage Regulator	Watch Dog Timer	Operation	Comments
PoR	Off	Off	Off	Off	Off	Proceed to Ready mode after $V_{BB}>V_{ON}$.	—
Ready	Off	On	Off	On	On	If CS/LWAKE high, then proceed to Operation or Transmitter Off mode.	Bus Off state
Operation	On	On	Off	On	On	If CS/LWAKE low level, then proceed to Power-Down. If $\overline{FAULT}$/TxE low level, then Transmitter-Off mode.	Normal Operation mode
Power-Down	Off	Off	On Activity Detect	Off	Off	On LIN bus rising edge or CS/LWAKE high level, proceed to READY mode.	Lowest-Power mode
Transmitter Off	Off	On	Off	On	Off	If CS/LWAKE low level, then proceed to Power down. If $\overline{FAULT}$/TxE high, then Operation mode.	Bus Off state, Lower-Power mode

1.2 Windowed Watchdog Reset

The Watchdog Timer monitors for activity on the Windowed Watchdog Timer Trigger input pin $\overline{WWDTTRIG}$. The $\overline{WWDTTRIG}$ pin is expected to be strobed within a given time frame. When this time frame has expired without an edge transition on the $\overline{WWDTTRIG}$ pin, the $\overline{WWDTRESET}$ pin is driven active (low) to reset the system. This feature is enabled by connecting a resistor between the WWDTSELECT pin and VSS. Monitoring is then done by requiring the host processor to force a falling edge transition on the $\overline{WWDTTRIG}$ pin within a predetermined time frame (TWD).

The start time of the trigger window is fixed at 50% of the total watchdog period, after the last trigger. The length of the window is determined by the value of the resistor on pin WWDTSELECT. The Watchdog Timer is disabled if WWDTSELECT is floating.

1.2.1 WWDT DURING INITIAL POWER-UP

The $\overline{WWDTRESET}$ is driven high after a power-on reset. The Watchdog Timer begins counting at this point, awaiting an edge on $\overline{WWDTTRIG}$ pin. Note that there is no window enabled, yet. If no falling edge is detected on the $\overline{WWDTTRIG}$ pin before the timer expires, the $\overline{WWDTRESET}$ is pulse low and the timer is restarted. When a trigger edge on the $\overline{WWDTTRIG}$ pin is seen, the window is enabled and the timer is reset.

FIGURE 1-2: $\overline{WWDTRESET}$ DURING INITIAL POWER-UP

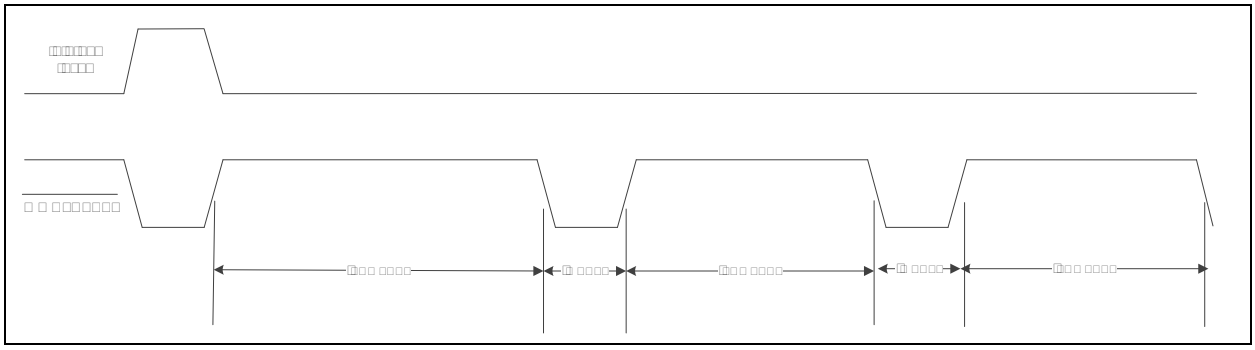

Figure 1-2 shows the behavior of the $\overline{WWDTRESET}$ pin after a system reset with no trig at all. If no trig is given during the power-up window, $\overline{WWDTRESET}$ is reset low for the time tWDRST.

The power-up window length tPOWERUP duration is determined by the value of the resistor connected between pin WWDTSELECT and pin VSS, while the reset pulse duration is about 150 µs.

Duration for tPOWERUP and tWDRST are:

- tPOWERUP = 0.8 ms x (RWWDTSELECT+1) typical
- tWDRST = 150 µs typical
- RWWDTSELECT is in kΩ.

Once a trig is asserted, the power-up sequence “stops” and the normal behavior begins.

1.2.2 WINDOWED WATCHDOG BEHAVIOR

After windowed watchdog begins its normal behavior, three different cases can appear.

- A pulse (falling edge) on the $\overline{\text{WWDTTRIG}}$ pin is detected within the trigger window; the watchdog timer will be reset, and a new watchdog period will begin; $\overline{\text{WWDTRESET}}$ pin remains high (Figure 1-3.)
- A pulse (falling edge) on the $\overline{\text{WWDTTRIG}}$ pin is detected before the trigger window (too early trigger); $\overline{\text{WWDTRESET}}$ is asserted (low) immediately after the falling edge is detected for approximately t_{WDRST}; the counter is reset and the next watchdog period begins at the rising edge of the voltage on $\overline{\text{WWDTRESET}}$ pin (Figure 1-12).
- No pulse on the $\overline{\text{WWDTTRIG}}$ pin is detected during the whole watchdog window (no trigger); $\overline{\text{WWDTRESET}}$ is asserted (low) for approximately t_{WDRST} when the timer has expired; the counter is reset and the next watchdog period begins at the rising edge of the voltage on $\overline{\text{WWDTRESET}}$ pin (Figure 1-5).

The trigger window is between 50% to 100% of the watchdog window length, $t_{WLENGTH}$. The window length is determined by the external resistor between WWDTSELECT pin and V_{SS}.

EQUATION 1-1:

$$t_{WLENGTH} = (0.175\ \text{ms} \times R_{WWDTSELECT}) + 1.2\ \text{typical}$$

t_{WDRST} = 150 µs typical

$R_{WWDTSELECT}$ is in kΩ; its value ranges from 33 kΩ to 680 kΩ and window length ranges from 7 ms to 120 ms typical.

If the WWDTSELECT pin is floating, the watchdog is disabled and the $\overline{\text{WWDTRESET}}$ remains high.

FIGURE 1-3: CORRECT TRIGGER

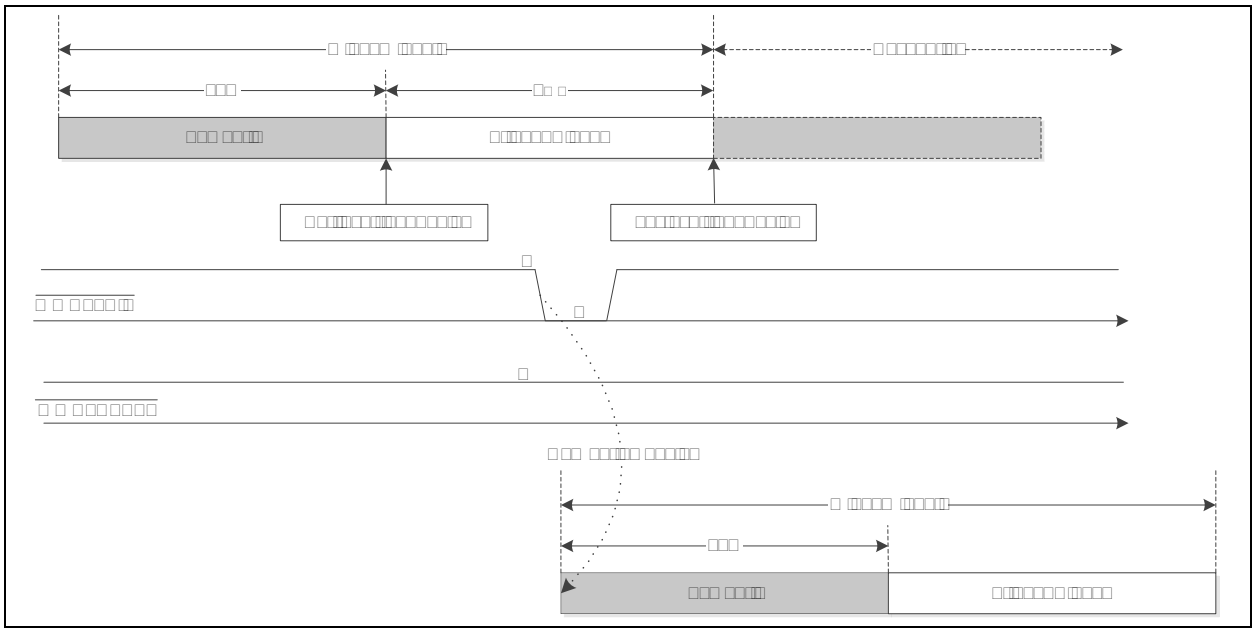

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FIGURE 1-4: TOO EARLY TRIGGER

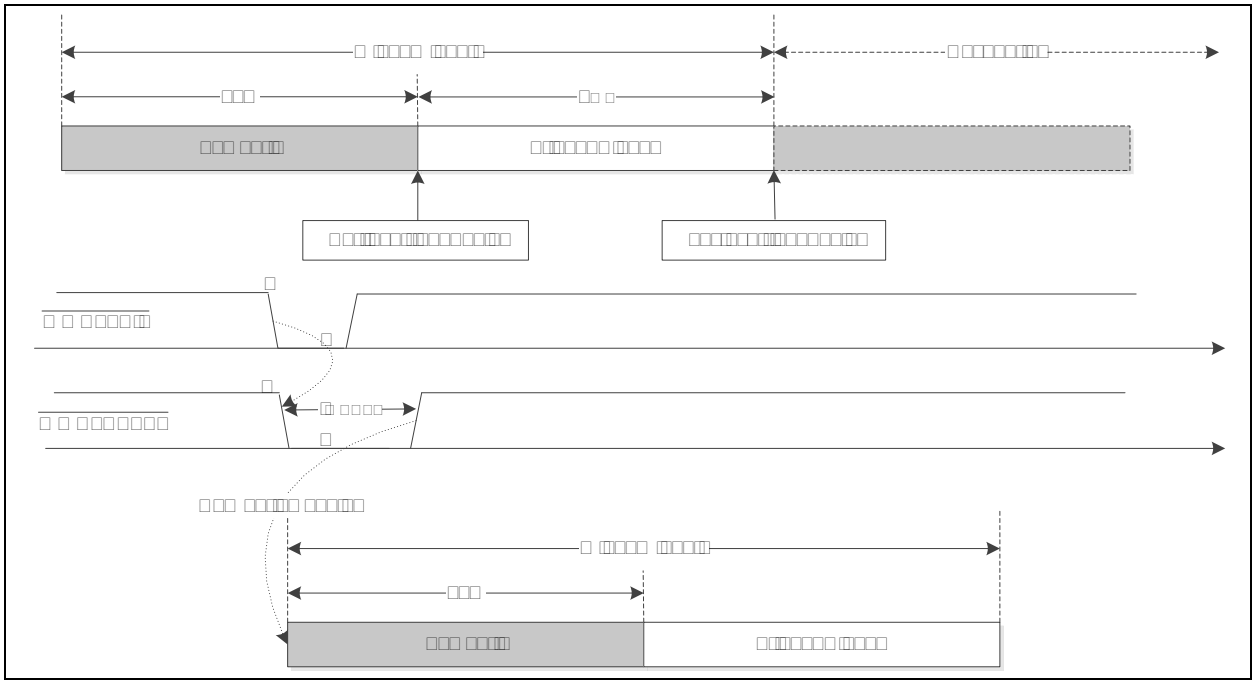
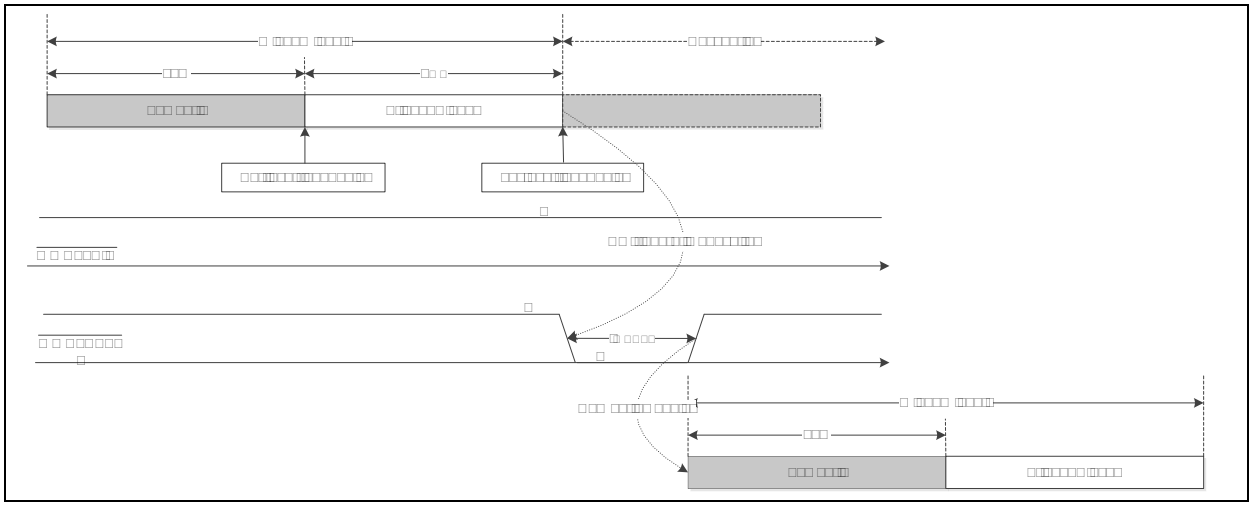


FIGURE 1-5: NO TRIGGER



1.3 Pin Descriptions

Please refer to Table 1-2 for the pinout overview.

TABLE 1-2: PINOUT DESCRIPTIONS

PIN Name	Devices		PIN Type	Function
	14-Pin PDIP, SOIC	5 x 5 QFN		Normal Operation
VBATRATIO	1	18	Analog Output	VBATRATIO = VBAT/24 × VREG
RXD	2	1	Output	Receive Data Output
CS/LWAKE	3	2	TTL Input, HV-tolerant	Chip Select and Local Wake-up Input
VREG	4	3	Output	Voltage Regulator Output
TXD	5	4	Input, HV-tolerant	Transmit Data Input
$\overline{\text{RESET}}$	6	5	Output	Reset Output
NC	7	6,9,10,11, 16,19,20	Not Connected	—
VSS	8	8	Power	Ground
LBUS	9	7	I/O, HV	LIN Bus
VBB	10	12	Power	Battery
$\overline{\text{FAULT}}$/TXE	11	13	I/O, HV-tolerant	Fault Detect Output/Transmitter Enable Input
WWDTSELECT	12	14	Input	A Resistor between this pin and Ground determines the Watchdog Window length
$\overline{\text{WWDTTRIG}}$	13	15	Input	Windowed Watchdog Trigger Input
$\overline{\text{WWDTRESET}}$	14	17	Output, HV-tolerant	Windowed Watchdog Reset Output
EP	—	21	Exposed Thermal Pad (EP)	Exposed Thermal Pad can be left unconnected, or connected to the ground.

1.3.1 VBATRATIO

This is an analog output pin that reflects the voltage at the VBAT pin. It is scaled by VREG such that:

VBATRATIO = VBAT/24 × VREG

0 <= VBATRATIO <= VREG

The resistive divider and the output driver are switched off during Power-Down mode in order to reduce power consumption.

1.3.2 RXD

Receive Data Output pin. The RXD pin is a standard CMOS output pin and it follows the state of the LBUS pin.

1.3.3 CS/LWAKE

Chip Select and Local Wake-Up Input pin (TTL level, high voltage tolerant). This pin controls the device state transition. Refer to Figure 1-1.

If CS/LWAKE = 1, the device can work in Operation mode ($\overline{\text{FAULT}}$/TXE = 1) or Transmitter Off mode ($\overline{\text{FAULT}}$/TXE = 0).

If CS/LWAKE = 0, the device can work in Power-Down mode or Ready mode.

An internal pull-down resistor will keep the CS/LWAKE pin low to ensure that no disruptive data will be present on the bus while the microcontroller is executing a Power-on Reset and I/O initialization sequence. When CS/LWAKE is '1', a weak pull-down (~600 kΩ) is used to reduce current. When CS/LWAKE is '0' a stronger pull-down (~300 kΩ) is used to maintain the logic level.

This pin may also be used as a local wake-up input (see Figure 1-12). The microcontroller will set the I/O pin to control the CS/LWAKE. An external switch, or other source, can then wake-up both the transceiver and the microcontroller.

Note: CS/LWAKE should NOT be tied directly to pin VREG as this could force the MCP2050 into Operation Mode before the microcontroller is initialized.

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1.3.4 VREG

Positive Supply Voltage Regulator Output pin. An on-chip LDO gives +5.0 or +3.3V 70 mA regulated voltage on this pin.

1.3.5 TXD

Transmit Data Input pin (TTL level, HV compliant, adaptive pull-up). The transmitter reads the data stream on TXD pin and sends it to LIN bus. The LBUS pin is low (dominant) when TXD is low, and high (recessive) when TXD is high.

The Transmit Data Input pin has an internal adaptive pull-up to an internally-generated 4.2V (approximate). When TXD is '0', a weak pull-up (~900 kΩ) is used to reduce current. When TXD is '1' a stronger pull-up (~300 kΩ) is used to maintain the logic level. A series reverse-blocking diode allows applying TXD input voltages greater than the internally generated 4.2V and renders TXD pin HV compliant up to 30V (see the Block Diagram on page 2).

1.3.6 $\overline{\text{RESET}}$

Reset Output pin. This pin is open drain with ~90 kΩ pull-up to VREG. It indicates the internal voltage has reached a valid, stable level. As long as the internal voltage is valid (above 0.8VREG), this pin will remain high ('1'); otherwise the $\overline{\text{RESET}}$ pin switches to low ('0').

1.3.7 VSS

Ground pin.

1.3.8 LBUS

LBUS is a bidirectional LIN bus Interface pin and is controlled by the signal TXD. It has an open collector output with a current limitation. To reduce electromagnetic emission, the slopes during signal changes are controlled, and the LBUS pin has corner-rounding control for both falling and rising edges.

The internal LIN receiver observes the activities on LIN bus, and generates the output signal RXD that follows the state of the LBUS. A first degree 160 kHz, low-pass input filter optimizes electromagnetic immunity.

1.3.9 VBB

Battery Positive Supply Voltage pin. An external diode is connected in series to prevent the device from being reversely powered (refer Figure 1-12).

1.3.10 $\overline{\text{FAULT}}$/TXE

Fault Detect Output/Transmitter Enable Input pin. The output section is HV tolerant open drain (up to 30V). The input section is identical with TXD section (TTL level, HV compliant, adaptive pull-up). The internal pull-up resistor may be too weak for some applications. An external 10kΩ pull-up resistor is recommended to ensure a logic high level. Its state is defined as shown in Table 1-3. The device is placed in Transmitter Off mode whenever this pin is low ('0'), either from an internal fault condition or by external drive.

If CS/LWAKE is high ('1'), the $\overline{\text{FAULT}}$/TXE signals a mismatch between the TXD input and the LBUS level. This can be used to detect a bus contention. Since the bus exhibits a propagation delay, the sampling of the internal compare is debounced to eliminate false faults.

After the device wakes up, the $\overline{\text{FAULT}}$/TXE indicates what wakes the device if CS/LWAKE remains low ('0') (refer to Table 1-3).

The $\overline{\text{FAULT}}$/TXE pin sampled at a rate faster than every 10 µs.

1.3.11 WWDTSELECT

This is an analog input pin that sets the open window time to accept a trigger reset. A resistor between this pin and VSS sets this time. The equation to determine the value of the resistor can be found in **Section 1.2.2 "Windowed Watchdog Behavior"**.

1.3.12 $\overline{\text{WWDTTRIG}}$

This is an input pin to reset the Windowed Watchdog Timer. A high-to-low transition during the open window time will reset the timer and prevent the WWDT from timing out. The pin has an internal adaptive pull-up to an internally-generated 4.2V (approximate.).

When $\overline{\text{WWDTTRIG}}$ is '0', a weak pull-up (~800 kΩ) is connected to reduce current.

When $\overline{\text{WWDTTRIG}}$ is '1', the pull-up is stronger to maintain the logic level.

1.3.13 $\overline{\text{WWDTRESET}}$

$\overline{\text{WWDTRESET}}$ is an open-drain output pin. This pin is asserted low when the internal Windowed Watchdog Timer has expired or an attempt was made to clear the timer before the window has opened.

1.3.14 EP

It is recommended to connect this pad to VSS to enhance electromagnetic immunity and thermal resistance.

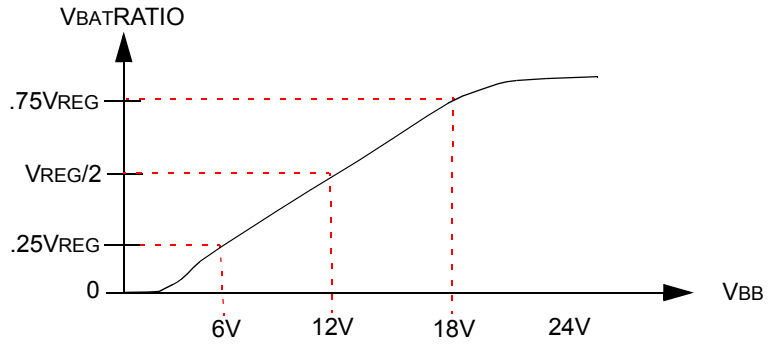
TABLE 1-3: $\overline{\text{FAULT}}$/TXE TRUTH TABLE

TXD In	RXD Out	LIN BUS I/O	Thermal Override	$\overline{\text{FAULT}}$/TXE		Definition
				External Input	Driven Output	
CS = 1						
L	H	VBB	OFF	H	L	**FAULT**, TXD driven low, LBUS shorted to VBB **(Note 1),** or LBUS/TXD permanent dominant detected, and transmit time-out shutdown.
H	H	VBB	OFF	H	H	**OK**
L	L	GND	OFF	H	H	**OK**
H	L	GND	OFF	H	H	**OK**, data is being received from LBUS
x	x	VBB	ON	H	L	**FAULT**, transceiver in thermal shutdown
x	x	VBB	x	L	x	**NO FAULT**, the CPU is commanding the transceiver to turn off the transmitter driver
CS = 0 after a wake-up						
x	x	x	x	x	L	**Wake-up from LIN bus activity**
x	x	x	x	x	H	**Wake-up from POR**

Legend: x = don't care

Note 1: The $\overline{\text{FAULT}}$/TXE is valid after approximately 25 µs after TXD falling edge. This is to eliminate false fault reporting during bus propagation delays.

FIGURE 1-6: VBATRATIO OUTPUT RANGE



Note 1: Linear range of VBATRATIO is between VBB = 6.0-18.0V.

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1.4 Fail-Safe Features

1.4.1 GENERAL FAIL-SAFE FEATURES

- An internal pull-down resistor on the CS/LWAKE pin disables the transmitter if the pin is floating.
- An internal pull-up resistor on the TXD pin places TXD in high, thus the LBUS is recessive if the TXD pin is floating.
- High-Impedance and low leakage current on LBUS during loss of power or ground.
- The current limit on LBUS protects the transceiver from being damaged if the pin is shorted to VBB.

1.4.2 THERMAL PROTECTION

The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter and voltage regulator.

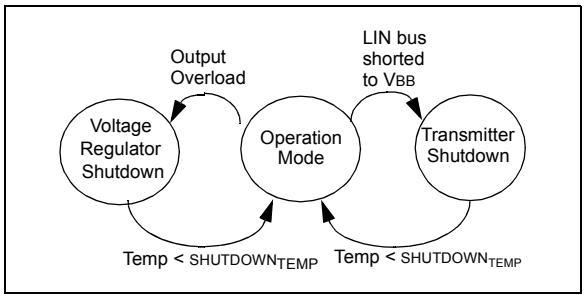
There are three causes for a thermal overload. A thermal shut down can be triggered by any one, or a combination of, the following thermal overload conditions.

- Voltage regulator overload
- LIN bus output overload
- Increase in die temperature due to increase in environment temperature

The recovery time from the thermal shutdown is equal to adequate cooling time.

Driving the TXD and checking the RXD pin makes it possible to determine whether there is a bus contention (TXD = high, RXD = low) or a thermal overload condition (TXD = low, RXD = high).

FIGURE 1-7: THERMAL SHUTDOWN STATE DIAGRAMS



1.4.3 TXD/LBUS TIME-OUT TIMER

LIN bus can be driven to a dominant level either from TXD pin or externally. An internal timer deactivates the LBUS transmitter if a dominant status (low) on LIN bus lasts longer than Bus Dominant Time-Out Time tTO(LIN) (approximately 20 ms); at the same time, RXD output is put in recessive (high), $\overline{\text{FAULT}}$/TXE is also driven to low and the internal LIN pull-up resistor is disconnected. The timer is reset on any recessive LBUS status or POR mode. The recessive status on LBUS can be caused either by the bus being externally pulled up or by TXD pin being returned high.

1.5 Internal Voltage Regulator

The MCP2050 has a positive regulator capable of supplying +5.0V or +3.3V at up to 70 mA of load current with tolerances of ±3% over the entire operating temperature range of -40°C to +125°C. The regulator uses an LDO design, is short-circuit-protected and will turn the regulator output off if its output falls below the Shutdown Voltage Threshold VSD.

With a load current of 70 mA, the minimum input-to-output voltage differential required for the output to remain in regulation is typically +0.5V (+1V maximum over the full operating temperature range). Quiescent current is less than 100 µA with a full 70 mA load current when the input-to-output voltage differential is greater than +3.00V.

Regarding the correlation between VBB, VREG and IDD, refer to Figure 1-9 and Figure 1-10. When the input voltage (VBB) drops below the differential needed to provide stable regulation, the voltage regulator output VREG will track the input down to approximately VOFF. The regulator will turn off the output at this point. This will allow PIC® microcontrollers, with internal POR circuits, to generate a clean arming of the Power-on Reset trip point. The MCP2050 will then monitor VBB and turn on the regulator when VBB is above the threshold of regulator turn-on voltage VON.

Under specific ambient temperature and battery voltage range, the voltage regulator can output as high as 150 mA current.

For current load capability of the voltage regulator, refer to Figure 1-9 and Figure 1-10.

In Power-Down mode, the VBB monitor is turned off.

Note: The regulator overload current limit is approximately 250 mA. The regulator output voltage VREG is monitored. If output voltage VREG is lower than VSD, the voltage regulator will turn off. After a recovery time of about 3 ms, the VREG will be checked again. If there is no short circuit, (VREG > VSD) then the voltage regulator remains on.

The regulator requires an external output bypass capacitor for stability. See Figure 2-1 for correct capacity and ESR for stable operation.

Note: A ceramic capacitor of at least 10 µF, or a tantalum capacitor of at least 2.2 µF is recommended for stability.

Warning: In worst-case scenarios, the ceramic capacitor may derate by 50%, based on tolerance, voltage and temperature. Therefore, in order to ensure stability, ceramic capacitors smaller than 10 µF may require a small series resistance to meet the ESR requirements, as shown in Table 1-4.

TABLE 1-4: RECOMMENDED SERIES RESISTANCE FOR CERAMIC CAPACITORS

Resistance	Capacitor
1Ω	1 µF
0.47Ω	2.2 µF
0.22Ω	4.7 µF
0.1Ω	6.8 µF

FIGURE 1-8: VOLTAGE REGULATOR BLOCK DIAGRAM

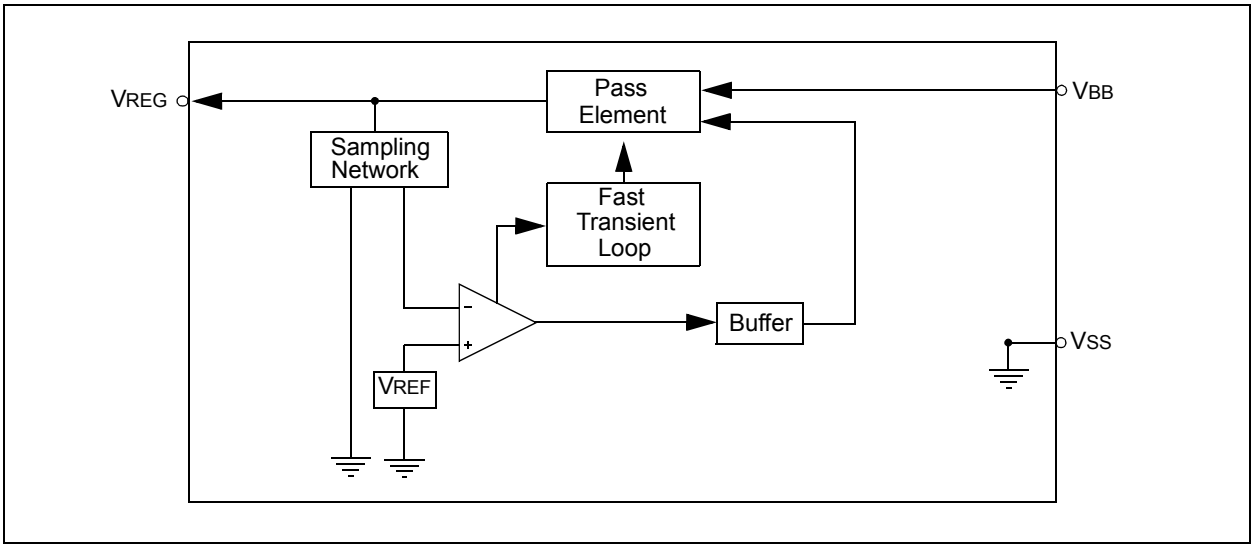


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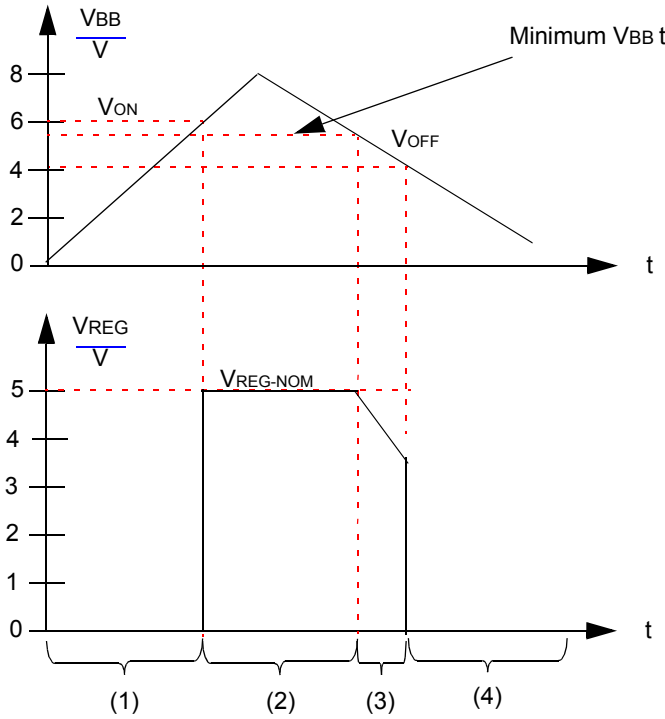
FIGURE 1-9: VOLTAGE REGULATOR OUTPUT ON POWER-ON RESET



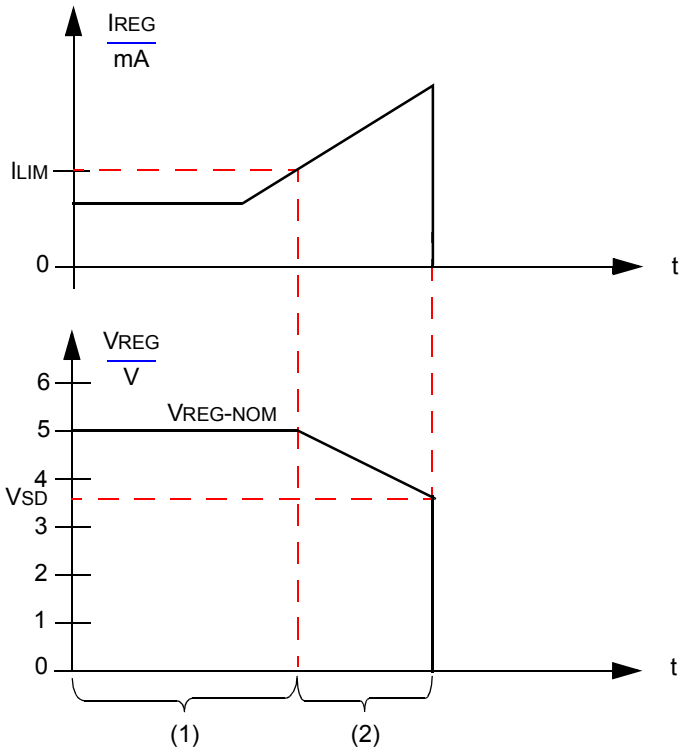
Note 1: Start-Up, $V_{BB} < V_{ON}$, regulator off.

2: $V_{BB} > V_{ON}$, regulator on.

3: $V_{BB} \leq$ minimum V_{BB} to maintain regulation.

4: $V_{BB} < V_{OFF}$, regulator will turn off.

FIGURE 1-10: VOLTAGE REGULATOR OUTPUT ON OVER CURRENT SITUATION



Note 1: IREG less than ILIM, regulator on.

2: After IREG exceeds ILIM, the voltage regulator output will be reduced until VSD is reached.

1.6 Optional External Protection

1.6.1 REVERSE BATTERY PROTECTION

An external reverse-battery-blocking diode should be used to provide polarity protection (see Figure 1-12).

1.6.2 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 43V transient suppressor (TVS) diode, between VBB and ground, with a transient protection resistor (RTP) in series with the battery supply and the VBB pin protects the device from power transients and ESD events greater than 43V (see Figure 1-12). The maximum value for the RTP protection resistor depends on two parameters: the minimum voltage the part will start at, and the impacts of this RTP resistor on the VBB value, thus on the Bus recessive level and slopes.

This leads to a set of three equations to fulfill.

Equation 1-2 provides a max RTP value according to the minimum battery voltage the user wants the part to start at.

Equation 1-3 provides a max RTP value according to the maximum error on the recessive level thus VBB since the part uses VBB as the reference value for the recessive level.

Equation 1-4 provides a max RTP value according to the maximum relative variation the user can accept on the slope when IREG varies.

Since both Equation 1-2 and Equation 1-3 must be fulfilled, the maximum allowed value for RTP is thus the smaller of the two values found when solving Equation 1-2 and Equation 1-3.

Usually Equation 1-2 gives the higher constraint (smaller value) for RTP as shown in the following example where VBATmin is 8V.

However, the user needs to check that the value found with Equation 1-2 also fulfills Equation 1-3 and Equation 1-4.

While this protection is optional, it should be considered as good engineering practice.

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EQUATION 1-2:

$$R_{TP} \leq \frac{V_{BATmin} - 5.5V}{250mA}$$

$$5.5V = V_{OFF} + 1.0V$$

250 mA is the peak current at power-on when VBB =5.5V

Assume VBATMIN = 8V. Equation 1-2 shows 10Ω.

EQUATION 1-3:

$$R_{TP} \leq \frac{\Delta V_{RECESSIVE}}{I_{REGMAX}}$$

Where:

ΔVRECESSIVE = Maximum variation tolerated on the recessive level

Assume ΔVRECCESSIVE = 1V and IREGMAX = 50 mA Equation 1-3 shows 20Ω.

EQUATION 1-4:

$$R_{TP} \leq \frac{\Delta Slope \times (V_{BATMIN} - 1V)}{I_{REGMAX}}$$

Where:

ΔSlope = Maximum variation tolerated on the slope level

IREGMAX = Maximum current the current will provide to the load

VBATMIN > VOFF + 1.0V

Assume ΔSlope = 15%, VBATMIN = 8V and IREGMAX = 50 mA. Equation 1-3 shows 20Ω.

1.6.3 CBAT CAPACITOR

Selecting CBAT = 10 x CREG is recommended. However, this leads to a high-value capacitor. Lower values for CBAT capacitor can be used with respect to some rules. In any case, the voltage at the VBB pin should remain above VOFF when the device is turned on.

The current peak at start-up (due to the fast charge of the CREG and CBAT capacitors) may induce a significant drop on the VBB pin. This drop is proportional to the impedance of the VBAT connection (see Figure 1-12).

The VBAT connection is mainly inductive and resistive. Therefore, it can be modeled as a resistor (RTOT) in series with an inductor (L). RTOT and L can be measured.

The following formula gives an indication of the minimum value of CBAT using RTOT and L:

EQUATION 1-5:

$$\frac{C_{BAT}}{C_{REG}} = \sqrt{\frac{100L^2 + R_{TOT}^2}{1 + L^2 + \frac{R_{TOT}^2}{100}}}$$

Where:

L = Inductor (measured in mH)

RTOT = RLINE + RTP (measured in Ω)

Equation 1-5 allows lower CBAT/CREG values than the 10x ratio we recommend.

Assume that we have a good quality VBAT connection with RTOT = 0.1Ω and L = 0.1 mH.

Solving the equation gives CBAT/CREG = 1.

If we increase RTOT up to 1Ω, the result becomes CBAT/CREG = 1.4. However, if the connection is highly resistive or highly inductive (poor connection), the CBAT/CREG ratio greatly increases.

TABLE 1-5: CBAT/CREG RATIO BY VBAT CONNECTION TYPE

Connection Type	RTOT	L	CBAT/CREG Ratio
Good	0.1Ω	0.1 mH	1
Typical	1Ω	0.1 mH	1.4
Highly inductive	0.1Ω	1 mH	7
Highly resistive	10Ω	0.1 mH	7

Figure 1-11 shows the minimum recommended CBAT/CREG ratio as a function of the impedance of the VBAT connection.

FIGURE 1-11: MINIMUM RECOMMENDED CBAT/CREG RATIO

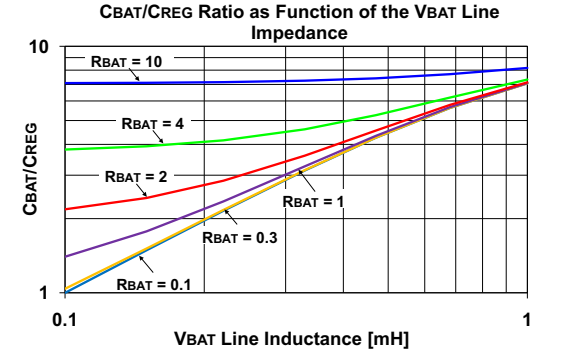
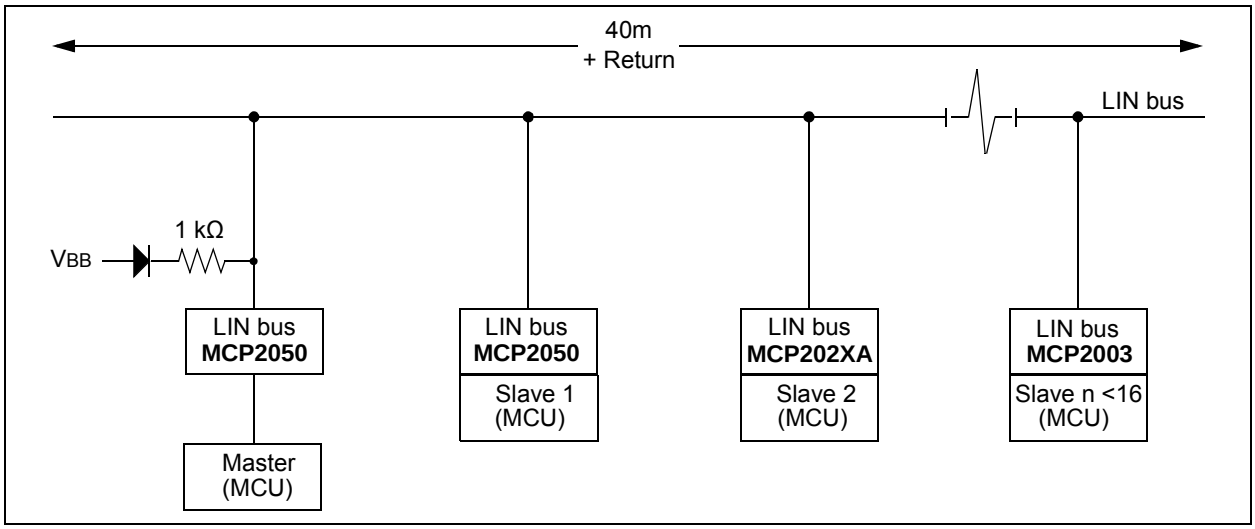


FIGURE 1-13: TYPICAL LIN NETWORK CONFIGURATION



1.8 ICSP™ Considerations

The following should be considered when the MCP2050 is connected to pins supporting in-circuit programming:

- Power used for programming the microcontroller can be supplied from the programmer, or from the MCP2050.
- The voltage on the VREG pin should not exceed the maximum value of VREG as shown in **Section 2.3, DC Specifications**.

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

V_{IN} DC Voltage on R_{XD}, and $\overline{RESET}$ ..... -0.3V to V_{REG} + 0.3
V_{IN} DC Voltage on T_{XD}, CS/LWAKE, $\overline{FAULT}/T_{XE}$ ..... -0.3 to + 40V
V_{BB} Battery Voltage, continuous, non-operating (**Note 1**) ..... -0.3 to + 40V
V_{BB} Battery Voltage, non-operating (LIN bus recessive, no regulator load, t < 60s) (**Note 2**) ..... -0.3 to + 43V
V_{BB} Battery Voltage, transient ISO 7637 Test 1 ..... -100V
V_{BB} Battery Voltage, transient ISO 7637 Test 2a ..... +75V
V_{BB} Battery Voltage, transient ISO 7637 Test 3a ..... -150V
V_{BB} Battery Voltage, transient ISO 7637 Test 3b ..... +100V
V_{LBUS} Bus Voltage, continuous ..... -18 to + 30V
V_{LBUS} Bus Voltage, transient (**Note 3**) ..... -27 to + 43V
I_{LBUS} Bus Short-Circuit Current Limit ..... 200 mA
ESD protection on LIN, V_{BB} (IEC 61000-4-2) (**Note 4**) ..... ±15 KV
ESD protection on LIN, V_{BB} (Human Body Model) (**Note 5**) ..... ±8 KV
ESD protection on all other pins (Human Body Model) (**Note 5**) ..... ±4 KV
ESD protection on all pins (Charge Device Model) (**Note 6**) ..... ±1500V
ESD protection on all pins (Machine Model) (**Note 7**) ..... ±200V
Maximum Junction Temperature ..... 150°C
Storage Temperature ..... -65 to + 150°C

† **NOTICE**: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: LIN 2.x compliant specification.

2: SAE J2602-2 compliant specification.

3: ISO 7637/1 load dump compliant (t < 500 ms).

4: According to IEC 61000-4-2, 330 ohm, 150 pF and Tranceiver EMC Test Specifications [2] to [4]

5: According to AEC-Q100-002/JESD22-A114

6: According to AEC-Q100-011B

7: According to AEC-Q100-003/JESD22-A115

2.2 Nomenclature used in this document

Some terms and names used in this data sheet deviate from those referred to in the LIN specifications. Equivalent values are shown below.

LIN 2.1 Name	Term used in the following tables	Definition
V_{BAT}	*not used*	ECU operating voltage
V_{SUP}	V_{BB}	Supply voltage at device pin
V_{BUS_LIM}	I_{SC}	Current Limit of Driver
V_{BUSREC}	$V_{IH(LBUS)}$	Recessive state
V_{BUSDOM}	$V_{IL(LBUS)}$	Dominant state

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2.3 DC Specifications

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V, T_A = -40°C to +125°C C_{REG} = 10 µF					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power						
V_{BB} Quiescent Operating Current	I_{BBQ}	—	—	200	µA	I_{OUT} = 0 mA, LBUS recessive V_{REG} = 5.0V
		—	—	200	µA	I_{OUT} = 0 mA, LBUS recessive V_{REG} = 3.3V
V_{BB} Quiescent Operating Current with Watchdog Enabled	I_{BBQWDT}	—	—	250	µA	I_{OUT} = 0 mA, LBUS recessive V_{REG} = 5.0V
				250		I_{OUT} = 0 mA, LBUS recessive V_{REG} = 3.3V
V_{BB} READY Current	I_{BBRD}	—	—	100	µA	I_{OUT} = 0 mA, LBUS recessive V_{REG} = 5.0V
		—	—	100	µA	I_{OUT} = 0 mA, LBUS recessive V_{REG} = 3.3V
V_{BB} Ready Current WWDT Enabled	$I_{BBRDWDT}$	—	—	150	µA	With voltage regulator on, transmitter off, receiver on, $\overline{FAULT}/TXE$ = V_{IL}, CS = V_{IH},V_{REG} = 5.0V
				150		With voltage regulator on, transmitter off, receiver on, $\overline{FAULT}/TXE$ = V_{IL}, CS = V_{IH},V_{REG} = 3.3V
V_{BB} Transmitter-Off Current with Watchdog Disabled	I_{BBTO}	—	—	100	µA	With voltage regulator on, transmitter off, receiver on, $\overline{FAULT}/TXE$ = V_{IL}, CS = V_{IH},V_{REG} = 5.0V
		—	—	100	µA	With voltage regulator on, transmitter off, receiver on, $\overline{FAULT}/TXE$ = V_{IL}, CS = V_{IH},V_{REG} = 3.3V
V_{BB} Power-Down Current	I_{BBPD}	—	4.5	8	µA	With voltage regulator powered-off, receiver on and transmitter off, $\overline{FAULT}/TXE$ = V_{IH}, TXD = V_{IH}, CS = V_{IL})
V_{BB} Current with V_{SS} Floating	$I_{BBNOGND}$	-1	—	1	mA	V_{BB} = 12V, GND to V_{BB}, V_{LIN} = 0-18V

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, TX = 0, V_{LBUS} = V_{BB}).

2: Characterized, not 100% tested.

3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled; $V_{WK(LBUS)}$ is used to detect bus activities.

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2.3 DC Specifications (Continued)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V, T_A = -40°C to +125°C C_{REG} = 10 µF					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Microcontroller Interface						
High-Level Input Voltage (T_{XD}, $\overline{FAULT}$/T_{XE}, $\overline{WWDTTRIG}$)	V_{IH}	2.0	—	V_{REG} +0.3	V	
Low-Level Input Voltage (T_{XD}, $\overline{FAULT}$/T_{XE}, $\overline{WWDTTRIG}$)	V_{IL}	-0.3	—	0.8	V	
High-Level Input Current (T_{XD}, $\overline{FAULT}$/T_{XE}, $\overline{WWDTTRIG}$)	I_{IH}	-2.5	—	0.4	µA	Input voltage = 4.0V. ~800 kΩ internal adaptive pull-up
Low-Level Input Current (T_{XD}, $\overline{FAULT}$/T_{XE}, $\overline{WWDTTRIG}$)	I_{IL}	-10	—	—	µA	Input voltage = 0.5V. ~800 kΩ internal adaptive pull-up
High-Level Input Voltage (CS/LWAKE)	V_{IH}	2.0	—	V_{BB}	V	Through a current-limiting resistor
Low-Level Input Voltage (CS/LWAKE)	V_{IL}	-0.3	—	0.8	V	
High-Level Input Current (CS/LWAKE)	I_{IH}	—	—	8.0	µA	Input voltage = 0.8V_{REG} ~1.3 MΩ internal pull-down to V_{SS}
Low-Level Input Current (CS/LWAKE)	I_{IL}	—	—	5.0	µA	Input voltage = 0.2V_{REG} ~1.3 MΩ internal pull-down to V_{SS}
Low-Level Output Voltage (R_{XD})	V_{OLRXD}	—	—	0.2V_{REG}	V	I_{OL} = 2 mA
High-Level Output Voltage (R_{XD})	V_{OHRXD}	0.8V_{REG}	—	—	V	I_{OH} = 2 mA
Low-Level Output Voltage ($\overline{FAULT}$/T_{XE})	V_{OLOD}	—		1.0	V	I_{OL} = 4 mA
Low-Level Output Voltage ($\overline{RESET}$)	V_{OLRST}	—	—	1.0	V	I_{OL} = 4 mA

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, T_X = 0, V_{LBUS} = V_{BB}).

2: Characterized, not 100% tested.

3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled; $V_{WK(LBUS)}$ is used to detect bus activities.

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2.3 DC Specifications (Continued)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V, T_A = -40°C to +125°C C_{REG} = 10 µF					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Bus Interface						
High-Level Input Voltage	$V_{IH(LBUS)}$	0.6 V_{BB}	—	—	V	Recessive state
Low-Level Input Voltage	$V_{IL(LBUS)}$	-8	—	0.4 V_{BB}	V	Dominant state
Input Hysteresis	V_{HYS}	—	—	0.175 V_{BB}	V	$V_{IH(LBUS)} – V_{IL(LBUS)}$
Low-Level Output Current	$I_{OL(LBUS)}$	40	—	200	mA	Output voltage = 0.1 V_{BB}, V_{BB} = 12V
Pull-Up Current on Input	$I_{PU(LBUS)}$	-180	—	-72	µA	~30 kΩ internal pull-up @ $V_{IH (LBUS)}$ = 0.7 V_{BB}, V_{BB}=12V
Short-Circuit Current Limit	I_{SC}	50	—	200	mA	**(Note 1)**
High-Level Output Voltage	$V_{OH(LBUS)}$	0.8 V_{BB}	—	V_{BB}	V	
Driver Dominant Voltage	$V_{_LOSUP}$	—	—	1.1	V	V_{BB} = 7.3V, R_{LOAD} = 1000Ω
Driver Dominant Voltage	$V_{_HISUP}$	—	—	1.2	V	V_{BB} = 18V, R_{LOAD} = 1000Ω
Input Leakage Current (at the receiver during dominant bus level)	$I_{BUS_PAS_DOM}$	-1	—	—	mA	Driver off, V_{BUS} = 0V, V_{BB} = 12V
Input Leakage Current (at the receiver during recessive bus level)	$I_{BUS_PAS_REC}$	-20	—	20	µA	Driver off, 8V < V_{BB} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{BB}$
Leakage Current (disconnected from ground)	$I_{BUS_NO_GND}$	-10	—	+10	µA	GND_{DEVICE} = V_{BB}, 0V < V_{BUS} < 18V, V_{BB} = 12V
Leakage Current (disconnected from V_{BB})	$I_{BUS_NO_PWR}$	-10	—	+10	µA	V_{BB} = GND, 0 < V_{BUS} < 18V
Receiver Center Voltage	V_{BUS_CNT}	0.475 V_{BB}	0.5 V_{BB}	0.525 V_{BB}	V	V_{BUS_CNT} = ($V_{IL (LBUS)}$ + $V_{IH (LBUS)}$)/2
Slave Termination	R_{SLAVE}	20	30	47	kΩ	(**Note 2**)
Capacitance of slave node	C_{SLAVE}			50	pF	(**Note 2**)
Wake-Up Voltage Threshold on LIN Bus	$V_{WK(LBUS)}$	—	—	3.4	V	Wake up from Power-Down mode (**Note 3**)

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, T_X = 0, V_{LBUS} = V_{BB}).

2: Characterized, not 100% tested.

3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled; $V_{WK(LBUS)}$ is used to detect bus activities.

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2.3 DC Specifications (Continued)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V, T_A = -40°C to +125°C C_{REG} = 10 µF					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Voltage Regulator – 5.0V						
Output Voltage Range	V_{REG}	4.85	5.00	5.15	V	0 mA < I_{OUT} < 70 mA
Line Regulation	$\Delta V_{OUT}1$	—	10	50	mV	I_{OUT} = 1 mA, 6.0V < V_{BB} < 18V
Load Regulation	$\Delta V_{OUT}2$	—	10	50	mV	5 mA < I_{OUT} <70 mA 6.0V < V_{BB} < 12V
Power Supply Ripple Reject	PSRR	—	—	50	dB	1 V_{PP} @10-20 kHz I_{LOAD} = 20 mA
Output Noise Voltage	eN	—	—	100	µV_{RMS}	10 Hz – 40 MHz C_{FILTER} = 10 µf, C_{BP} = 0.1 µf, I_{LOAD} = 20 mA
Shutdown Voltage Threshold	V_{SD}	3.5	—	4.0	V	See **Figure 1-10** (**Note 2**)
Input Voltage to Turn Off Output	V_{OFF}	3.9	—	4.5	V	
Input Voltage to Turn On Output	V_{ON}	5.25	—	6.0	V	
Voltage Regulator – 3.3V						
Output Voltage	V_{REG}	3.20	3.30	3.40	V	0 mA < I_{OUT} < 70 mA
Line Regulation	$\Delta V_{OUT}1$	—	10	50	mV	I_{OUT} = 1 mA, 6.0V < V_{BB} < 18V
Load Regulation	$\Delta V_{OUT}2$	—	10	50	mV	5 mA < I_{OUT} < 70 mA, 6.0V < V_{BB} < 12V
Power Supply Ripple Reject	PSRR	—	—	50	dB	1 V_{PP} @10-20 kHz, I_{LOAD} = 20 mA
Output Noise Voltage	eN	—	—	100	µV_{RMS} /$\sqrt{Hz}$	10 Hz – 40 MHz C_{FILTER} = 10 µf, C_{BP} = 0.1 µf, I_{LOAD} = 20 mA
Shutdown Voltage	V_{SD}	2.5	—	2.7	V	See **Figure 1-10** (**Note 2**)

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, T_X = 0, V_{LBUS} = V_{BB}).

2: Characterized, not 100% tested.

3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled; $V_{WK(LBUS)}$ is used to detect bus activities.

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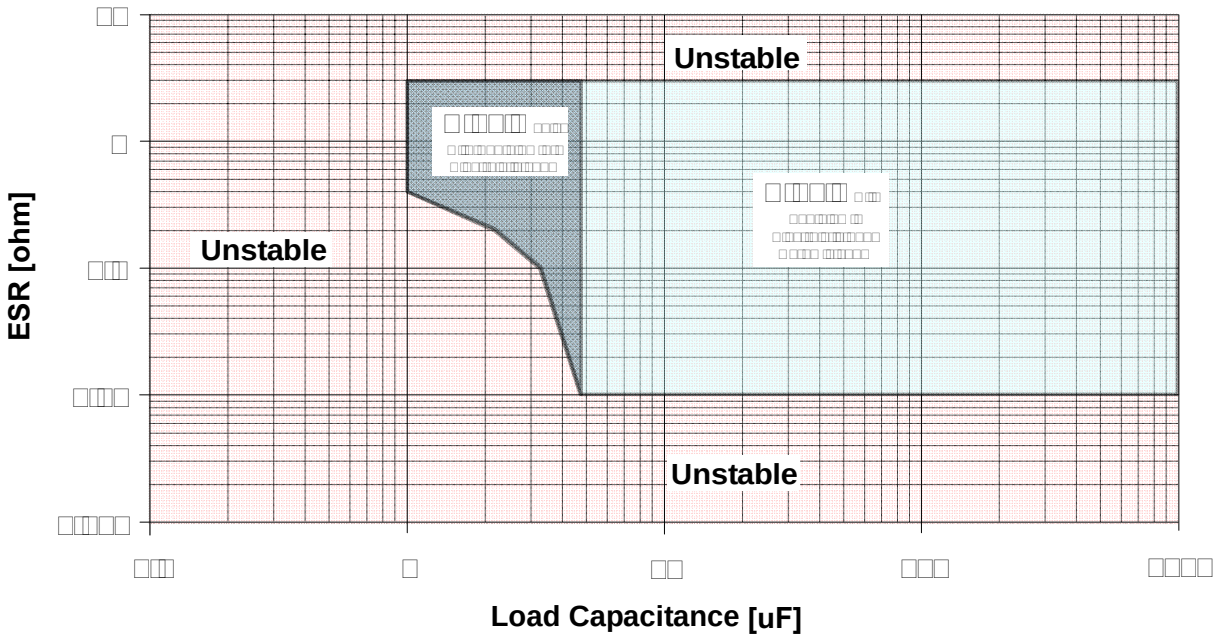
FIGURE 2-1: ESR CURVES FOR LOAD CAPACITOR SELECTION



Note 1: The graph shows the minimum capacitance after de-rating due to tolerance, temperature and voltage

2.4 AC Specifications

AC CHARACTERISTICS	**Electrical Characteristics**: Unless otherwise indicated, all limits are specified for V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Bus Interface - Constant Slope Time Parameters (DC specifications are for a V_{BB} range of 6.0 to 18.0V)						
Slope Rising and Falling Edges	t_{SLOPE}	3.5	—	22.5	µs	7.3V <= V_{BB} <= 18V
Propagation Delay of Transmitter	$t_{TRANSPD}$	—	—	5.0	µs	$t_{TRANSPD}$ = max ($t_{TRANSPDR}$ or $t_{TRANSPDF}$)
Propagation Delay of Receiver	t_{RECPD}	—	—	6.0	µs	t_{RECPD} = max (t_{RECPDR} or t_{RECPDF})
Symmetry of Propagation Delay of Receiver Rising Edge w.r.t. Falling Edge	t_{RECSYM}	-2.0	—	2.0	µs	trecsym = max (t_{RECPDF} – t_{RECPDR}) R_{RXD} 2.4 kΩ to V_{CC}, C_{RXD} 20pF
Symmetry of Propagation Delay of Transmitter Rising Edge w.r.t. Falling Edge	$t_{TRANSSYM}$	-2.0	—	2.0	µs	$t_{TRANSSYM}$ = max ($t_{TRANSPDF}$ - $t_{TRANSPDR}$)
Bus Dominant Time-Out Time	$t_{TO(LIN)}$	—	25	—	mS	
Time to Sample of $\overline{FAULT}$/T_{XE} for Bus Conflict Reporting	t_{FAULT}	—	—	32.5	µs	t_{FAULT} = max ($t_{TRANSPD}$ + t_{SLOPE} + t_{RECPD})
Duty Cycle 1 @ 20.0 kbit/sec		0.396	—	—	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.744 x V_{BB}, $TH_{DOM(MAX)}$ = 0.581 x V_{BB}, V_{BB} =7.0V - 18V; t_{BIT} = 50 µs. D1 = $t_{BUS_REC(MIN)}$ / 2 x t_{BIT})
Duty Cycle 2 @ 20.0 kbit/sec		—	—	0.581	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.284 x V_{BB}, $TH_{DOM(MAX)}$ = 0.422 x V_{BB}, V_{BB} =7.6V - 18V; t_{BIT} = 50 µs. D2 = $t_{BUS_REC(MAX)}$ / 2 x t_{BIT})
Duty Cycle 3 @ 10.4 kbit/sec		0.417	—	—	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.778 x V_{BB}, $TH_{DOM(MAX)}$ = 0.616 x V_{BB}, V_{BB} =7.0V - 18V; t_{BIT} = 96 µs. D3 = $t_{BUS_REC(MIN)}$ / 2 x t_{BIT})
Duty Cycle 4 @ 10.4 kbit/sec		—	—	0.590	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.251 x V_{BB}, $TH_{DOM(MAX)}$ = 0.389 x V_{BB}, V_{BB} =7.6V - 18V; t_{BIT} = 96 µs. D4 = $t_{BUS_REC(MAX)}$ / 2 x t_{BIT})

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2.4 AC Specifications (Continued)

AC CHARACTERISTICS	**Electrical Characteristics**: Unless otherwise indicated, all limits are specified for V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Voltage Regulator						
Bus Activity Debounce time	t_{BDB}	30	80	250	µs	
Bus Activity to Voltage Regulator Enabled	$t_{BACTIVE}$	35	—	200	µs	
Voltage Regulator Enabled to Ready	t_{VEVR}	300	—	1200	µs	**(Note 1)**
Chip Select to Ready Mode	tCSR	—	—	230	µs	
Chip Select to Power-Down	tCSPD	—	—	300	µs	**(Note 2)**
Short-Circuit to Shutdown	tSHUTDOWN	20	—	100	µs	
$\overline{\text{RESET}}$ Timing						
V_{REG} OK detect to $\overline{\text{RESET}}$ inactive	tRPU	—	—	60.0	µs	
V_{REG} not OK detect to $\overline{\text{RESET}}$ active	tRPD	—	—	60.0	µs	
WWDT						
Reset Pulse Length	tWDRST	—	150	—	µs	-40/+100%
Power-Up Watchdog Window Length	tPOWERUP	—	27.2	—	ms	±15% RWWDTSELECT = 33 kΩ **(Note 2, Note 3)**
Watchdog Window Length	tWLENGTH	5.95	7	8.05	ms	±15% RWWDTSELECT = 33 kΩ **(Note 4, Note 5)**
		102	120	138	ms	±15% RWWDTSELECT = 680 kΩ **(Note 4, Note 5)**

Note 1: Time depends on external capacitance and load. Test condition: C_{REG} = 4.7uF, no resistor load.

2: Characterized, not 100% tested.

3: $t_{POWERUP}$ = 0.8 ms × (RWWDTSELECT+1); R in kΩ.

4: $t_{WLENGTH}$ = (0.175 ms × RWWDTSELECT) + 1.2 ±15%; R in kΩ.

5: Characterized; tested for RWWDTSELECT = 33 kΩ and 680 kΩ

2.5 Thermal Specifications

Parameter	Symbol	Typ	Max	Units	Test Conditions
Recovery Temperature	θRECOVERY	+140	—	°C	
Shutdown Temperature	θSHUTDOWN	+150	—	°C	
Short Circuit Recovery Time	tTHERM	1.5	5.0	ms	
Thermal Package Resistances					
Thermal Resistance, 14L-PDIP	θJA	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θJA	90.8	—	°C/W	
Thermal Resistance, 20L-QFN	θJA	44.6	—	°C/W	

Note 1: The maximum power dissipation is a function of T_{JMAX}, ΘJA and ambient temperature T_A. The maximum allowable power dissipation at an ambient temperature is $P_D = (T_{JMAX} - T_A)\ \Theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the MCP2050 will go into thermal shutdown.

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2.6 Typical Performance Curves

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C

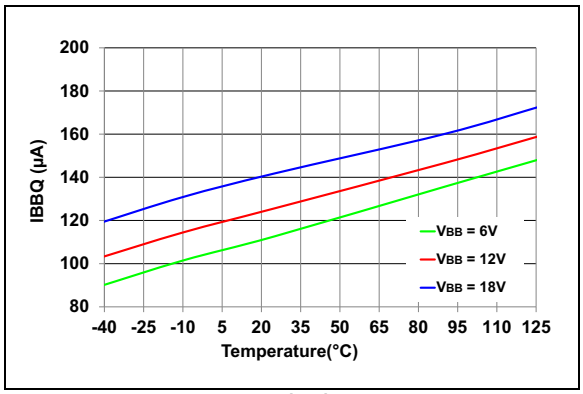

FIGURE 2-2: *Typical I_{BBQ} vs. Temperature – 5.0V.*

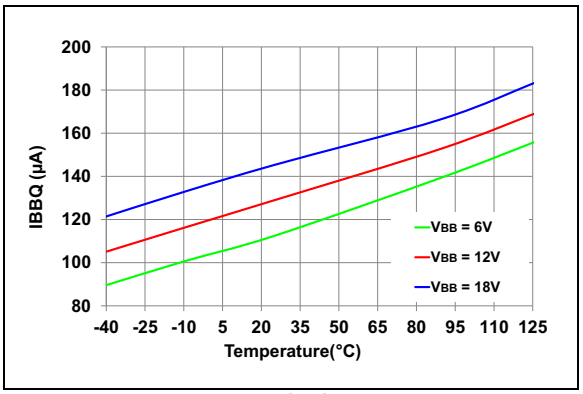

FIGURE 2-5: *Typical I_{BBQ} vs. Temperature – 3.3V.*

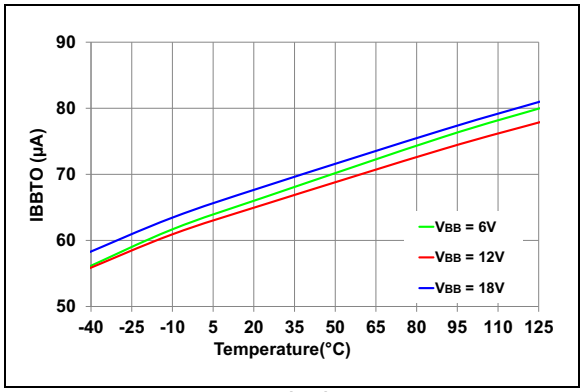

FIGURE 2-3: *Typical I_{BBTO} vs. Temperature – 5.0V.*

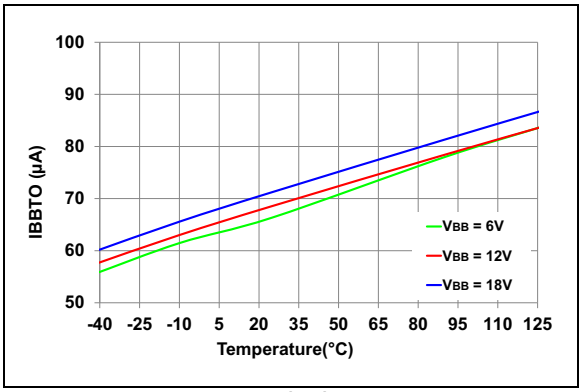

FIGURE 2-6: *Typical I_{BBTO} vs. Temperature – 3.3V.*

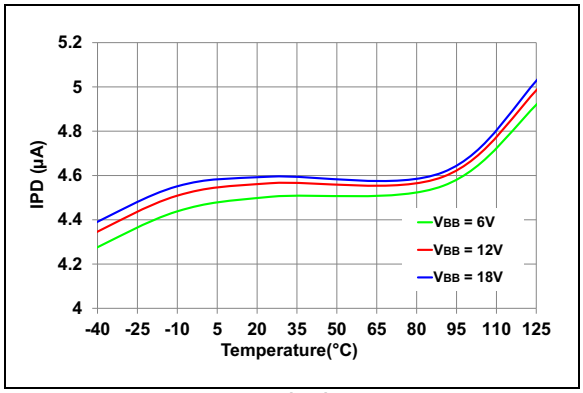

FIGURE 2-4: *Typical I_{PD} vs. Temperature – 5.0V.*

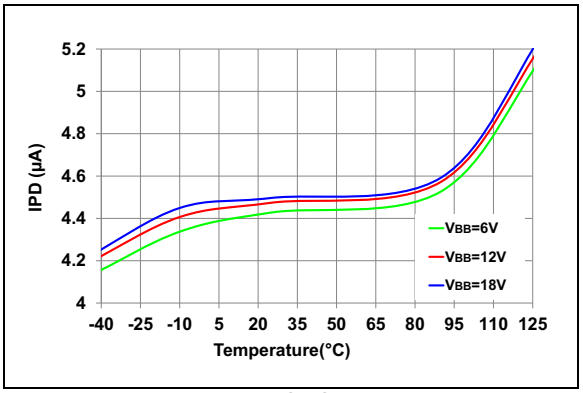

FIGURE 2-7: *Typical I_{PD} vs. Temperature – 3.3V.*

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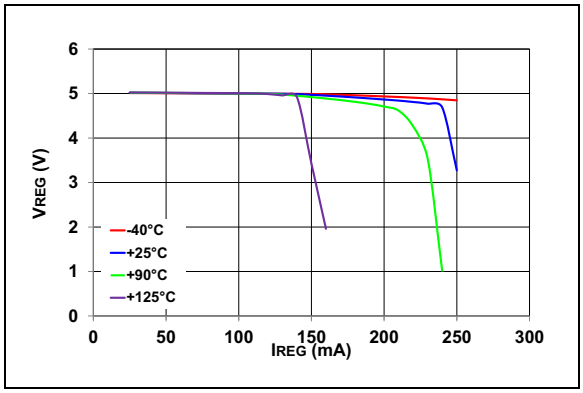

FIGURE 2-8: *5.0 VREG vs. IREG at VBB = 12V.*

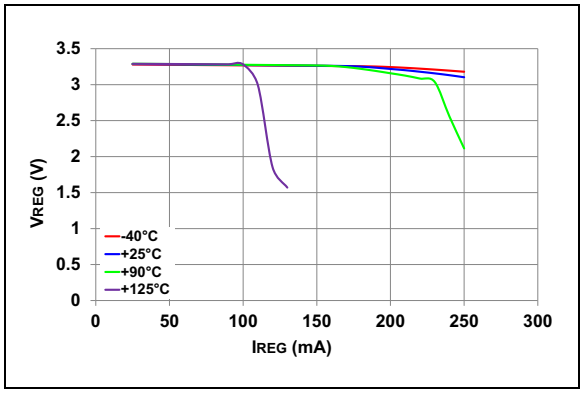

FIGURE 2-9: *3.3V VREG vs. IREG at VBB = 12V.*

2.7 Timing Diagrams and Specifications

FIGURE 2-10: BUS TIMING DIAGRAM

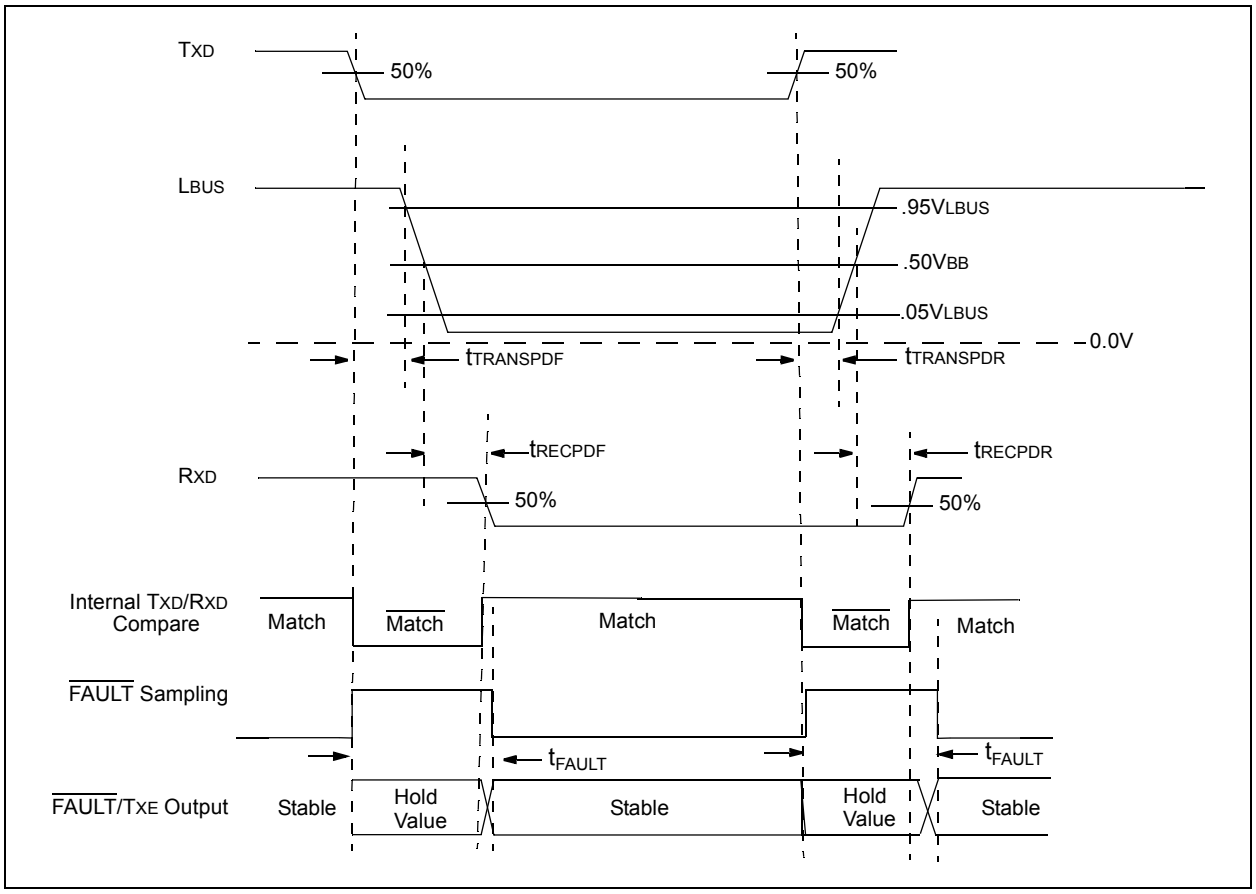

FIGURE 2-11: REGULATOR BUS WAKE TIMING DIAGRAM

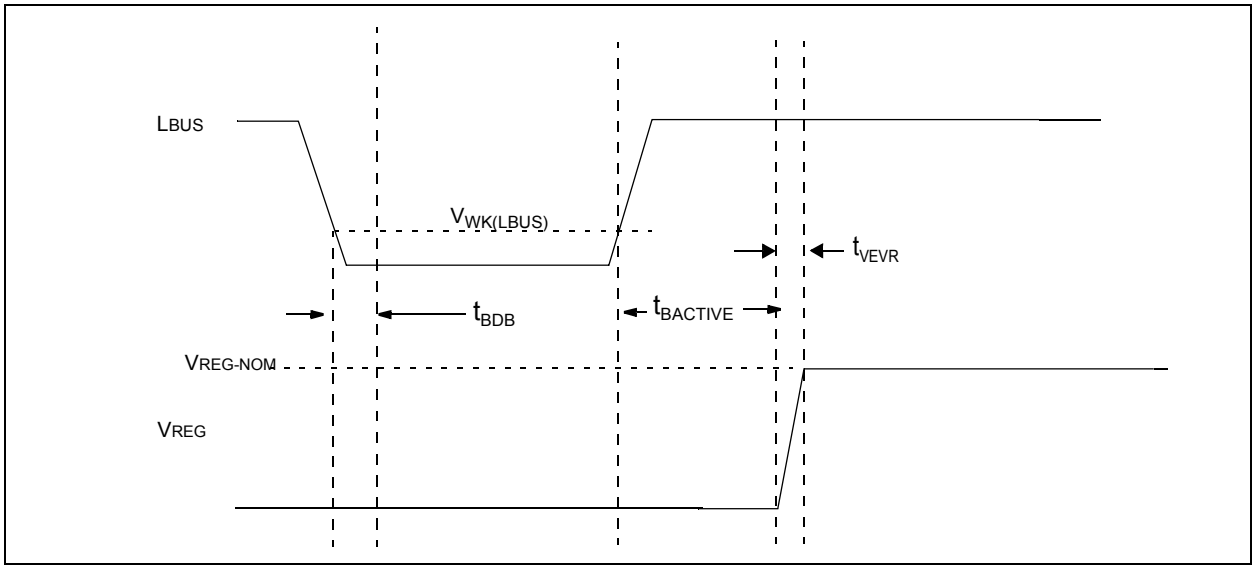

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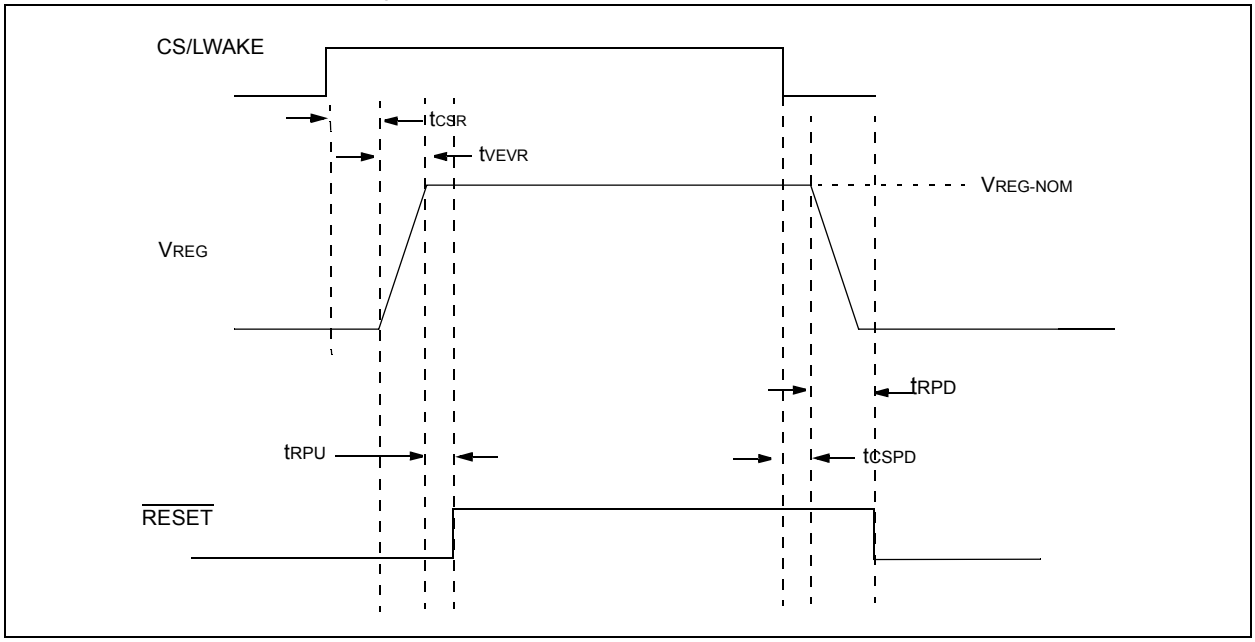
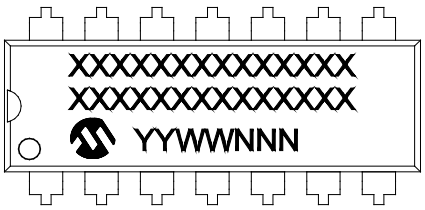
FIGURE 2-12: CS/LWAKE, REGULATOR AND $\overline{\text{RESET}}$ TIMING DIAGRAM



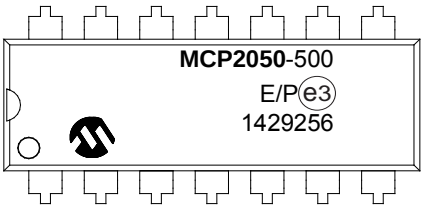
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

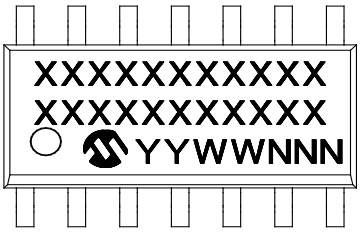
14-Lead PDIP (300 mil)



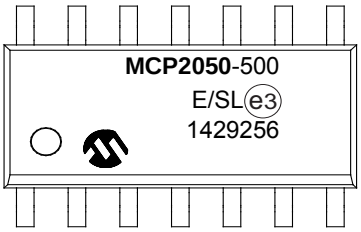
Example



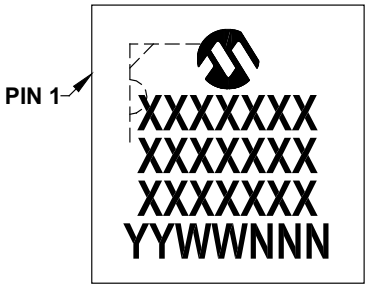
14-Lead SOIC (.150")



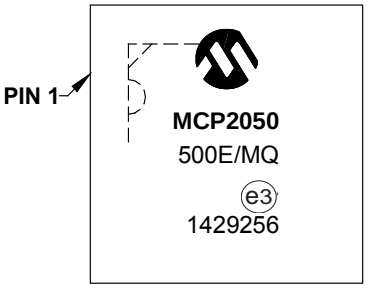
Example



20-Lead QFN (5x5x0.9 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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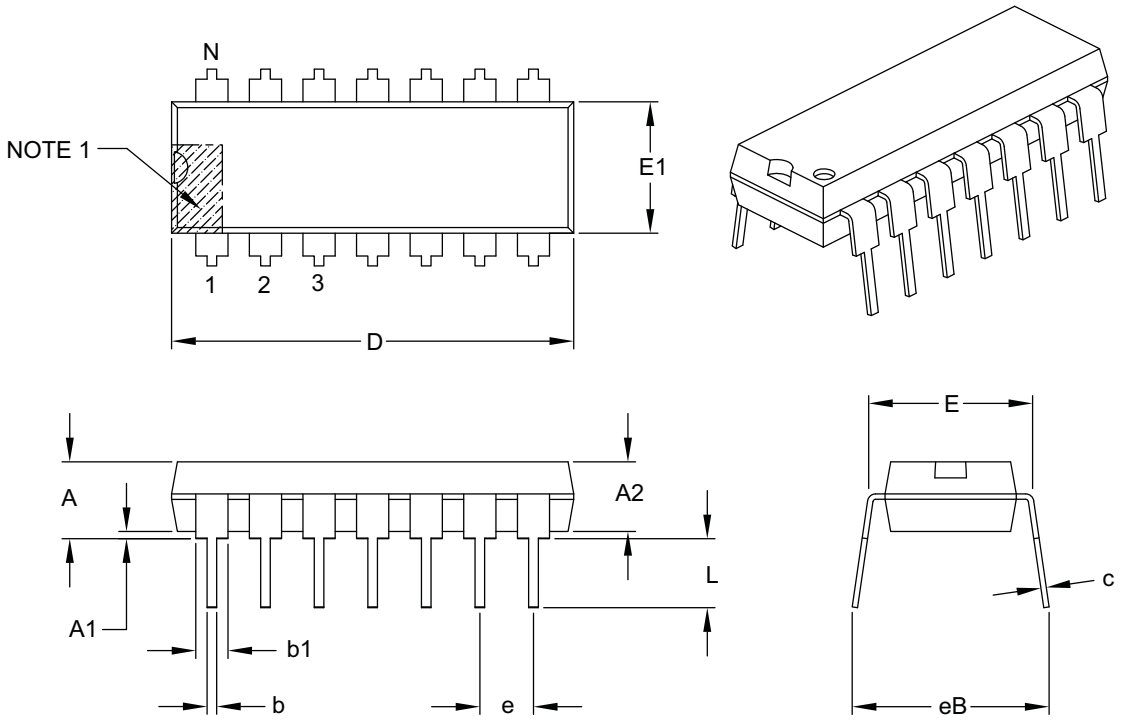
14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

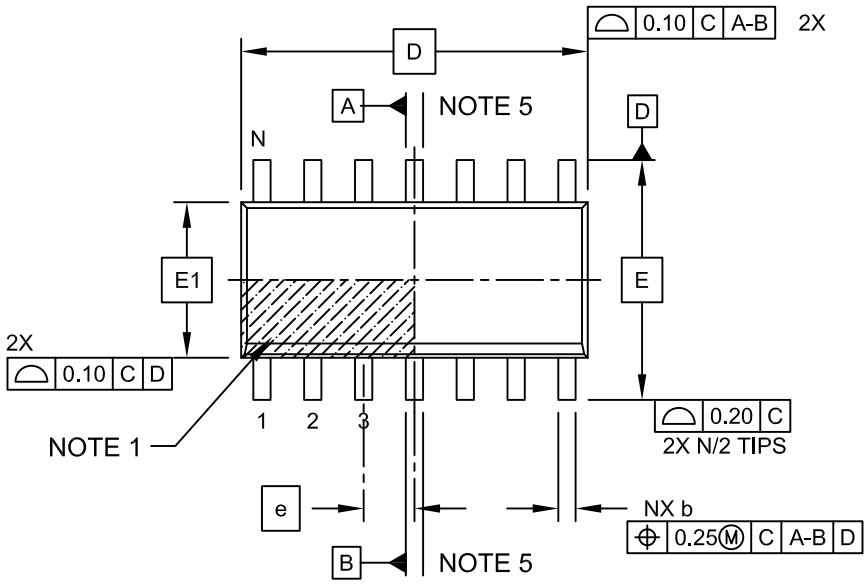
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

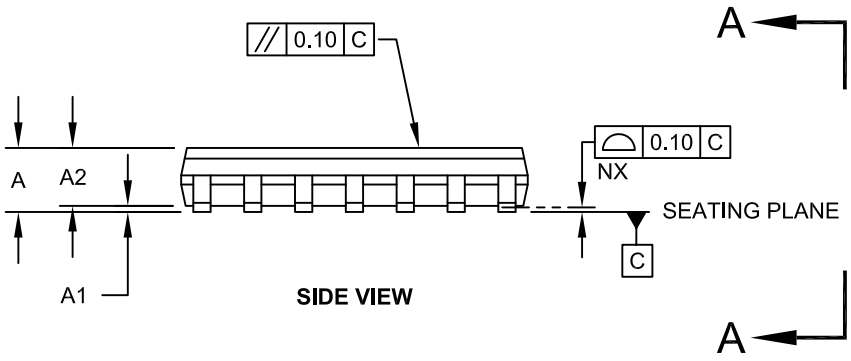
Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

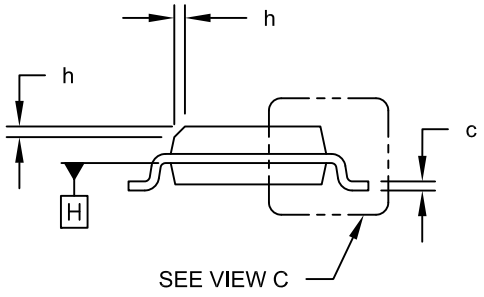
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing No. C04-065C Sheet 1 of 2

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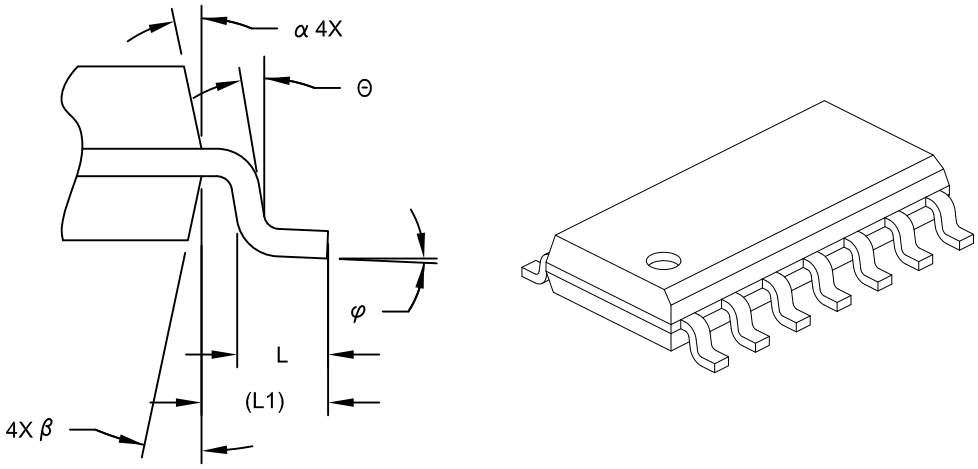
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

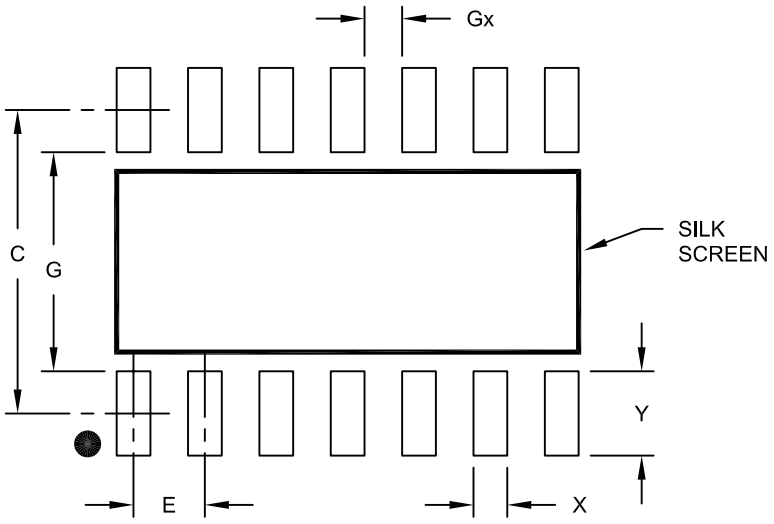
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

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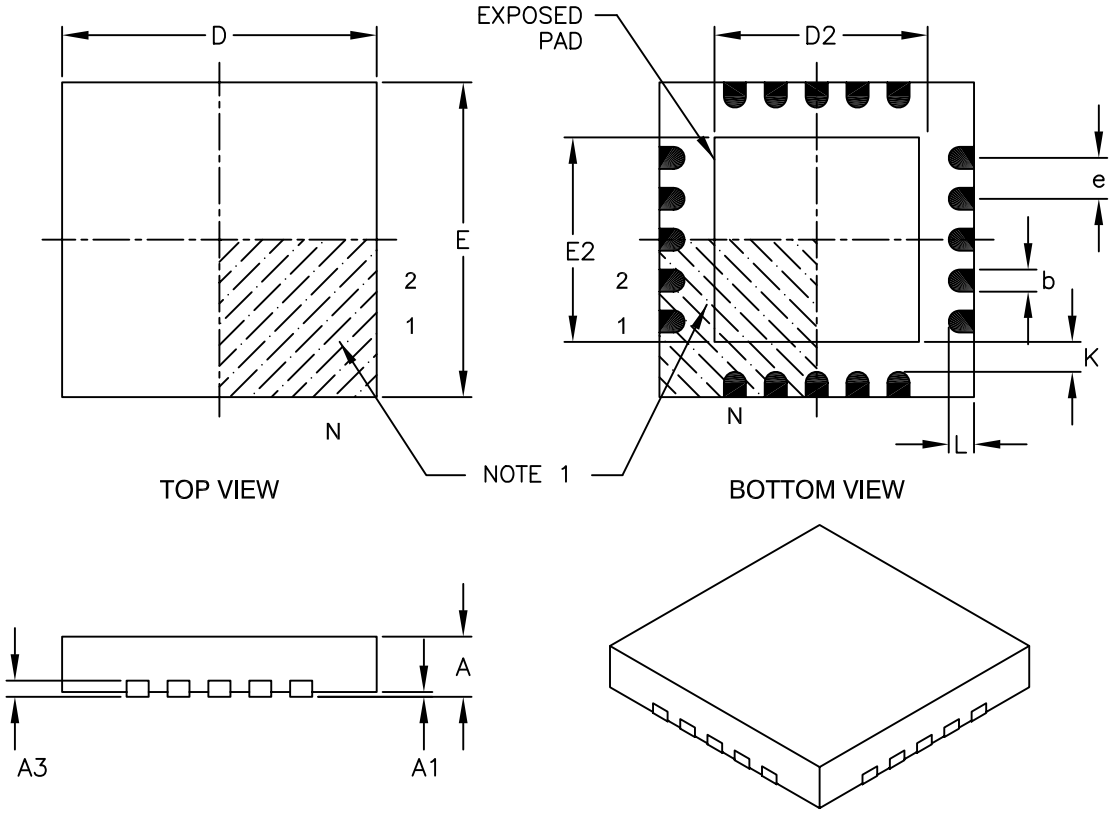
20-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.15	3.25	3.35
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.15	3.25	3.35
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.35	0.40	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

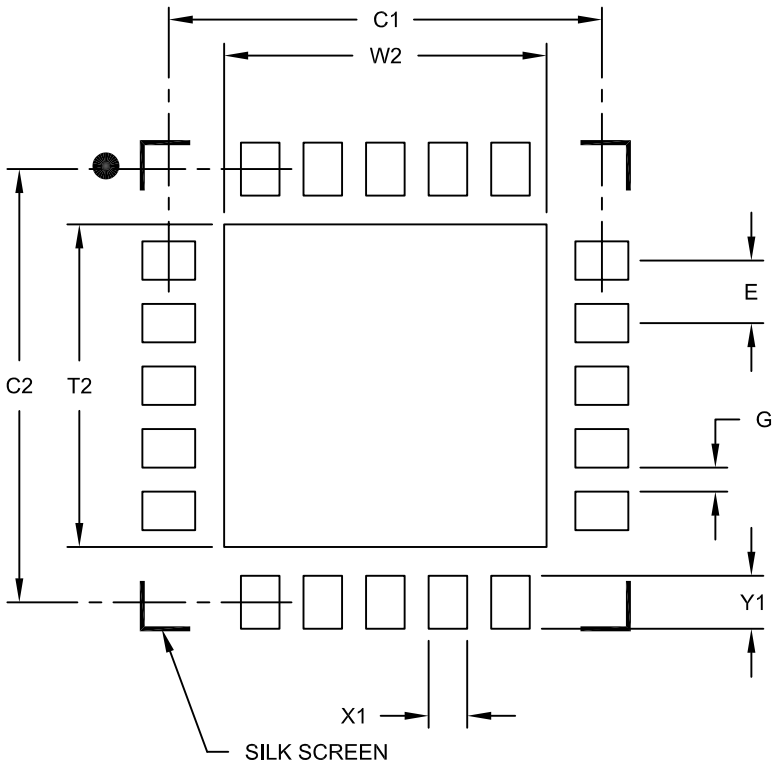
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-139B

20-Lead Plastic Quad Flat, No Lead Package (MQ) - 5x5 mm Body [QFN]
With 0.40mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			3.35
Optional Center Pad Length	T2			3.35
Contact Pad Spacing	C1		4.50	
Contact Pad Spacing	C2		4.50	
Contact Pad Width (X20)	X1			0.40
Contact Pad Length (X20)	Y1			0.55
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2139A

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	–X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	MCP2050:	LIN Transceiver with Voltage Regulator
	MCP2050T:	LIN Transceiver with Voltage Regulator (Tape and Reel) (SOIC and QFN)
Tape and Reel Option:	Blank =	Standard packaging (tube or tray)
	T =	Tape and Reel(1)
Temperature Range:	E =	-40°C to +125°C
Package:	MQ =	20-Lead Plastic Quad Flat, No Lead Package – 5x5x0.9 mm Body (QFN)
	P =	14-Lead Plastic Dual In-Line – 300 mil Body (PDIP)
	SL =	14-Lead Plastic Small Outline – Narrow, 3.90 mm Body (SOIC)

Examples:

a)	MCP2050-330E/P:	3.3V, Extended Temperature, 14-LD PDIP Package
b)	MCP2050-330E/MQ:	3.3V, Extended Temperature, 20-LD QFN Package
c)	MCP2050T-330E/MQ:	Tape and Reel, 3.3V, Extended Temperature, 20-LD QFN Package
d)	MCP2050-330E/SL:	3.3V, Extended Temperature, 14-LD SOIC Package
e)	MCP2050T-330E/SL:	Tape and Reel, 3.3V, Extended Temperature, 14-LD SOIC Package
f)	MCP2050-500E/P:	5.0V, Extended Temperature, 14-LD PDIP Package
g)	MCP2050-500E/MQ:	5.0V, Extended Temperature, 20-LD QFN Package
h)	MCP2050T-500E/MQ:	Tape and Reel, 5.0V, Extended Temperature, 20-LD QFN Package
i)	MCP2050-500E/SL:	5.0V, Extended Temperature, 14-LD SOIC Package
j)	MCP2050T-500E/SL:	Tape and Reel, 5.0V, Extended Temperature, 14-LD SOIC package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

APPENDIX A: REVISION HISTORY

Revision D (September 2014)

The following is the list of modifications:

1. Added Exposed Thermal Pad pin on QFN and in **Section 1.3, Pin Descriptions**.
2. Updated **Figure 1-7**.
3. Added note in **Figure 2-1**.
4. Added AC parameter for WWDT in **Section 2.4, AC Specifications**.
5. Created new **Section 2.6, Typical Performance Curves**.
6. Fixed minor typographical errors.

Revision C (August 2012)

The following is the list of modifications:

1. Removed two notes in **Section 2.4 "AC Specifications"**.

Revision B (April 2012)

The following is the list of modifications:

1. Corrected a label in Figure 1-12.
2. Corrected a label in Figure 1-13.
3. Updated the Product Identification System page.

Revision A (March 2012)

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