Power-Off Protection ±5 V, +12 V, Quad SPST Switches with 5 Ω On Resistance

ADG4612/ADG4613

FEATURES

Power-off protection
- **Switch guaranteed off with no power supplies present**
- **Inputs are high impedance with no power**

Switch turns off when input > V_{DD} + V_T
Overvoltage protection up to 16 V
PSS robust
Negative signal capability passes signals down to −5.5 V
6.1 Ω maximum on resistance
1.4 Ω on-resistance flatness
±3 V to ±5.5 V dual supply
3 V to 12 V single supply
3 V logic compatible inputs
Rail-to-rail operation
16-lead TSSOP and 16-lead 3 mm × 3 mm LFCSP

APPLICATIONS

Hot swap applications
Data acquisition systems
Battery-powered systems
Automatic test equipment
Communication systems
Relay replacement

GENERAL DESCRIPTION

The ADG4612/ADG4613 contain four independent single-pole/single-throw (SPST) switches. The ADG4612 switches are turned on with Logic 1 on the appropriate control input. The ADG4613 has two switches with digital control logic similar to that of the ADG4612; the logic is inverted on the other two switches. Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. The ADG4613 exhibits break-before-make switching action for use in multiplexer applications.

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance inputs, ensuring that no current flows, which can damage the switch or downstream circuitry. This is very useful in applications where analog signals may be present at the switch inputs before power is applied or where the user has no control over the power supply sequence.

In the off condition, signal levels up to 16 V are blocked. Also, when the analog input signal levels exceed V_{DD} by V_T, the switch turns off.

FUNCTIONAL BLOCK DIAGRAM

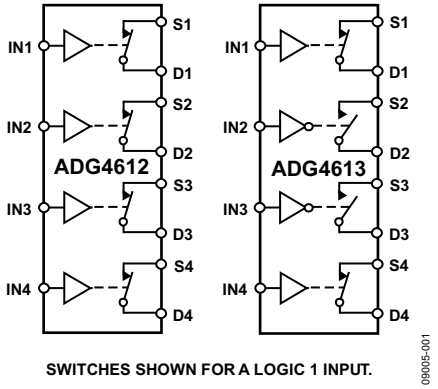

Figure 1.

The low on resistance of these switches make them ideal solutions for data acquisition and gain switching applications where low on resistance and distortion is critical. The on-resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals.

PRODUCT HIGHLIGHTS

1. Power-Off Protection On Both S and D Pins.
2. PSS Robustness.
3. Overvoltage Protection up to 16 V.
4. 5.2 Ω On Resistance.
5. 16-Lead TSSOP and 3 mm × 3 mm LFCSP Packages.

Rev. 0

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REVISION HISTORY

10/10—Revision 0: Initial Version

SPECIFICATIONS

5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range (Normal Mode)		−5.5 V to V_{DD}	V	V_{DD} to V_{SS} = 16 V maximum
On Resistance (R_{ON})	5.2		Ω typ	V_S = ±4.5 V, I_S = −10 mA; see Figure 22
	6.1	7.6	Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On-Resistance Match Between Channels (ΔR_{ON})	0.05		Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.15	0.18	Ω max	
On-Resistance Flatness ($R_{FLAT (ON)}$)	1.4		Ω typ	V_S = ±4.5 V, I_S = −10 mA
	1.75	2.2	Ω max	
LEAKAGE CURRENTS (NORMAL MODE)				V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±5		nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 23
	±10	±300	nA max	
Drain Off Leakage, I_D (Off)	±5		nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 23
	±10	±300	nA max	
Channel On Leakage, I_D (On), I_S (On)	±10		nA typ	V_S = V_D = ±4.5 V; see Figure 24
	±16	±700	nA max	
LEAKAGE CURRENTS (ISOLATION MODE)				
Source Off Leakage, I_S (Off)	±0.03		µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V
	±0.1	±2.5	µA max	V_S = −5.5 V, V_D = +10.5 V; or V_S = +10.5 V, V_D = −5.5 V; see Figure 23
	±8		µA typ	V_{DD} = +5.5 V, V_{SS} = −5.5 V or 0 V
	±22	±30	µAmax	V_S = −5.5 V, V_D = +10.5 V; or V_S = +10.5 V, V_D = −5.5 V; see Figure 23
Drain Off Leakage, I_D (Off)	±0.03		µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V
	±0.1	±2.5	µA max	V_S = −5.5 V, V_D = +10.5 V; or V_S = +10.5 V, V_D = −5.5 V; see Figure 23
	±8		µA typ	V_{DD} = +5.5 V, V_{SS} = −5.5 V or 0 V
	±22	±30	µA max	V_S = −5.5 V, V_D = +10.5 V; or V_S = +10.5 V, V_D = −5.5 V; see Figure 23
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL}	±0.015		µA typ	V_{IN} = V_{GND}
	±0.1	±0.15	µA max	
Input Current, I_{INH}	±13		µA typ	V_{IN} = V_{DD}
	±16	±18	µA max	
Logic Pull-Down Resistance, R_{PD}	400		kΩ typ	
Digital Input Capacitance, C_{IN}	4		pF typ	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	73		ns typ	R_L = 300 Ω, C_L = 35 pF
	125	149	ns max	V_S = 3 V; see Figure 25
t_{OFF}	100		ns typ	R_L = 300 Ω, C_L = 35 pF
	125	149	ns max	V_S = 3 V; see Figure 25

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
Break-Before-Make Time Delay, t_D	20		ns typ	R_L = 50 Ω, C_L = 35 pF
(ADG4613 Only)		3	ns min	V_{S1} = V_{S2} = 3 V; see Figure 26
Fault Response Time	295		ns typ	V_S = 2 V to 8 V, R_L = 300 Ω, C_L = 35 pF
Fault Recovery Time	1.2		µs typ	V_S = 2 V to 8 V, R_L = 300 Ω, C_L = 35 pF
Threshold Voltage, V_T	1.8		V typ	
Charge Injection	225		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 27
Off Isolation	−54		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Channel-to-Channel Crosstalk	−71		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Total Harmonic Distortion + Noise, THD + N	0.13		% typ	R_L = 110 Ω, 6 V p-p, f = 20 Hz to 20 kHz; see Figure 31
Insertion Loss	−0.5		dB typ	R_L = 50 Ω, C_L = 5 pF; f = 1 MHz; see Figure 30
−3 dB Bandwidth	293		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 30
C_S (Off)	13		pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	13		pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	50		pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS				
Normal Mode				Digital inputs = 0 V or V_{DD}
I_{DD}	90		µA typ	V_{DD} = +5.5 V, V_{SS} = −5.5 V
	140	165	µA max	
I_{SS}	27		µA typ	V_{DD} = +5.5 V, V_{SS} = −5.5 V
	50	58	µA max	
Isolation Mode				V_{DD} = +5.5 V, V_{SS} = −5.5 V or floating
I_{DD}	90		µA typ	Digital inputs = 0 V or 5.5 V
	140	165	µA max	V_S = −5.5 V or +10.5 V
				V_{DD} = 0 V or floating, V_{SS} = −5.5 V
I_{SS}	0.1		µA typ	Digital inputs = 0 V or 5.5 V
	0.2	6	µA max	V_S = −5.5 V or +10.5 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		−5.5 V to V_{DD}	V	V_{DD} to V_{SS} = 16 V maximum
On-Resistance (R_{ON})	4.5		Ω typ	V_S = 0 V to +10 V, I_S = −10 mA; see Figure 22
	5.1	6.4	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels (ΔR_{ON})	0.05		Ω typ	V_S = 0 V to +10 V, I_S = −10 mA
	0.15	0.18	Ω max	
On-Resistance Flatness ($R_{FLAT (ON)}$)	1		Ω typ	V_S = 0 V to +10 V, I_S = −10 mA
	1.25	1.6	Ω max	
LEAKAGE CURRENTS				
Normal Mode				V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±3		nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 23
	±10	±200	nA max	
Drain Off Leakage, I_D (Off)	±3		nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 23
	±10	±200	nA max	
Channel On Leakage, I_D (On), I_S (On)	±7		nA typ	V_S = V_D = 1 V or 10 V; Figure 24
	±11	±300	nA max	
Isolation Mode				
Source Off Leakage, I_S (Off)	±0.05		µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V
	±0.3	±3	µA max	V_S = 1 V/16 V, V_D = 16 V/1 V; see Figure 23
	±10		µA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, V_S = 16 V/1 V, V_D = 1 V/16 V; see Figure 23
	±28	±38	µA max	
Drain Off Leakage, I_D (Off)	±0.05		µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V V_S = 1 V/16 V, V_D = 16 V/1 V; see Figure 23
	±0.3	±3	µA max	
	±10		µA typ	V_{DD} = 13.2 V, V_{SS} = 0 V V_S = 16 V/1 V, V_D = 1 V/16 V; see Figure 23
	±28	±38	µA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL}	±0.015		µA typ	V_{IN} = V_{GND}
	±0.1	±0.15	µA max	
Input Current, I_{INH}	±13		µA typ	V_{IN} = 5 V
	±16	±18	µA max	
Input Current, I_{INH}	±34		µA typ	V_{IN} = V_{DD}
	±40	±42	µA max	
Logic Pull-Down Resistance, R_{PD}	400		kΩ typ	
Digital Input Capacitance, C_{IN}	4		pF typ	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	46		ns typ	R_L = 300 Ω, C_L = 35 pF
	73	90	ns max	V_S = 8 V; see Figure 25
t_{OFF}	70		ns typ	R_L = 300 Ω, C_L = 35 pF
	91	103	ns max	V_S = 8 V; see Figure 25

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
Break-Before-Make Time Delay, t_D	17		ns typ	R_L = 50 Ω, C_L = 35 pF
(ADG4613 Only)		11	ns min	V_{S1} = V_{S2} = 8 V; see Figure 26
Fault Response Time	250		ns typ	V_S = 9 V to 15 V, R_L = 300 Ω, C_L = 35 pF
Fault Recovery Time	1.4		µs typ	V_S = 9 V to 15 V, R_L = 300 Ω, C_L = 35 pF
Threshold Voltage, V_T	1.8		V typ	
Charge Injection	292		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 27
Off Isolation	−56		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Channel-to-Channel Crosstalk	−74		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Total Harmonic Distortion + Noise, THD + N	0.26		% typ	R_L = 110 Ω, 6 V p-p, f = 20 Hz to 20 kHz; see Figure 31
Insertion Loss	−0.27		dB typ	R_L = 50 Ω, C_L = 5 pF; f = 1 MHz; see Figure 30
−3 dB Bandwidth	250		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 30
C_S (Off)	11.5		pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	11.5		pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	48		pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS				
Normal Mode				V_{DD} = 13.2 V, V_{SS} = 0 V
I_{DD}	90		µA typ	Digital inputs = 0 V or V_{DD}
	140	165	µA max	
I_{DD}	600		µA typ	Digital inputs = 5 V
	660	900	µA max	
Isolation Mode				V_{DD} = 13.2 V, V_{SS} = 0 V or floating
I_{DD}	90		µA typ	V_S = 16 V or 1 V
	140	165	µA max	Digital inputs = 0 V or V_{DD}

[1] Guaranteed by design, not subject to production test.

5 V SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		−5.5 V to V_{DD}	V	V_{DD} to V_{SS} = 16 V maximum
On-Resistance (R_{ON})	12.5		Ω typ	V_S = 0 V to +4.5 V, I_S = −10 mA; see Figure 22
	14.7	17	Ω max	V_{DD} = 4.5 V, V_{SS} = 0 V,
On-Resistance Match Between Channels (ΔR_{ON})	0.15		Ω typ	V_S = 0 V to +4.5 V, I_S = −10 mA
	0.5	0.6	Ω max	
On-Resistance Flatness ($R_{FLAT (ON)}$)	6.2		Ω typ	V_S = 0 V to +4.5 V, I_S = −10 mA
	8	8.9	Ω max	
LEAKAGE CURRENTS				
Normal Mode				V_{DD} = 5.5 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.8		nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 23
	±3	±80	nA max	
Drain Off Leakage, I_D (Off)	±0.8		nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 23
	±3	±80	nA max	
Channel On Leakage, I_D (On), I_S (On)	±2		nA typ	V_S = V_D = 1 V or 4.5 V; see Figure 24
	±5	±120	nA max	
Isolation Mode				
Source Off Leakage, I_S (Off)	±0.05		µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V
	±0.15	±3	µA max	V_S = 1 V/16 V, V_D = 16 V/1 V; see Figure 23
	±10		µA typ	V_{DD} = 5.5 V, V_{SS} = 0 V
	±28	±38	µA max	V_S = 1 V/16 V, V_D = 16 V/1 V ; Figure 23
Drain Off Leakage, I_D (Off)	±0.05		µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V
	±0.15	±3	µA max	V_S = 1 V/16 V, V_D = 16 V/1 V; see Figure 23
	±10		µA typ	V_{DD} = 5.5 V, V_{SS} = 0 V
	±28	±38	µA max	V_S = 1 V/16 V, V_D = 16 V/1 V ; see Figure 23
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL}	±0.015		µA typ	V_{IN} = V_{GND}
	±0.1	±0.15	µA max	
Input Current, I_{INH}	±13		µA typ	V_{IN} = V_{DD}
	±16	±18	µA max	
Logic Pull-Down Resistance, R_{PD}	400		kΩ typ	
Digital Input Capacitance, C_{IN}	4		pF typ	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	116		ns typ	R_L = 300 Ω, C_L = 35 pF
	190	226	ns max	V_S = 3 V; see Figure 25
t_{OFF}	87		ns typ	R_L = 300 Ω, C_L = 35 pF
	120	136	ns max	V_S = 3 V; see Figure 25
Break-Before-Make Time Delay, t_D	70		ns typ	R_L = 50 Ω, C_L = 35 pF
(ADG4613 Only)		32	ns min	V_{S1} = V_{S2} = 3 V; see Figure 26
Fault Response Time	240		ns typ	V_S = 2 V to 8 V, R_L = 300 Ω, C_L = 35 pF
Fault Recovery Time	1.2		µs typ	V_S = 2 V to 8 V, R_L = 300 Ω, C_L = 35 pF
Threshold Voltage, V_T	1.8		V typ	
Charge Injection	75		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 27
Off Isolation	−54		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 28

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
Channel-to-Channel Crosstalk	−71		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 29
Total Harmonic Distortion + Noise, THD + N	0.85		% typ	R_L = 110 Ω, f = 20 Hz to 20 kHz, V_S = 3.5 V p-p; see Figure 31
Insertion Loss	−0.5		dB typ	R_L = 50 Ω, C_L = 5 pF; f = 1 MHz; see Figure 30
−3 dB Bandwidth	293		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 30
C_S (Off)	14		pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	14		pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	50		pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS				
Normal Mode				V_{DD} = 5.5 V, V_{SS} = 0 V
I_{DD}	90		µA typ	Digital inputs = 0 V or V_{DD}
	140	165	µA max	
Isolation Mode				V_{DD} = 5.5 V, V_{SS} = 0 V or floating
I_{DD}	90		µA typ	Digital inputs = 0 V or 5.5 V
	140	165	µA max	V_S = 1 V/16 V, V_D = 16 V/1 V

[1] Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, SX OR DX

Table 4.

Parameter	25°C	85°C	Unit
CONTINUOUS CURRENT, Sx OR Dx			
V_{DD} = +5 V, V_{SS} = −5 V			
TSSOP (θ_{JA} = 112°C/W)	109	52	mA maximum
LFCSP (θ_{JA} = 48.7°C/W)	160	83	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V			
TSSOP (θ_{JA} = 112°C/W)	113	56	mA maximum
LFCSP (θ_{JA} = 48.7°C/W)	175	87	mA maximum
V_{DD} = 5 V, V_{SS} = 0 V			
TSSOP (θ_{JA} = 112°C/W)	78	39	mA maximum
LFCSP (θ_{JA} = 48.7°C/W)	118	56	mA maximum

POWER SUPPLY OPERATION

Temperature range is −40°C to +105°C, unless otherwise noted.

Table 5.

Parameter	Min	Max	Unit	Comments
POWER SUPPLY				
V_{DD} to V_{SS}		16	V	GND = 0 V
V_{DD}	2.7	16	V	GND = 0 V
V_{SS}	−5.5	0	V	GND = 0 V
DUAL SUPPLY				
V_{SS}/V_{DD}	−5.5	+10.5	V	V_{DD} to V_{SS} = 16 V, GND = 0 V
SINGLE SUPPLY				
V_{DD}	0	16	V	V_{DD} to V_{SS} = 16 V, GND = 0 V, V_{SS} = 0 V
Analog Signal Range, V_D, V_S				
Normal Mode	−5.5	V_{DD}	V	V_{DD} to V_{SS} = 16 V maximum
Isolation Mode	−5.5	+16	V	Most negative (V_S, V_D, or V_{SS}) to most positive (V_S, V_D, Inx, or V_{DD}) = 16 V maximum

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	18 V
V_{DD} to GND	−0.3 V to +18 V
V_{SS} to GND	+0.3 V to −7 V
Analog Inputs; V_S to V_D	18 V
Analog Inputs; V_D , V_S	−7 V to +18 V
Most Negative (V_S,V_D or V_{SS}) to Most Positive (V_S,V_D, Inx, or V_{DD})	18 V
Digital Inputs, INx	GND − 0.3 V to +18 V
Peak Current, Sx or Dx	350 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, Sx or Dx[1]	Data + 15%
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb-free	260 (0/−5)°C

[1] See Table 4.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

THERMAL RESISTANCE

θ_{JA} is specified for a 4-layer board and, where applicable, with the exposed pad soldered to the board.

Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead TSSOP	112	°C/W
16-Lead LFCSP	48.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

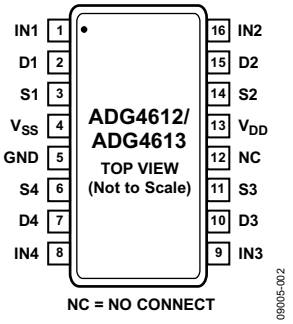


Figure 2. TSSOP Pin Configuration

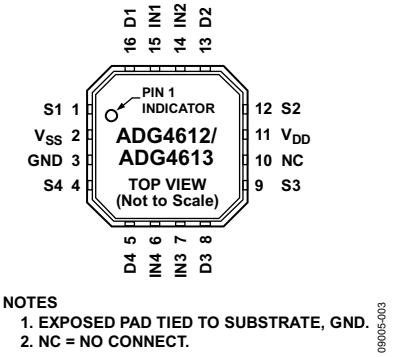


Figure 3. LFCSP Pin Configuration

Table 8. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	IN1	Logic Control Input 1. This pin has an internal 400 kΩ pull-down resistor to GND.
2	16	D1	Drain Terminal 1. Can be an input or output.
3	1	S1	Source Terminal 1. Can be an input or output.
4	2	V_{SS}	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Source Terminal 4. Can be an input or output.
7	5	D4	Drain Terminal 4. Can be an input or output.
8	6	IN4	Logic Control Input 4. This pin has an internal 400 kΩ pull-down resistor to GND.
9	7	IN3	Logic Control Input 3. This pin has an internal 400 kΩ pull-down resistor to GND.
10	8	D3	Drain Terminal 3. Can be an input or output.
11	9	S3	Source Terminal 3. Can be an input or output.
12	10	NC	No Connection.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	S2	Source Terminal 2. Can be an input or output.
15	13	D2	Drain Terminal 2. Can be an input or output.
16	14	IN2	Logic Control Input 2. This pin has an internal 400 kΩ pull-down resistor to GND.
N/A	0	EPAD	The exposed pad is connected to the substrate GND. For best heat dissipation, it is recommended that this pad be connected to GND. If heat dissipation is not a concern, it is possible to leave the pad floating. Connecting the exposed pad to V_{SS} (if V_{SS} is not equal to GND) can cause current to flow and can damage the part.

Table 9. ADG4612 Truth Table

ADG4612 INx	Switch Condition
1	On
0	Off

Table 10. ADG4613 Truth Table

ADG4613 INx	S1, S4	S2, S3
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

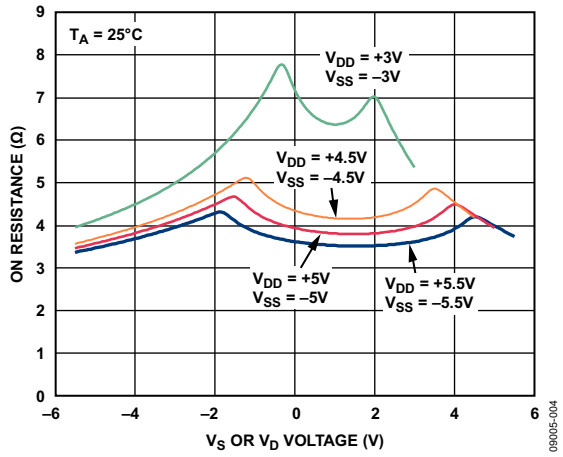


Figure 4. On Resistance as a Function of V_S, V_D (Dual Supply)

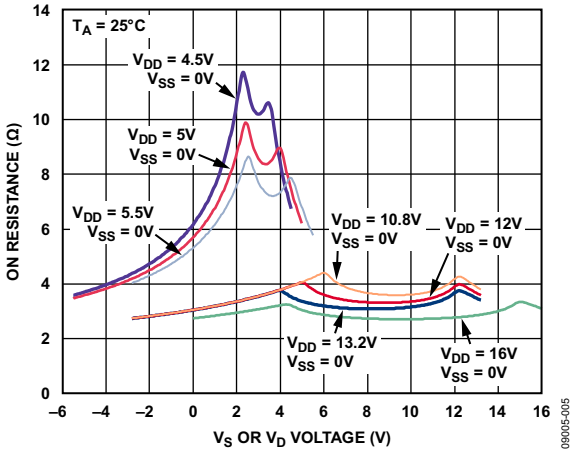


Figure 5. On Resistance as a Function of V_S, V_D (Single Supply)

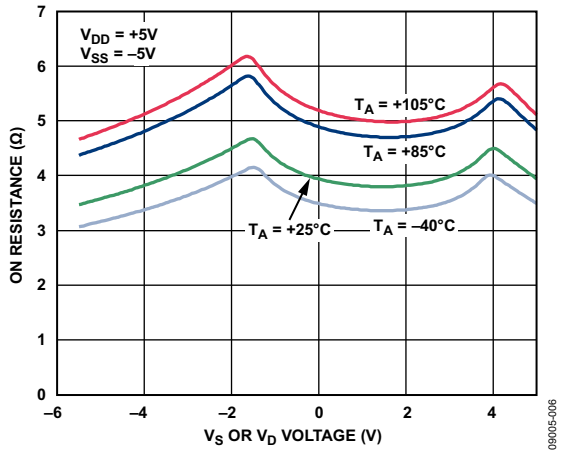


Figure 6. On Resistance as a Function of V_S, V_D for Different Temperatures, 5 V Dual Supply

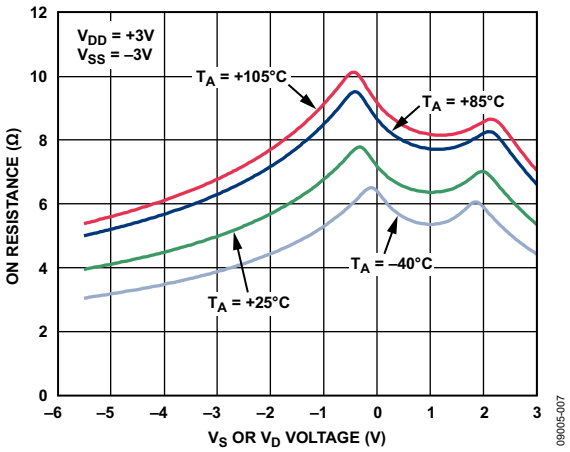


Figure 7. On Resistance as a Function of V_S, V_D for Different Temperatures, 3 V Dual Supply

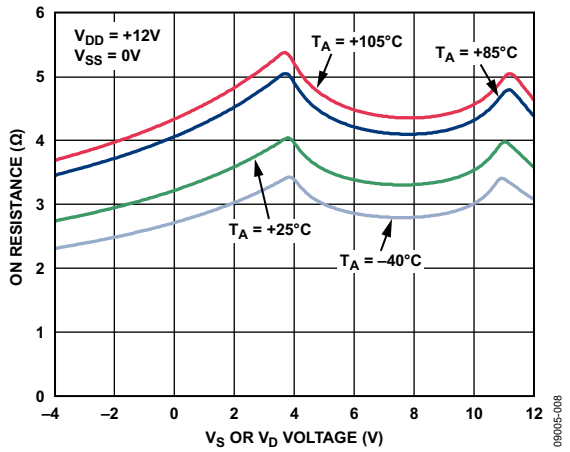


Figure 8. On Resistance as a Function of V_S, V_D for Different Temperatures, 12 V Single Supply

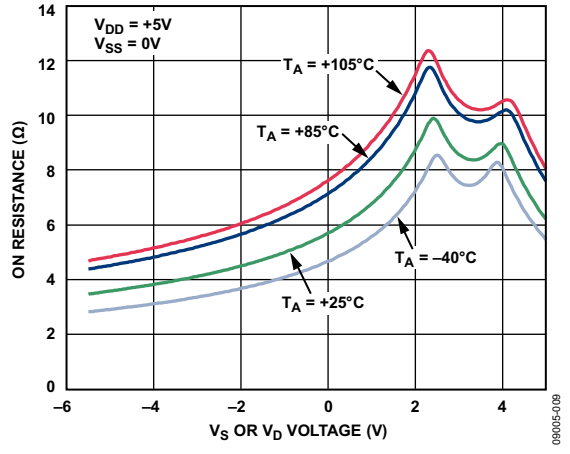


Figure 9. On Resistance as a Function of V_S, V_D for Different Temperatures, 5 V Single Supply

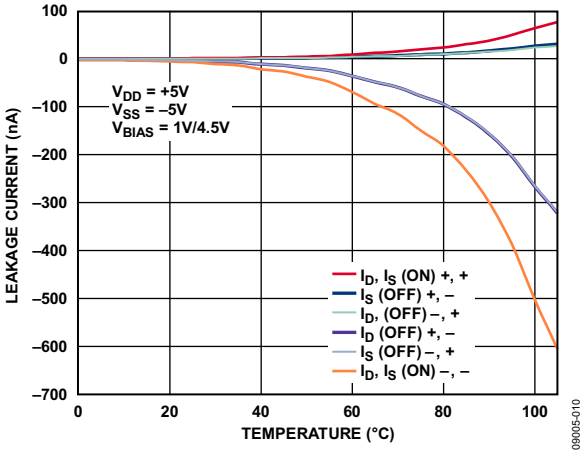


Figure 10. Leakage Currents as a Function of Temperature, 5 V Dual Supply

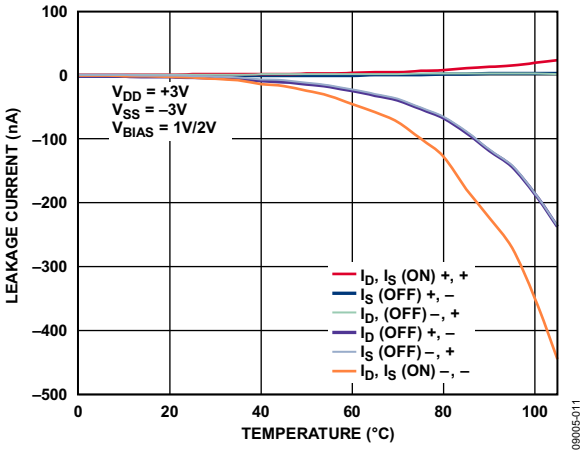


Figure 11. Leakage Currents as a Function of Temperature, 3 V Dual Supply

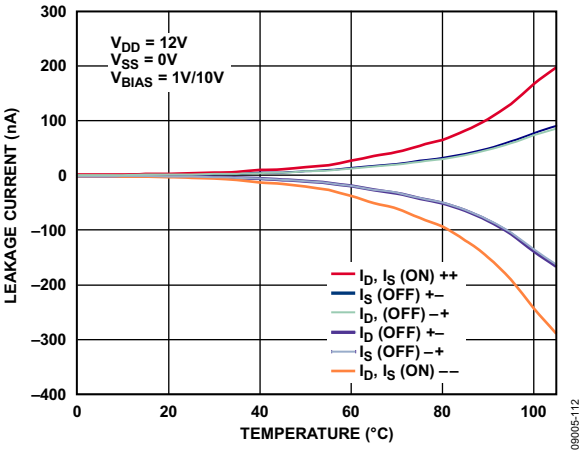


Figure 12. Leakage Currents as a Function of Temperature, 12 V Single Supply

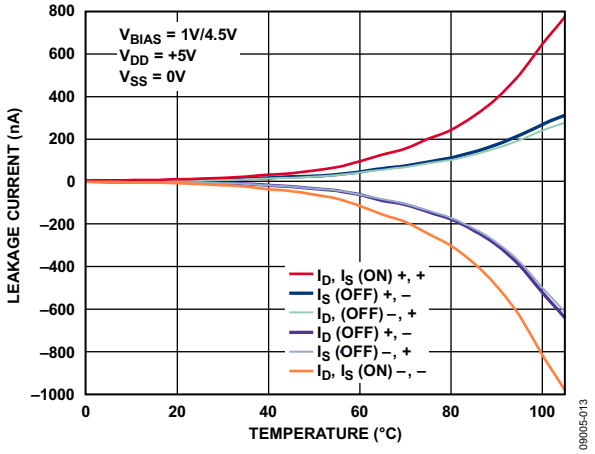


Figure 13. Leakage Currents as a Function of Temperature, 5 V Single Supply

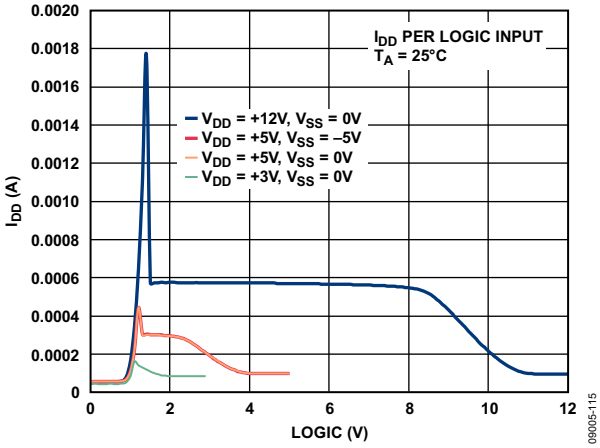


Figure 14. I_{DD} vs. Logic Level

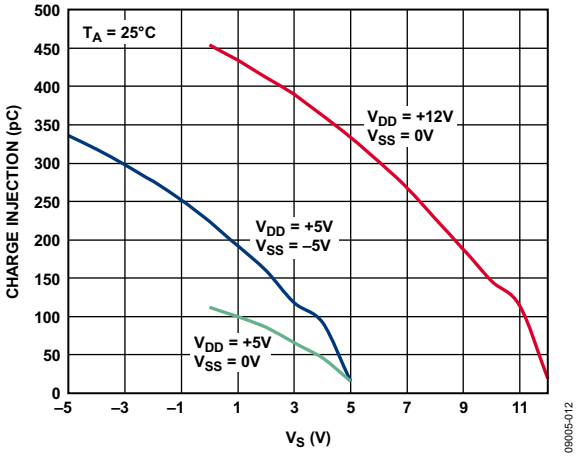


Figure 15. Charge Injection vs. Source Voltage

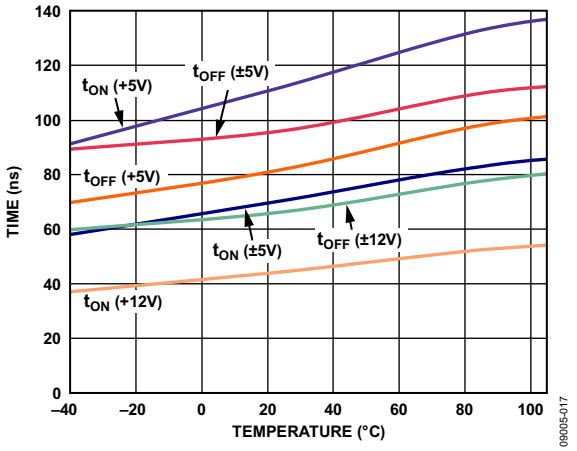


Figure 16. t_{ON}/t_{OFF} Times vs. Temperature

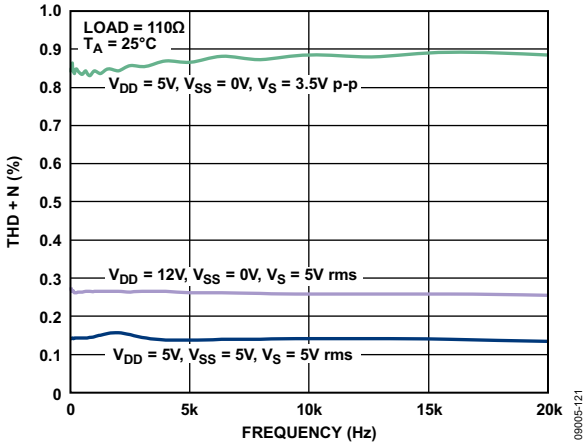


Figure 19. THD + N vs. Frequency

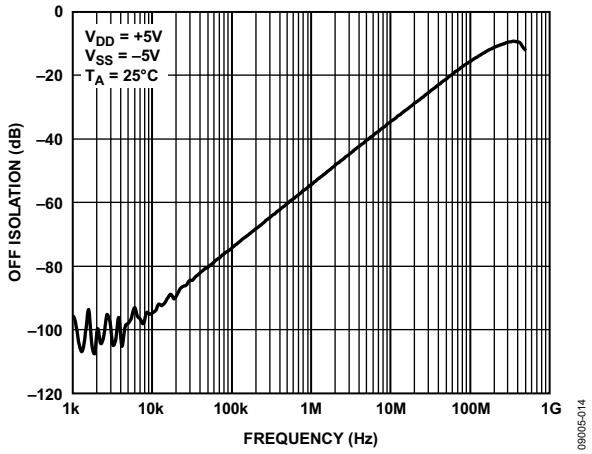


Figure 17. Off Isolation vs. Frequency

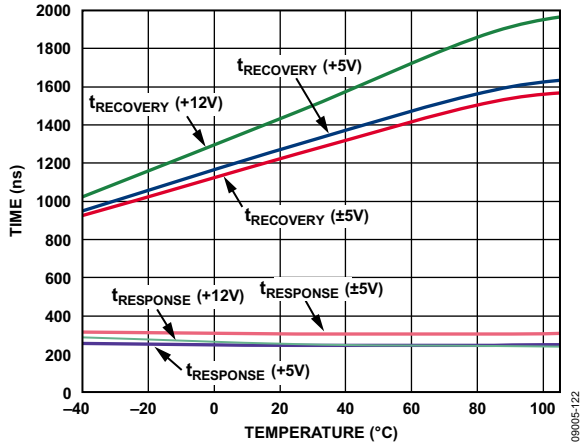


Figure 20. Fault Response Time/Fault Recovery Time

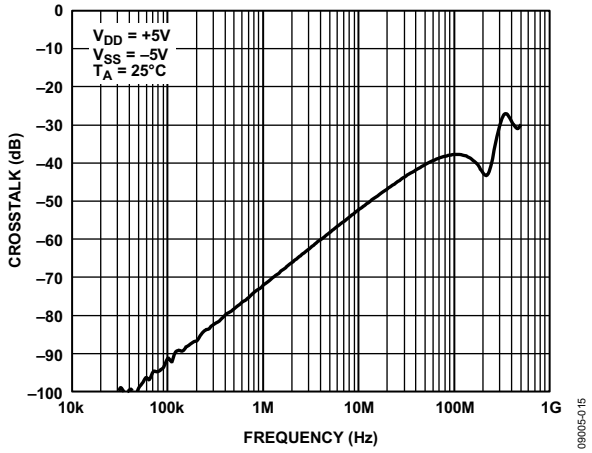


Figure 18. Crosstalk vs. Frequency

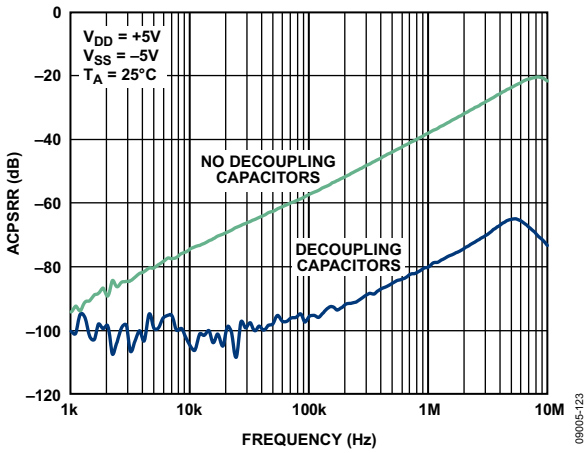


Figure 21. ACPSRR vs. Frequency

TEST CIRCUITS

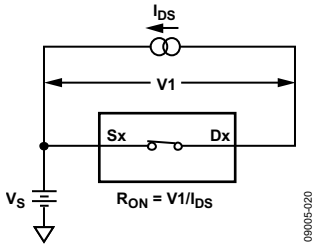


Figure 22. On Resistance

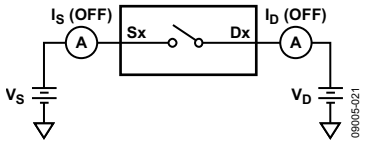


Figure 23. Off Leakage

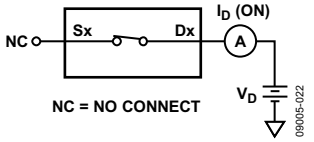


Figure 24. On Leakage

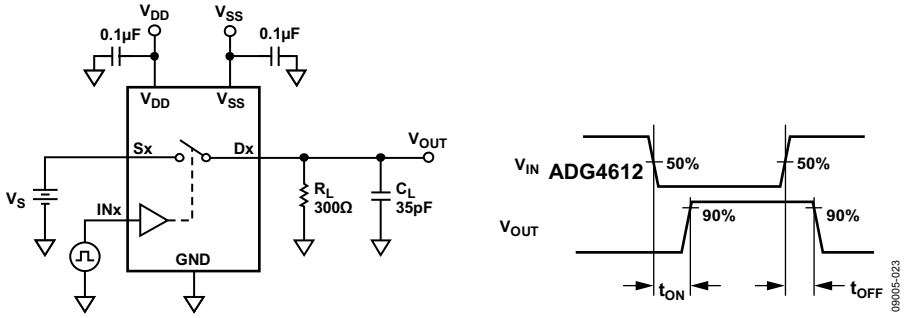


Figure 25. Switching Times

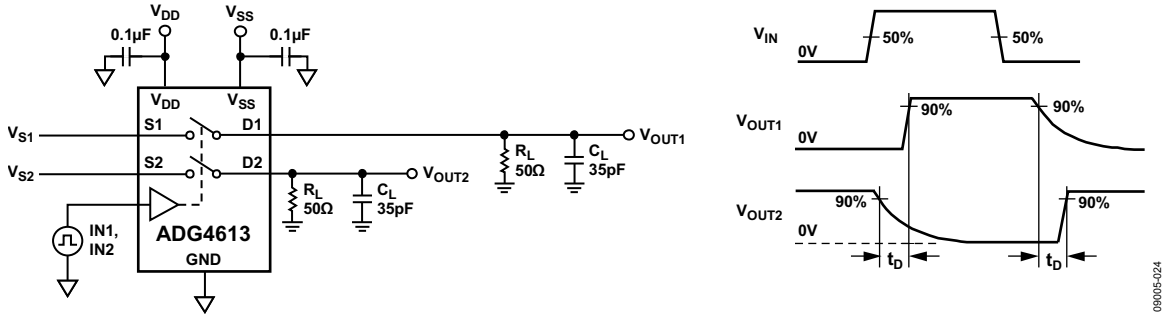


Figure 26. Break-Before-Make Time Delay, t_D

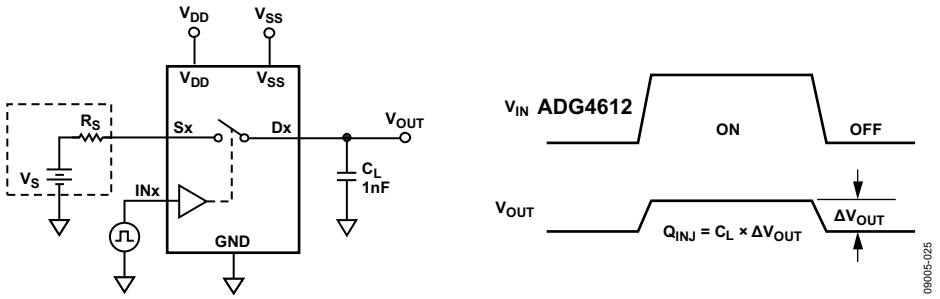


Figure 27. Charge Injection

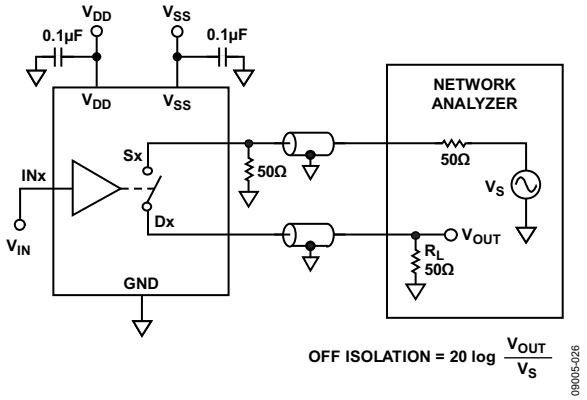


Figure 28. Off Isolation

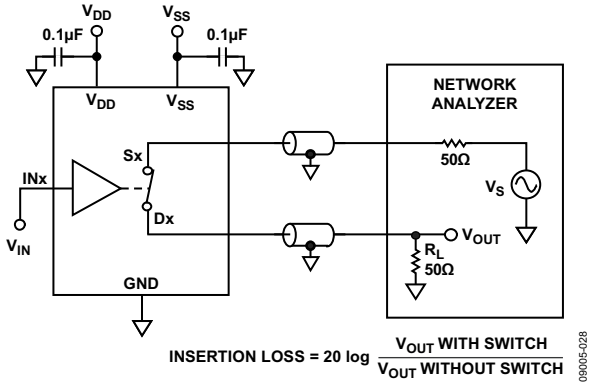


Figure 30. Bandwidth

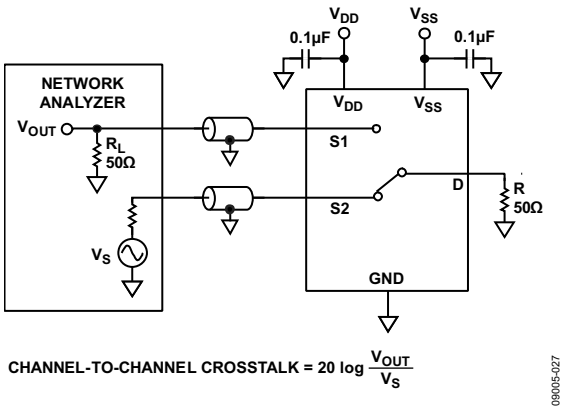


Figure 29. Channel-to-Channel Crosstalk

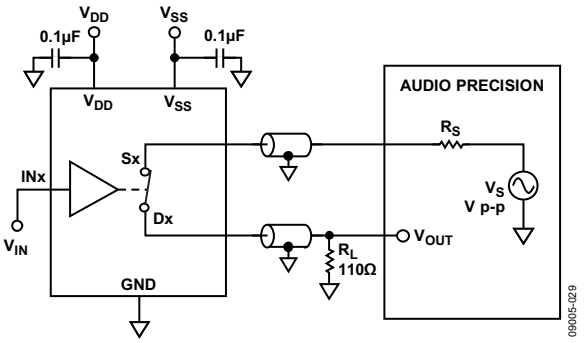


Figure 31. THD + Noise

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}
R_{ON} represents the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by $R_{FLAT (ON)}$.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON}
t_{ON} represents the delay between applying the digital control input and the output switching on.

t_{OFF}
t_{OFF} represents the delay between applying the digital control input and the output switching off.

t_D
t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Fault Response Time
Fault response time is the delay between a fault condition ($V_S > V_{DD}$) on an analog input and the corresponding output below V_{DD}.

Fault Recovery Time
Fault recovery time is, in recovering from a fault condition, the delay between 50% of the input signal to 90% of the output signal.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

THEORY OF OPERATION

The ADG4612/ADG4613 contain four independent single-pole/single-throw (SPST) switches. Each switch is rail-to-rail and conducts equally well in both directions when on.

The ADG4612/ADG4613 has two modes of operation: normal mode and isolation mode.

The operation modes are made possible by a special detection circuitry that monitors the voltage levels at the source or drain terminals and V_{DD} relative to ground. Depending on these voltage levels, the device operates in normal mode or isolation mode accordingly.

Isolation mode is a useful feature that isolates the inputs from the outputs where input signals may be present before supplies or during positive fault conditions that can occur in applications.

Normal Mode

In normal mode, the switch functions as a normal 4 × SPST switch, whereby the switch is controlled by the logic input pins, IN1 to IN4.

The following three conditions need to be satisfied for the switch to be in the on condition;

- $V_{DD} \geq 2.7$ V; and
- Input signal, V_S, $V_D < V_{DD} + V_T$; and
- Logic input, INx set to on level

When the switch is in the on condition, if the signal range is from V_{DD} to −5.5 V, the signals present on the switch inputs are passed through to the switch output. If the analog input exceeds V_{DD} by a threshold voltage, V_T, the switch turns off and is in isolation mode.

If the analog input signal exceeds the negative supply, V_{SS}, when the switch is off, the switch blocks a signal up to −5.5 V. If the switch is on, the switch remains on, and this signal is passed to the output. See the Negative Fault Condition; Negative Signal Handling section for more details.

Isolation Mode

In isolation mode, all switches are in the off condition. The switch inputs are isolated from the switch outputs. The switch inputs are high impedance inputs with greater than 475 kΩ impedance to V_{DD} ground and across the switch. This prevents any current from flowing that can damage the switch. This is very useful in applications where analog signals may be present at the switch inputs before power is present or where the user has no control over the power supply sequence.

The switch is in isolation mode when

- No power supplies are present, that is, when V_{DD} is floating or $V_{DD} \leq 1$ V; or
- Input signal, V_S, $V_D > V_{DD} + V_T$

The negative supply rail, V_{SS}, can be floating or 0 V to −5.5 V. The ground pin must be connected to the ground potential.

Table 11. Switch Operation Mode

V_{DD}	V_{SS}[1]	GND	V_S, V_D (Input Voltage, Sx or Dx)	Switch Condition	Switch Mode
Floating	X	0 V	−5.5 V to +10.5 V 0 V to 16 V	All switches off Inputs isolated from outputs	Isolation
0 V to 0.8 V	X	0 V	−5.5 V to +10.5 V 0 V to 16 V	All switches off Inputs isolated from outputs	Isolation
$V_{DD} \geq 2.7$ V	X	0 V	V_S, $V_D > V_{DD} + V_T$	All switches off Inputs isolated from outputs	Isolation
$V_{DD} \geq 2.7$ V to 16 V	0 V to −5.5 V	0 V	V_{DD} to V_{DD} − 16 V	Switch state is determined by logic levels, INx	Normal

[1] X = don't care; for example, floating, 0 V to −5.5 V.

BIPOLAR OPERATION AND SINGLE-SUPPLY OPERATION

The ADG4612/ADG4613 have a maximum operational range from V_{DD} to V_{SS} of 16 V. The maximum signal range from source to drain, V_S to V_D, is also 16 V. During operation of the device, the signal range can exceed the power supply rails, but the voltage between the most negative voltage on the device (V_S,V_D or V_{SS}) should be within 16 V of the most positive voltage (V_S, V_D, INx, or V_{DD}). These voltage ratings should be adhered to at all times for guaranteed functionality. See Table 5 for guaranteed supply ranges. Signal ranges and power supply ranges exceeding 16 V may affect the long-term reliability of the device.

The ground pin must always be connected to the GND potential to ensure proper functionality in isolation and normal operation mode.

The minimum V_{DD} voltage that the part is guaranteed operational is 2.7 V. The maximum recommended V_{DD} voltage is 16 V.

The minimum supply voltage recommended on V_{SS} is −5.5 V, and the maximum voltage allowable on V_{SS} is 0 V. Therefore, given that the V_{DD} to V_{SS} range is 16 V maximum when, V_{SS} = −5.5 V, the V_{DD} = +10.5 V maximum.

Positive Fault Condition

If the analog input exceeds V_{DD} by a threshold voltage, V_T, then the switch turns off and is in isolation mode. The part can handle a fault of up to 16 V, referenced to the most negative signal. For example, if V_{DD}= 5 V, V_{SS} = 0 V, then the switch protects against an overvoltage of up to 16 V. If V_{SS} = −5 V and V_{DD} = +5 V, then the switch protects against an overvoltage of up to +11 V.

Negative Fault Condition; Negative Signal Handling

The ADG4612/ADG4613 are not damaged if the analog inputs exceed the negative supply, V_{SS}. If the switch is in the off condition, the switch blocks a signal up to −5.5 V. If the switch is in the on condition, the switch remains on, and the negative signal is passed to the output; therefore, the ADG4612/ADG4613 can pass a negative signal up to −5.5 V with V_{SS} = 0 V. The user must ensure that the downstream circuitry can handle this signal level. Also, the user should ensure the voltage between the most negative voltage on the device (V_S ,V_D or V_{SS}) is within 16 V of the most positive voltage (V_S, V_D, INx, or V_{DD}).

APPLICATIONS INFORMATION

There are many application scenarios that benefit from the functionality offered on the ADG4612/ADG4613 switches.

The ADG4612/ADG4613 offer power-off protection, ensuring the switch is guaranteed off and inputs are high impedance with no power supplies present. This isolation mode is a useful feature that isolates the inputs from the outputs where input signals may be present before supplies. The isolation mode also protects the system against positive fault conditions that can occur in applications, ensuring that the switch turns off and protects downstream circuitry. For example, a module can be connected to a live backplane, supplying signals to the board before supplies are present. This is common in hot swap applications where a card could be hot plugged in a shelf where there are others cards already working and powered on.

The ADG4612/ADG4613 allow negative signals, down to −5.5 V to be passed without a negative supply. This can be very useful in applications that need to pass negative signals but do not have a negative supply available. This cannot be done with conventional CMOS switches because ESD protection diodes turn on and clamp the signals.

Theses features ensure the system is very robust to power supply sequencing issues that can be present in conventional CMOS devices.

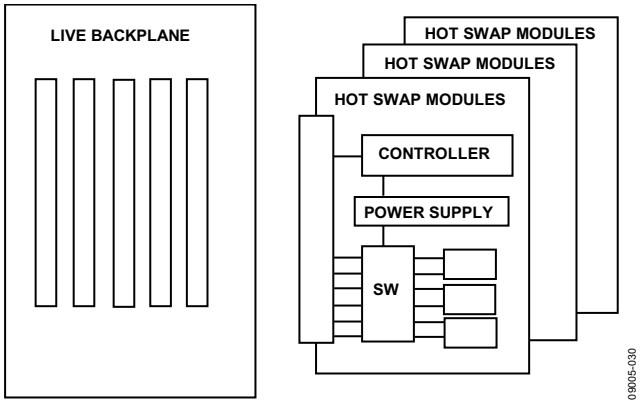


Figure 32. Typical Application

Signals on Inputs with No Power Present

In conventional CMOS switches, ESD protection diodes can be found on the analog and digital inputs to V_{DD} and GND or V_{SS} (see Figure 33, for example). If an input voltage is present on the switch inputs with no power supplies applied, current can flow through the ESD protection diodes. If this current is not limited to a safe level, it is possible to damage the ESD protection diodes and, hence, the switch. Input signals may pass through the switch to the output affecting downstream circuitry. The user may also be exceeding the absolute maximum ratings of the devices, and, therefore, affecting the long-term reliability of the device.

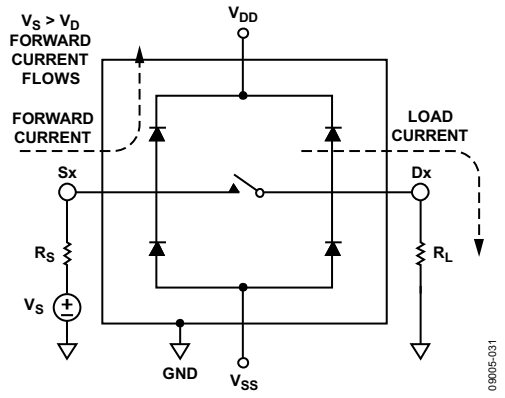


Figure 33. ESD Protection Diodes on Conventional CMOS Switch

Some users add external diodes or add current-limiting resistors to protect the device against the conditions shown in Figure 33. However, these solutions all have disadvantages in that they add extra board area, extra component count, and cost. The system level performance can also be affected by the higher on resistance from the current-limiting resistors or the higher leakage from external Schottky diodes. Using external diodes for protection still creates the problem where a floating V_{DD} line can be pulled up to a diode drop from the input signal.

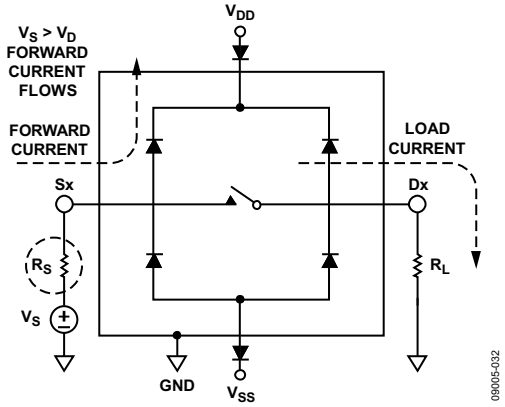


Figure 34. External Protection Added to Protect Switch Against Damage If Signals Present on Inputs Without Power Supplies

The ADG4612/ADG4613 eliminate the concerns shown in Figure 34. There are no internal ESD diodes from the analog or digital inputs to V_{DD} or V_{SS}. If signals are present on the ADG4612/ADG4613 inputs before power is present, the switch is in isolation mode, which means that the inputs have high impedance to V_{DD}, GND, and the output. This prevents current flow and protects the device from damage.

Power Supply Sequencing

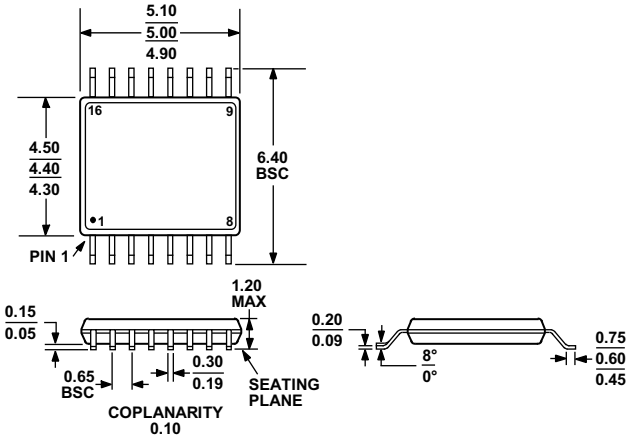
Another benefit of the ADG4612/ADG4613 is it eliminates concerns about the power supply sequence. The part can be powered up in any sequence without damage. For devices with conventional CMOS switches, it is recommend that power supplies are powered up before analog or digital inputs are present. The ADG4612/ADG4613 do not have any power supply sequencing requirements, thereby making them a very robust design. However, a ground must first be present for the device to function in isolation mode and normal mode.

V_{DD} Supply

Another area of concern with conventional CMOS switches that have analog signals present before the part is powered up is that the V_{DD} supply can be pulled up through the internal ESD protection diodes. The V_{DD} supply normally gets pulled up to the input voltage level minus a diode drop, $V_{DD} \sim V_S$, $V_D - V_{DIODE}$. This voltage can be high enough to power up other chips that are connected to this supply rail in a system, potentially damaging other components in that system.

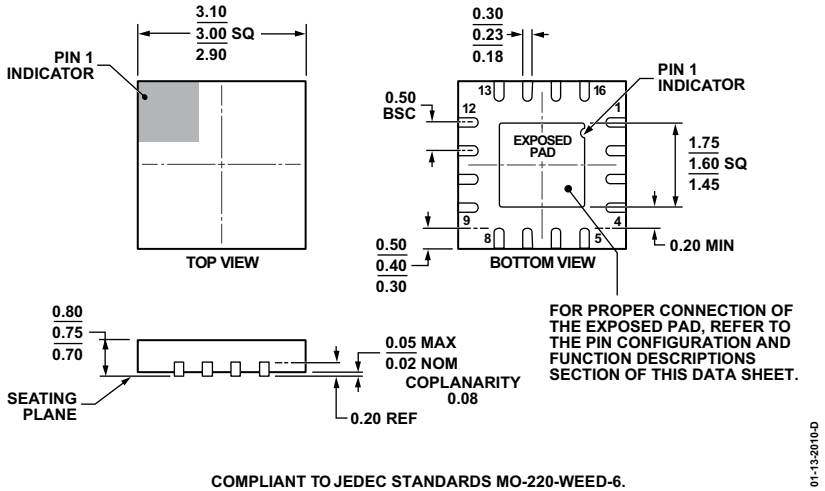
The ADG4612/ADG4613 architecture ensures that the V_{DD} supply is isolated from the analog inputs, thereby preventing the supplies from being pulled to a higher potential when a signal is present on the inputs without any power having been applied.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 36. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADG4612BRUZ	−40°C to +105°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG4612BRUZ-REEL7	−40°C to +105°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG4612BCPZ-REEL7	−40°C to +105°C	Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	LG5
EVAL-ADG4612EBZ		Evaluation Board		
ADG4613BRUZ	−40°C to +105°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG4613BRUZ-REEL7	−40°C to +105°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG4613BCPZ-REEL7	−40°C to +105°C	Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	S3Y

[1] Z = RoHS Compliant Part.

NOTES

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