



CTL240NS10-T52

N-Channel Enhancement MOSFET

Features

- Drain-Source Breakdown Voltage V_{DSS} 100V
- Drain-Source On-Resistance
 $R_{DS(ON)}$ 25m Ω , at $V_{GS}= 10V, I_D= 10A$
 $R_{DS(ON)}$ 33m Ω , at $V_{GS}= 5V, I_D= 10A$
- Continuous Drain Current at $T_C=25^\circ C I_D =24A$
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

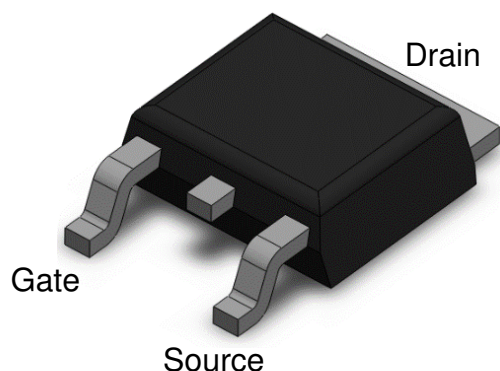
Description

The CTL240NS10-T52 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application.

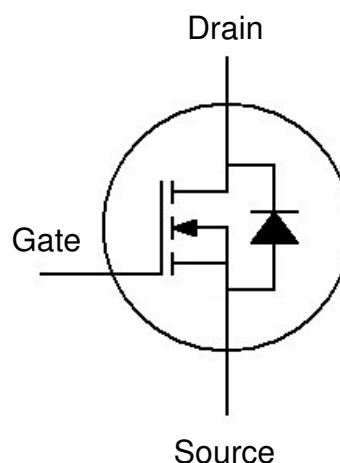
Applications

- DC/DC Converter
- Load Switch
- LCD/LED Display inverter

Package Outline



Schematic





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Absolute Maximum Rating at 25°C

| Symbol | Parameters | Test Conditions | Min | Note |
|------------------|--|-----------------|-----|------|
| V _{DS} | Drain-Source Voltage | 100 | V | |
| V _{GS} | Gate-Source Voltage | ±20 | V | |
| I _D | Continuous Drain Current @T _C =25°C | 24 | A | 1 |
| I _{DM} | Pulsed Drain Current | 96.2 | A | 1 |
| P _D | Total Power Dissipation @T _C =25°C | 27.7 | W | 2 |
| T _{STG} | Storage Temperature Range | -55 to 150 | °C | |
| T _J | Operating Junction Temperature Range | -55 to 150 | °C | |

Thermal Characteristics

| Symbol | Parameters | Test Conditions | Min | Typ | Max | Units | Notes |
|------------------|-------------------------------------|-----------------|-----|-----|-----|-------|-------|
| R _{θJC} | Thermal Resistance Junction-Case | | -- | -- | 4.5 | °C /W | 1,4 |



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Electrical Characteristics $T_A = 25^\circ\text{C}$ (unless otherwise specified)

Static Characteristics

| Symbol | Parameters | Test Conditions | Min | Typ | Max | Units | Notes |
|------------|--------------------------------|---------------------------------|-----|-----|-----------|---------|-------|
| B_{VDSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0V, I_D = 250\mu A$ | 100 | - | - | V | |
| I_{DSS} | Drain-Source Leakage Current | $V_{DS} = 100V, V_{GS} = 0V$ | - | - | 1 | μA | |
| I_{GSS} | Gate-Source Leakage Current | $V_{GS} = \pm 20V, V_{DS} = 0V$ | - | - | ± 100 | nA | |

On Characteristics

| Symbol | Parameters | Test Conditions | Min | Typ | Max | Units | Notes |
|--------------|-------------------------------|-----------------------------------|-----|-----|-----|------------|-------|
| $R_{DS(ON)}$ | Drain-Source On-Resistance | $V_{GS} = 10V, I_D = 10A$ | - | 25 | 30 | m Ω | 3 |
| | | $V_{GS} = 5V, I_D = 10A$ | - | 33 | 43 | m Ω | 3 |
| $V_{GS(th)}$ | Gate-Source Threshold Voltage | $V_{GS} = V_{DS}, I_D = 250\mu A$ | 2.0 | - | 4.0 | V | 3 |

Dynamic Characteristics

| Symbol | Parameters | Test Conditions | Min | Typ | Max | Units | Notes |
|-----------|------------------------------|--|-----|------|-----|-------|-------|
| C_{ISS} | Input Capacitance | $V_{GS} = 0V,$ $V_{DS} = 50V$ $f = 1MHz$ | - | 3340 | - | pF | |
| C_{OSS} | Output Capacitance | | - | 120 | - | | |
| C_{RSS} | Reverse Transfer Capacitance | | - | 87.7 | - | | |

Switching Characteristics

| Symbol | Parameters | Test Conditions | Min | Typ | Max | Units | Notes |
|--------------|----------------------------|--|-----|------|-----|-------|-------|
| $T_{D(ON)}$ | Turn-On Delay Time | $V_{DS} = 50V, R_G = 3\Omega$ $V_{GS} = 10V, R_L = 5\Omega$ | - | 29.3 | - | ns | |
| T_R | Rise Time | | - | 26.2 | - | | |
| $T_{D(OFF)}$ | Turn-Off Delay Time | | - | 70.2 | - | | |
| T_F | Fall Time | | - | 10.1 | - | | |
| Q_G | Total Gate Charge | $V_{DS} = 50V,$ $V_{GS} = 4.5V,$ $I_D = 10A$ | - | 33 | - | nC | |
| Q_{GS} | Gate-Source Charge | | - | 16.3 | - | | |
| Q_{GD} | Gate-Drain (Miller) Charge | | - | 20.4 | - | | |



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Drain-Source Diode Characteristics

| Symbol | Parameters | Test Conditions | Min | Typ | Max | Units | Notes |
|----------|-------------------------------|----------------------------|-----|-----|-----|-------|-------|
| V_{SD} | Body Diode Forward Voltage | $V_{GS} = 0V, I_{SD} = 1A$ | - | 0.7 | 1 | V | 1 |
| I_{SD} | Body Diode Continuous Current | | - | - | 1 | A | 1 |

Note:

1. The power dissipation is limited by 150°C junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. Thermal Resistance follow JESD51-3.



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Typical Characteristic Curves

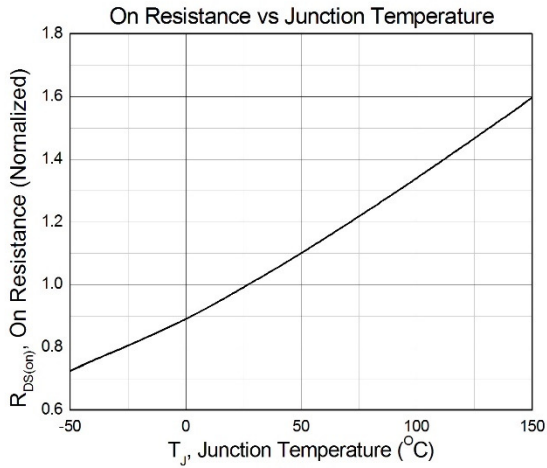


Figure 1

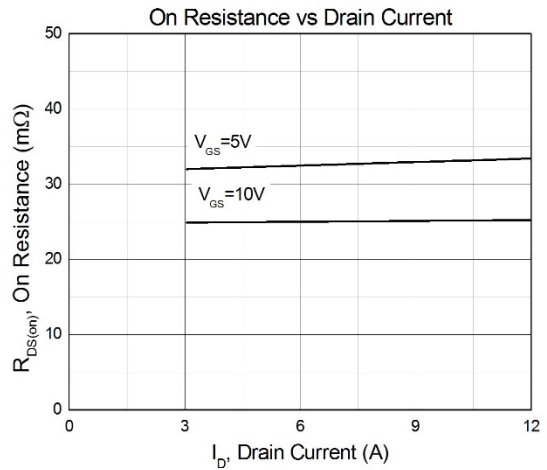


Figure 2

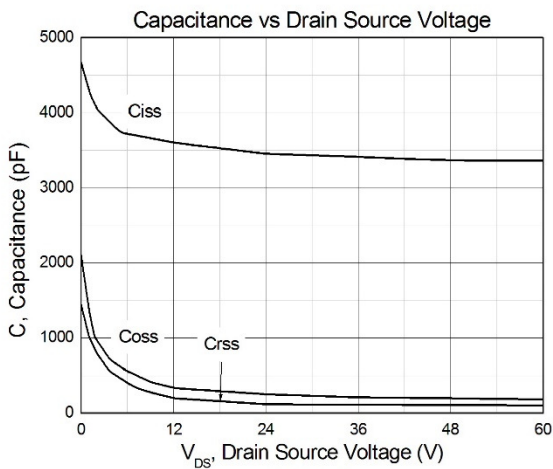


Figure 3

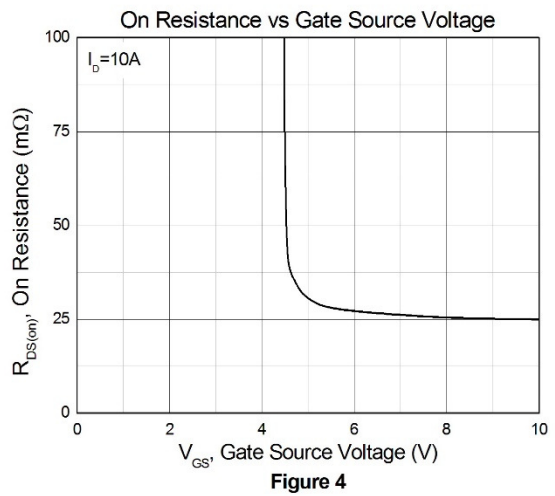


Figure 4

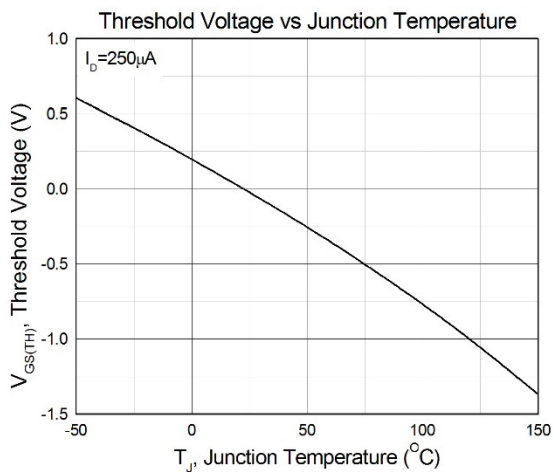


Figure 5

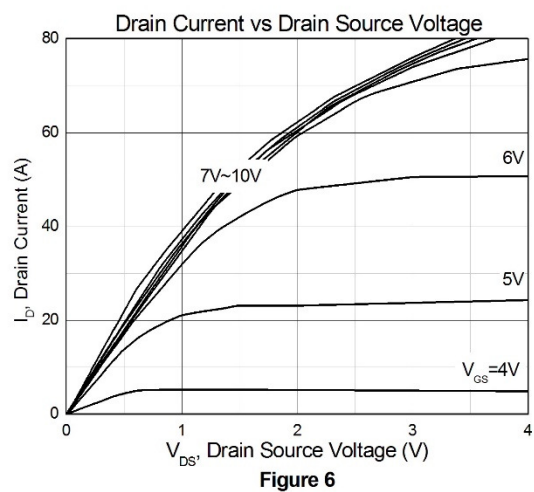


Figure 6



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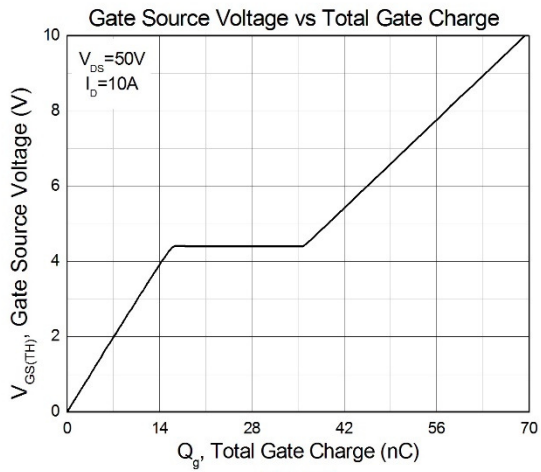


Figure 7

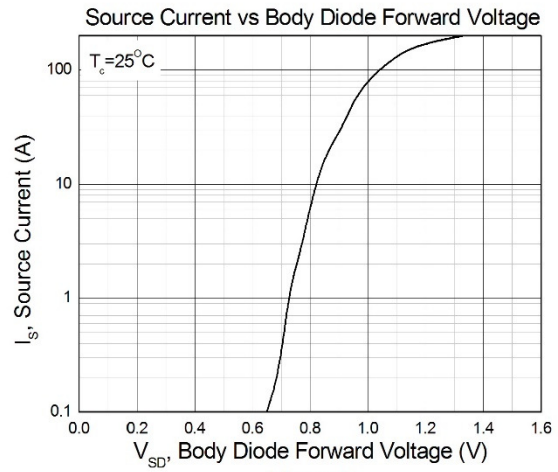


Figure 8



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Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

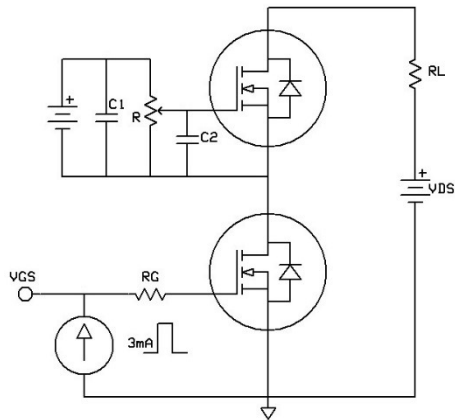


Figure 10: Gate Charge Waveform

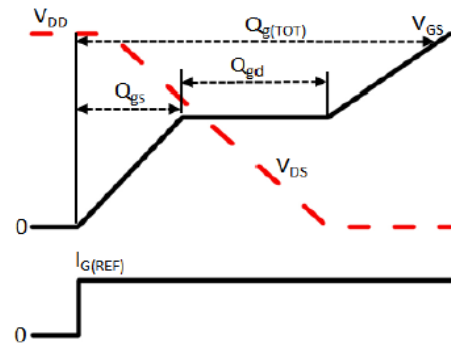


Figure 11: Switching Time Test Circuit

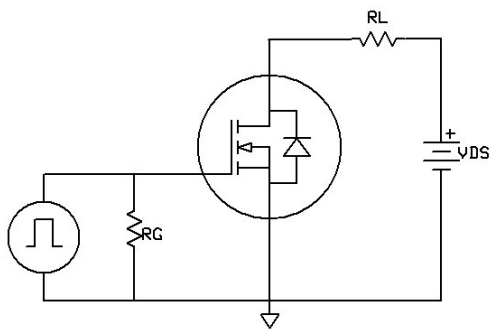
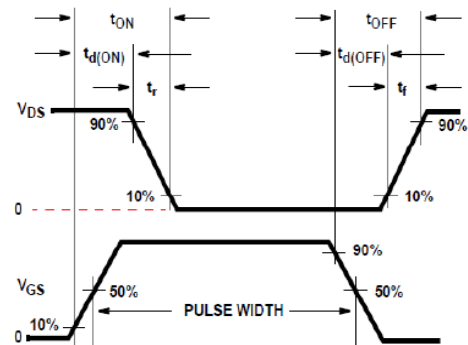


Figure 12: Switching Time Waveform

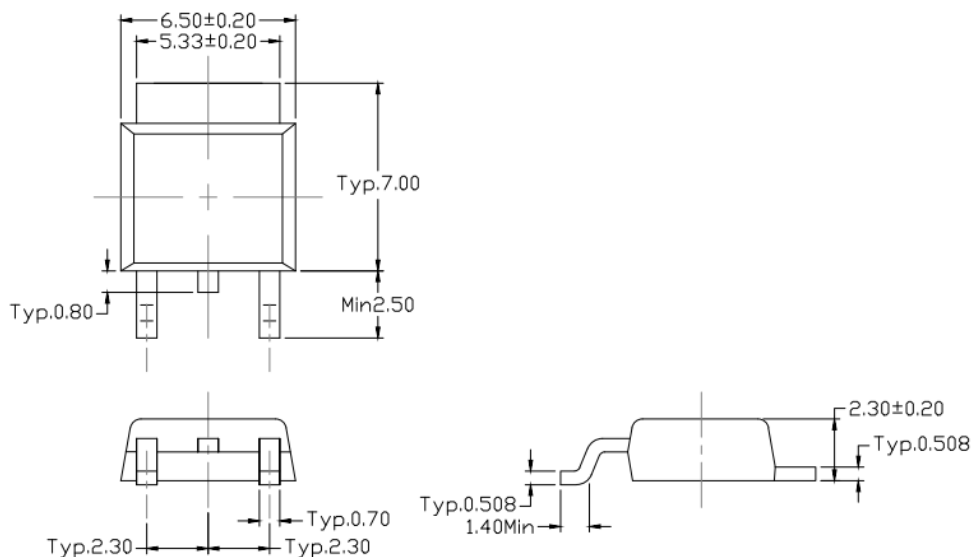




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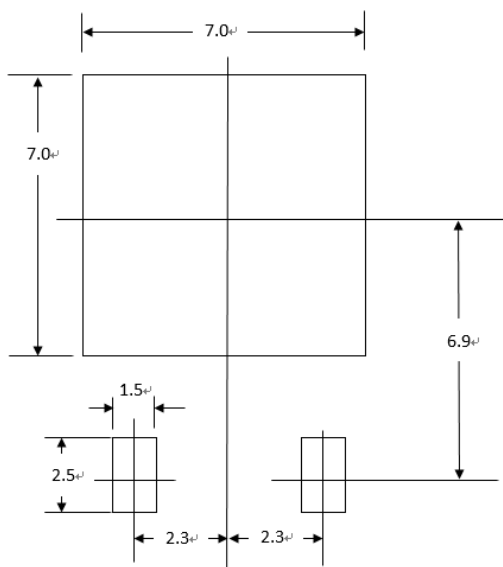
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Package Dimension (TO-252)

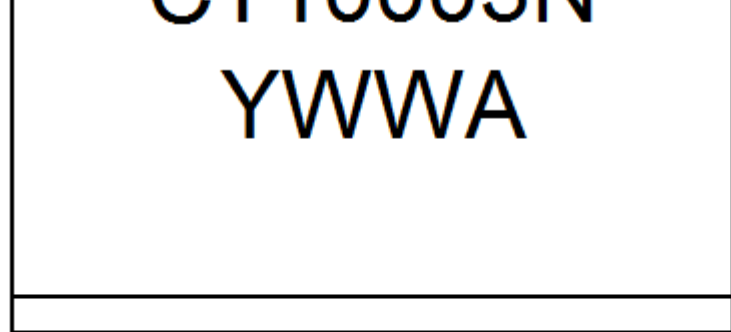


Dimensions in mm unless otherwise stated

Recommended pad layout for surface mount leadform

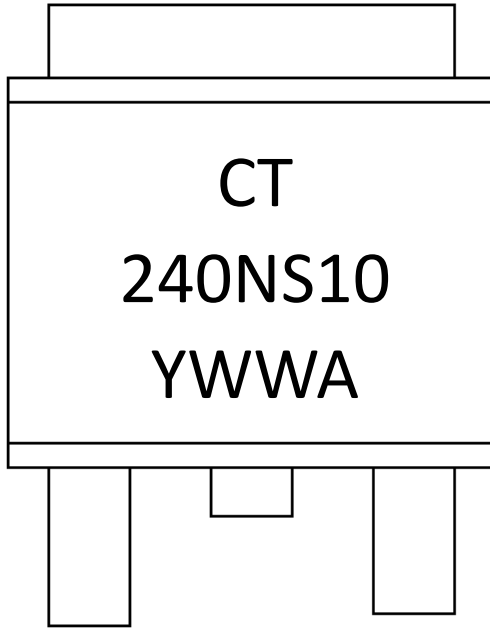


Dimensions in mm unless otherwise stated



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CT : Denotes "CT M"
 240NS10 : Device Numbe
 Y : Fiscal Year
 WW : Work Week
 A : Production Coc

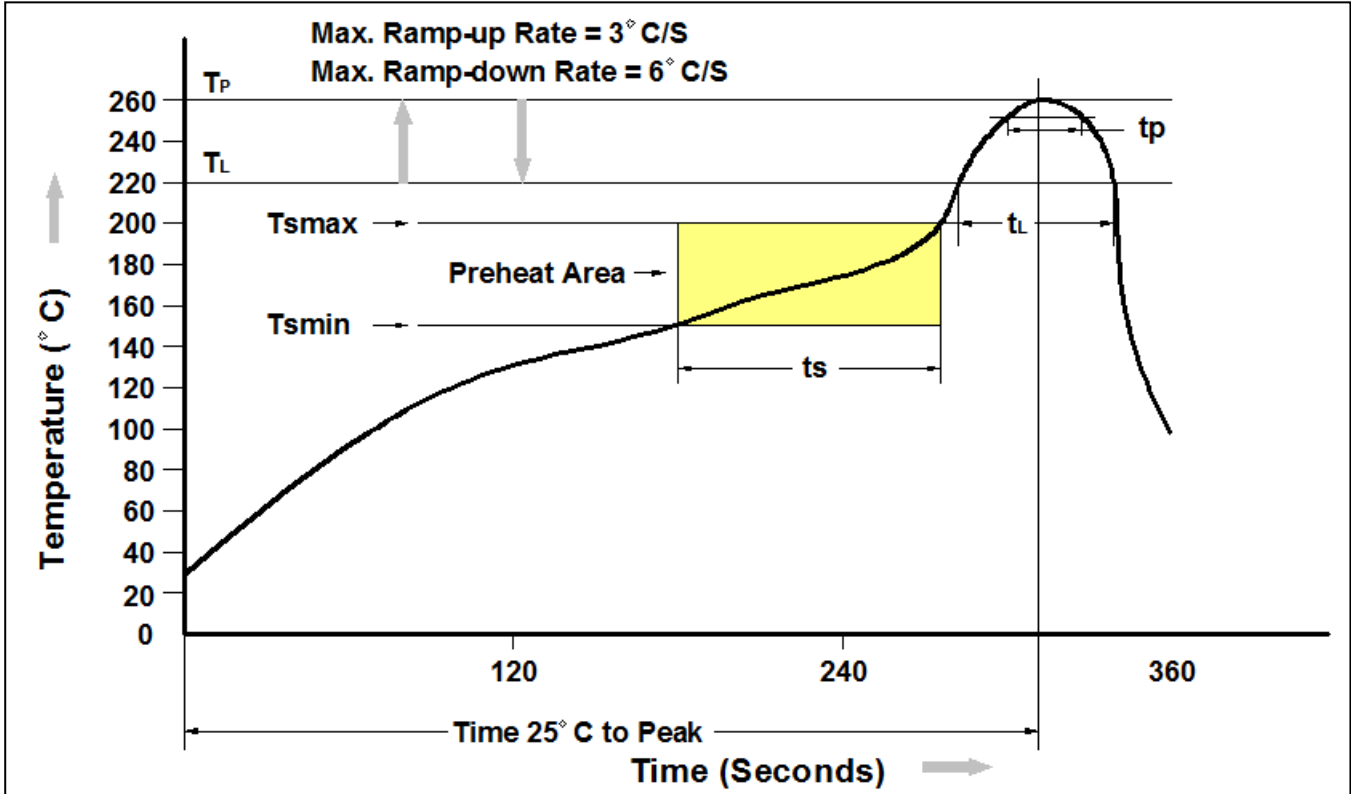


Ordering Information

| Part Number | Description | Quantity |
|--------------------|--------------------|-----------------|
| CTL240NS10-T52 | TO-252 Reel | 2500 pcs |



Reflow Profile



| Profile Feature | Pb-Free Assembly Profile |
|---|--------------------------|
| Temperature Min. (T _{smin}) | 150 °C |
| Temperature Max. (T _{smax}) | 200 °C |
| Time (t _s) from (T _{smin} to T _{smax}) | 60-120 seconds |
| Ramp-up Rate (t _L to t _P) | 3 °C/second max. |
| Liquidous Temperature (T _L) | 217 °C |
| Time (t _L) Maintained Above (T _L) | 60 – 150 seconds |
| Peak Body Package Temperature | 260 °C +0 °C / -5 °C |
| Time (t _P) within 5 °C of 260 °C | 30 seconds |
| Ramp-down Rate (T _P to T _L) | 6 °C/second max |
| Time 25 °C to Peak Temperature | 8 minutes max. |



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