DG485
Low-Power CMOS Octal Analog Switch Array

FEATURES
- ±15 Volt Input Range
- ON-Resistance < 85 Ω
- Serial Data Input/Output
- Low-Power (P_D < 105 µW)
- TTL and CMOS Compatible
- Any Combination of 8 SPST to the Output
- ESD Protection > ±4000 V

BENEFITS
- Devices Can Be Chained for System Expansion
- Reduced Control Wires
- Reduced Board Space
- Low Signal Distortion
- Reduced Switch Errors
- Reduced Power Supply
- Simple Interfacing
- Improved Reliability

APPLICATIONS
- Audio Switching and Routing
- Audio Teleconferencing
- Serial Data Acquisition and Process Control
- Battery and Remote Systems
- Automotive, Avionics and ATE Systems
- Summing Node Amplifiers

DESCRIPTION

The DG486 is an analog switch array that may be used as a low power 8-channel multiplexer for use in serial control applications. Any, all or none of the 8 switches may be closed at any given time. Combining low ON-resistance ($t_{DS(ON)}$ <85 Ω) and *fast switching* (t_{ON} <200 ns), the DG485 is ideally suited for data acquisition, process control, communication, and avionic applications.

The control data is input serially into the shift register with each clock pulse. The shift register contents can be latched-in via LD at any point into an octal latch which in turn controls all switches. $\overline{RS}$ resets the shift register, forcing all latch inputs to a LOW condition. The serial input (D_{IN}) and serial output (D_{OUT}) allow chaining of arrays for large systems.

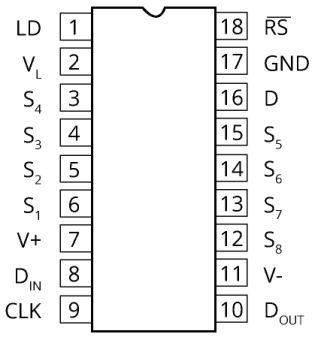
Built on the high voltage silicon gate process the DG485 has a wide 44 V range. An epitaxial layer prevents latchup.

Each channel conducts equally well in either direction when ON and blocks up to 30 volts peak-to-peak when OFF.

Packaging for the DG485 consists of the 18-pin CerDIP, plastic DIP and 20-pin PLCC for surface mount. Temperature ranges available are military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C).

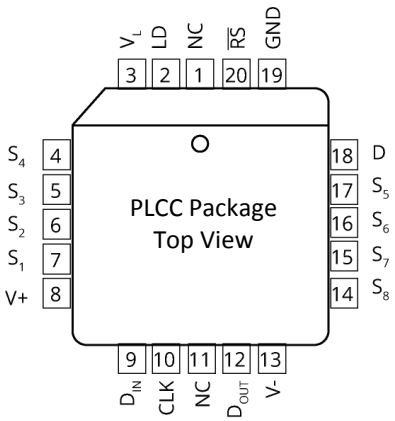
PIN CONFIGURATIONS

Dual-In-Line Package



Top View

Order Numbers:
CerDIP : DG485AK, DG485AK/883
Plastic : DG485DJ



Order Number:
DG485DN

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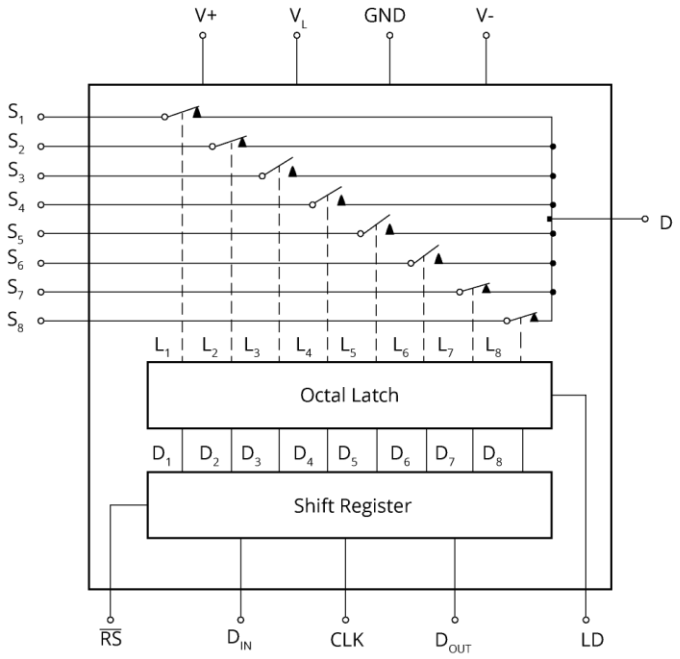
FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLES



$\overline{RS}$	CLK	D_{IN}	D_1	D_N
1	↑	0	0	D_{N-1}
1	↑	1	1	D_{N-1}
1	↓	X	D_1	D_N (No Change)
0	X	X	0	0

The CLK Input is edge triggered

LD	D_N	L_N	SW_N
↑	0	0	OFF
↑	1	1	ON
↓	D_n	L_n	(No Change)

The LD Input is level triggered

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[1] V_S, V_D ..... (V-) -2 V to (V+) +2 V
Or 30 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle) ..... 100 mA
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
18-Pin CerDIP** ..... 600 mW
18-Pin Plastic DIP*** ..... 470 mW
20-Pin PLCC**** 450mW

* All leads welded or soldered to PC Board
** Derate 9.2 mW/°C above 75°C
*** Derate 16.5 mW/°C above 25°C
**** Derate 6mW/°C above 75°C

[1] Signals on Sx, Dx, or INx exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2,4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[c]	V_{ANALOG}		Full		-15	15	-15	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V+ = 13.5 V, V- = -13.5 V I_S = -5 mA, V_D = ±10 V	Room Full	55		85 125		85 125	Ω
Delta Drain-Source ON-Resistance	$\Delta r_{DS(ON)}$	For each VD : $\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)AVG}}$	Room	6		10		10	%

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ANALOG SWITCH (Cont'd)									
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5 V, V- = -16.5 V	Room Hot	0.01	-1 -20	1 20	-1 -20	1 20	nA
	$I_{D(OFF)}$	V_D = -15.6 V, V_S = 15.5 V V_D = 15.5 V, V_S = -15.5 V	Room Hot	0.1	-10 -200	10 200	-10 -200	10 200	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V± = ±16.5 V V_S = V_D = ±15.5 V One Switch At A Time	Room Hot	0.11	-20 -500	20 500	-20 -500	20 500	
		V± = ±16.5 V V_S = V_D = ±15.5 V All Switches ON	Room	0.20					
INPUT									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V All Other = 2.4 V	Room Hot	-0.00001	-1 -5	1 5	-1 -5	1 5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 2.4 V All Other = 0.8 V	Room Hot	0.00001	-1 -5	1 5	-1 -5	1 5	
SERIAL DATA OUTPUT									
Output Voltage with V_{IN} Low – D_{OUT}	V_{OL}	I_O = 1.6 mA, V+ = 4.5 V	Full	0.25		0.4		0.4	V
Output Voltage with V_{IN} High - D_{OUT}	V_{OH}	I_O = -80 µA, V+ = 16.5 V V_L = 4.75 V	Full	4.4	2.7		2.7		
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	See Figure 1 V_S = ±10 V	Room Hot	170		200 275		200 275	ns
Turn-OFF Time	t_{OFF}	See Figure 1 V_S = ±10 V	Room Hot	150		200 275		200 276	
Data Setup Time	t_{DS}	See Figure 1	Room Hot		40 60		40 60		
Data Hold Time	t_{DH}		Room Hot		40 60		40 60		
LOAD Hold Time	t_{LH}	See Figure 1	Room Hot		100 150		100 150		
RESET Hold Time	t_{RM}		Room Hot		100 150		100 150		
RESET ↑ to CLOCK ↑ Delay	t_{DRO}		Room Hot		40 60		40 60		
Charge Injection	Q	Any One Channel V_S = 0 V, C_L = 1.000 pF	Room	17					pC
OFF Isolation[c]		R_L = 50 Ω, C_L = 5 pF f = 1 MHz, See Figure 2	Room	-75					dB

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DYNAMIC CHARACTERISTICS									
Source OFF Capacitance[c]	$C_{S(OFF)}$	Vgen = 0 V, Rgen = 0 Ω f = 1 MHz	Room	7					pF
Drain OFF Capacitance[c]	$C_{D(OFF)}$		Room	43					
On-State Capacitance[c]	$C_{S+D\ (ON)}$	Vgen = 0 V, Rgen = 0 Ω f = 1 MHz, One Channel ON	Room	53					
		Vgen = 0 V, Rgen = 0 Ω f = 1 MHz, All Channels ON	Room	122					
POWER SUPPLIES									
Positive Supply Current	I+	V+ = 16.5 V, V- = -16.5 V V_{IN} = 0 or 5 V V_L = 5.25 V D_{OUT} Open	Room Full	0.001		3 10		3 10	µA
Negative Supply Current	I-		Room Full	-0.001	-3 -10		-3 -10		
Logic Supply Current	I_L		Room Full	0.001		3 10		3 10	
Ground Current	I_{GND}		Room Full	-0.001	-3 -10		-3 -10		

NOTES :

a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. VIN = Input voltage to perform proper function.
f. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

TEST CIRCUITS

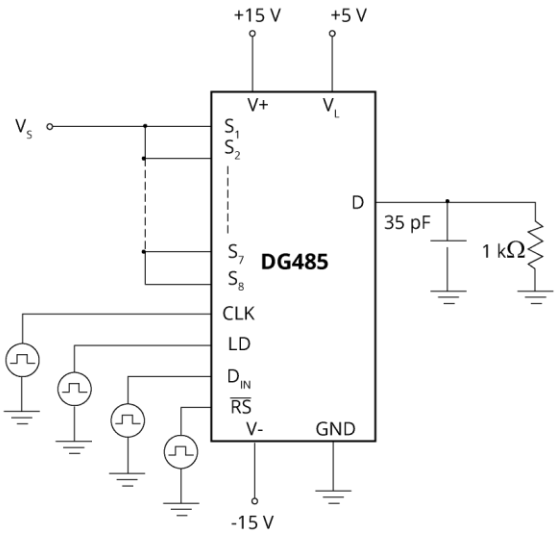

Figure 1. Switching Time Test Circuit

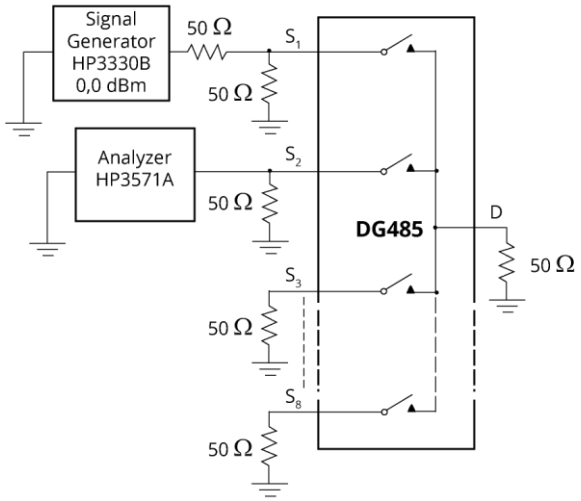

Figure 2. Adjacent Input Crosstalk

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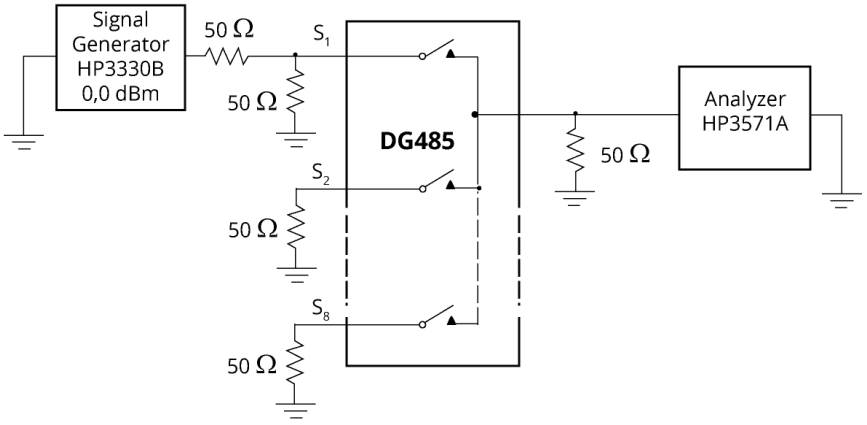
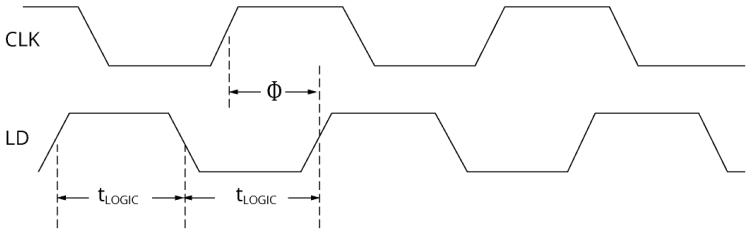


Figure 3. Off Isolation

APPLICATIONS



Φ = for CLK and LD inputs of the same frequency. The recommended phase delay of LD from CLK is ½ t_{LOGIC} to t_{LOGIC}.

$t_{LOGIC\ (MIN)}$: 80 ns at 25°C V+ = 15 V
150 ns at 125°C V- = -15 V
GND = 0 V

Figure 4.

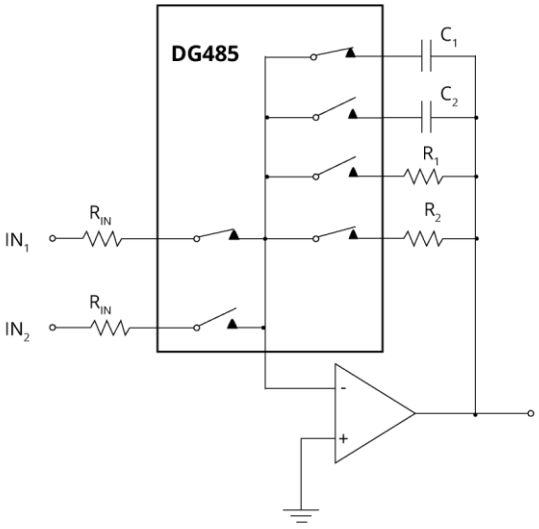


Figure 5. Multi-Function circuit Provides Input Selection, Gain Ranging and Filtering with One DG485

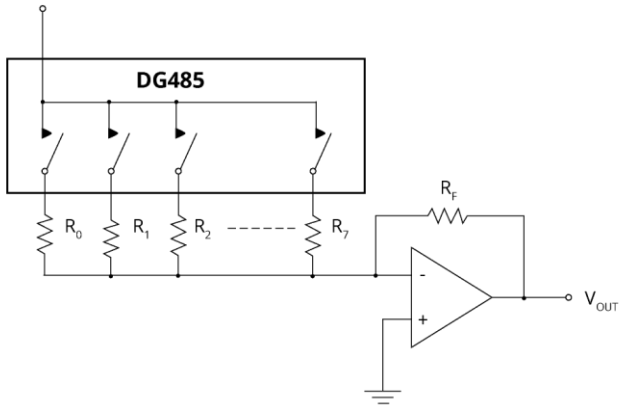


Figure 6. Non-Linear DAC Circuit

APPLICATIONS (Cont'd)

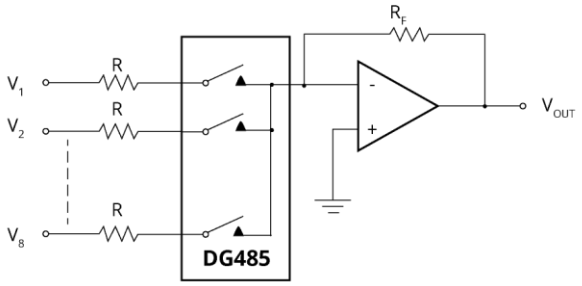


Figure 7. Summing Node Mixer

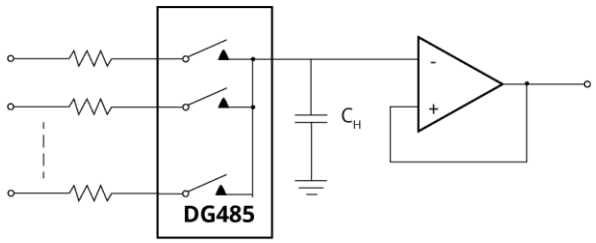


Figure 8. Multi-Channel Sampling and TDM application

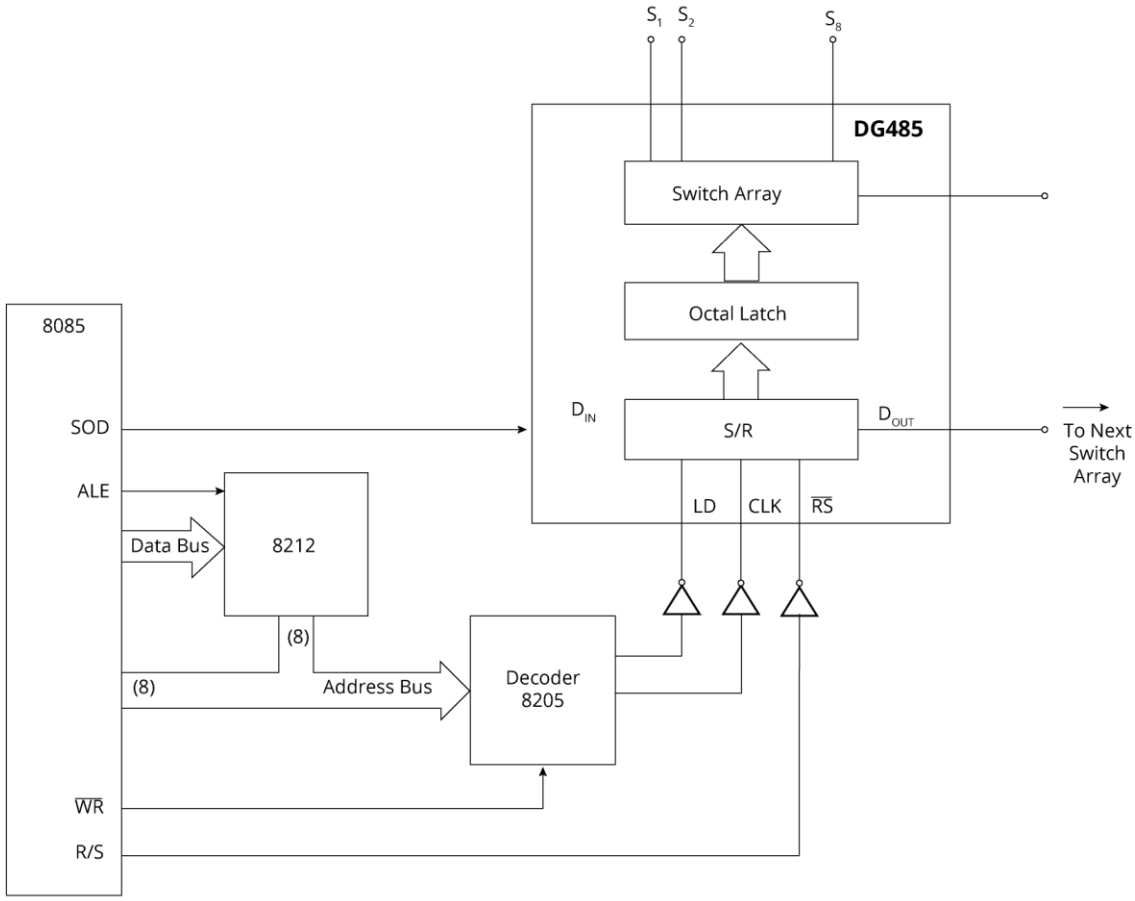


Figure 9. Direct Serial Interface (8085)

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