1 PRODUCT OVERVIEW

SAM8 PRODUCT FAMILY

Samsung's SAM87 family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

— Efficient register-oriented architecture

— Selectable CPU clock sources

— Idle and Stop power-down mode release by interrupt

— Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum of six CPU clocks) can be assigned to specific interrupt levels.

S3C8075/P8075 MICROCONTROLLERS

S3C8075/P8075 single-chip 8-bit microcontrollers are based on the powerful SAM87 CPU architecture. The internal register file is logically expanded to increase the on-chip register space. The S3C8075 has 16-Kbyte mask-programmable ROM. The S3P8075 has 16-Kbyte one-time-programmable EPROM.

Following Samsung's modular design approach, the following peripherals are integrated with the SAM87 core:

— Seven programmable I/O ports (total 56 pins)

— One 8-bit basic timer for oscillation stabilization and watchdog functions

— One synchronous operating mode and three full-duplex asynchronous UART modes

— Two 8-bit timers with interval timer and PWM modes

— Two 16-bit general-purpose timer/counters

OTP

The S3C8075 microcontroller is also available in OTP (One Time Programmable) version, S3P8075. S3P8075 microcontroller has an on-chip 16-Kbyte one-time-programmable EPROM instead of masked ROM. The S3P8075 is comparable to S3C8075, both in function and in pin configuration.

FEATURES

CPU

- SAM87 CPU core

Memory

- 272-byte general purpose register area
- 16-Kbyte internal program memory
- ROM-less operating mode

External Interface

- 64-Kbyte external data memory area
- 64-Kbyte external program memory area (ROM-less mode)

Instruction Set

- 78instructions
- IDLE and STOP instructions for power-down mode

Instruction Execution Time

- 500 ns at 12 MHz f_{CPU} (Min.)

Interrupts

- 17 interrupt sources
- 17 interrupt vectors
- Eight interrupt levels
- Fast interrupt processing

General I/O

- Four nibble-programmable ports
- One bit-programmable port
- Two bit-programmable ports for external interrupts

Timers

- Two 8-bit timers with interval timer and PWM modes

Timer/Counters

- Two 16-bit general-purpose timer/counters

Basic Timer

- One 8-bit basic timer (BT) for oscillation stabilization control and watch dog timer function.

Serial Port

- One synchronous operating mode and three full-duplex asynchronous UART modes

Operating Temperature Range

- $-40^{\circ}C$ to $+85^{\circ}C$

Operating Voltage Range

- 2.7 V to 5.5 V

Package Types

- 64-pin SDIP, 64-pin QFP

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Table 1-1. Comparison Table

Feature	S3C80B5	S3C8075
Core	SAM8	SAM87
ROM	16 K bytes	Same
RAM	272 bytes	Same
I/O	54	56 (add two pins)
Port 6	Open drain (9 V drive)	Normal C-MOS output
I/O option	None	Same
Timer	8-bit back-up timer	None
	Timer A, B — 8-bit — Interval/PWM mode — Timer A match interrupt	Same (some differ in interval mode, see manual)
	Timer C, D — Gate function — Timer/counter	Same
Watchdog timer	None	Watchdog timer (with BT)
SIO	UART — 8-bit/9-bit UART — SIO	Same
Interrupt	External × 12 — P2.4–P2.7, P4.0–P4.7	Same
	Internal × 6 — Timer A, C, D, SI, SO, Back-up	Internal × 5 — Timer A, C, D, SI, SO
Power down	Stop/idle	Same
Oscillator	Crystal, ceramic	Same
CPU clock divider	1/2	1/1, 1/2, 1/8, 1/16
Execution time (Min.)	0.6 μs at 20 MHz (f_{CPU} = 10 MHz)	0.5 μs at 12 MHz (f_{CPU} = 12 MHz)
Operating frequency	Max. 20 MHz (f_{CPU} = 10 MHz)	Max. 12 MHz (at 4.5 V) [2] Max. 4 MHz (at 2.7 V)
Operating voltage	4.5–5.5 V	2.7–5.5 V at 4 MHz 4.5–5.5 V at 12 MHz
OTP/MTP	MTP	OTP
Pin assignment	–	Different
Package	64SDIP/64QFP	Same
Start address	0020h	0100h
P5CON, P6CON	BANK0	BANK1
Interrupt pending bit clear	Write "1"	Write "0"

NOTES:

1. The S3C8075 can replace the S3C80B5. Their functions are mostly the same, but there are some differences. Table 1-1 shows the comparison of S3C8075 and S3C80B5.
2. Operating frequency is maximum CPU clock; the maximum oscillation frequency is 22.1184 MHz.
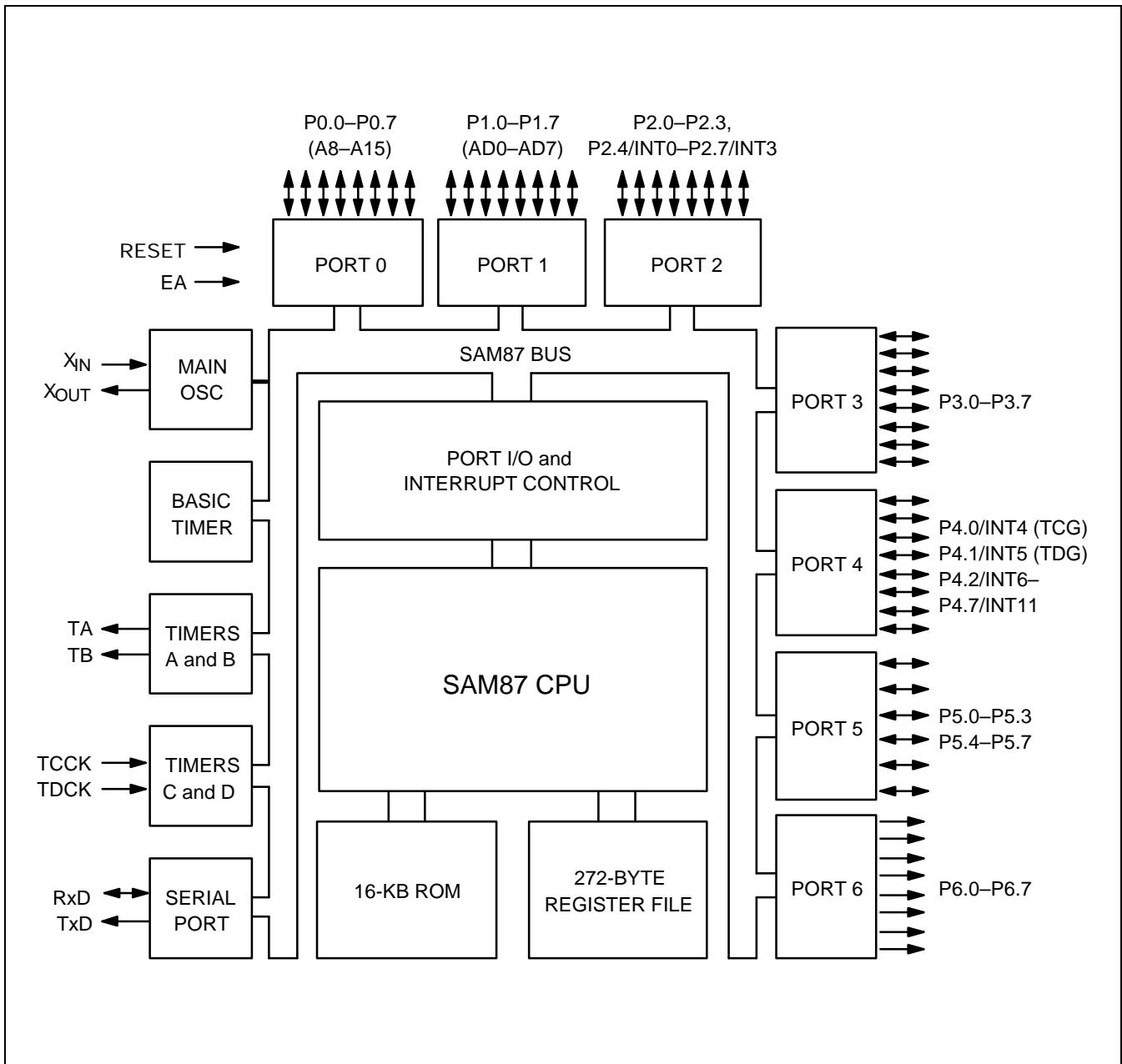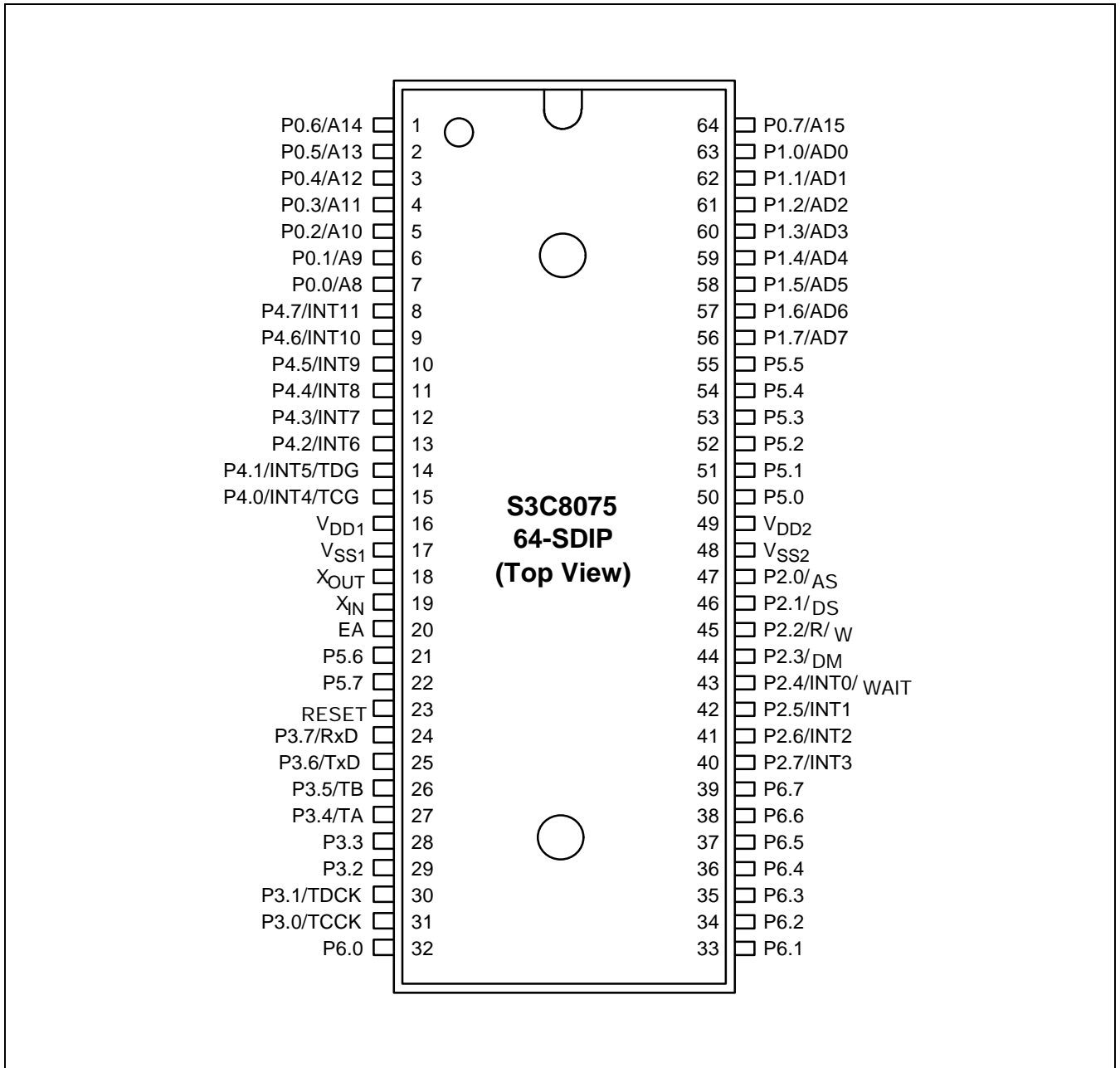
BLOCK DIAGRAM

Figure 1-1. S3C8075 Block Diagram

P0.6/A14	1	64	P0.7/A15
P0.5/A13	2	63	P1.0/AD0
P0.4/A12	3	62	P1.1/AD1
P0.3/A11	4	61	P1.2/AD2
P0.2/A10	5	60	P1.3/AD3
P0.1/A9	6	59	P1.4/AD4
P0.0/A8	7	58	P1.5/AD5
P4.7/INT11	8	57	P1.6/AD6
P4.6/INT10	9	56	P1.7/AD7
P4.5/INT9	10	55	P5.5
P4.4/INT8	11	54	P5.4
P4.3/INT7	12	53	P5.3
P4.2/INT6	13	52	P5.2
P4.1/INT5/TDG	14	51	P5.1
P4.0/INT4/TCG	15	50	P5.0
V_{DD1}	16	49	V_{DD2}
V_{SS1}	17	48	V_{SS2}
X_{OUT}	18	47	P2.0/$_{AS}$
X_{IN}	19	46	P2.1/$_{DS}$
EA	20	45	P2.2/R/$_W$
P5.6	21	44	P2.3/$_{DM}$
P5.7	22	43	P2.4/INT0/$_{WAIT}$
RESET	23	42	P2.5/INT1
P3.7/RxD	24	41	P2.6/INT2
P3.6/TxD	25	40	P2.7/INT3
P3.5/TB	26	39	P6.7
P3.4/TA	27	38	P6.6
P3.3	28	37	P6.5
P3.2	29	36	P6.4
P3.1/TDCK	30	35	P6.3
P3.0/TCCK	31	34	P6.2
P6.0	32	33	P6.1

**S3C8075
64-SDIP
(Top View)**

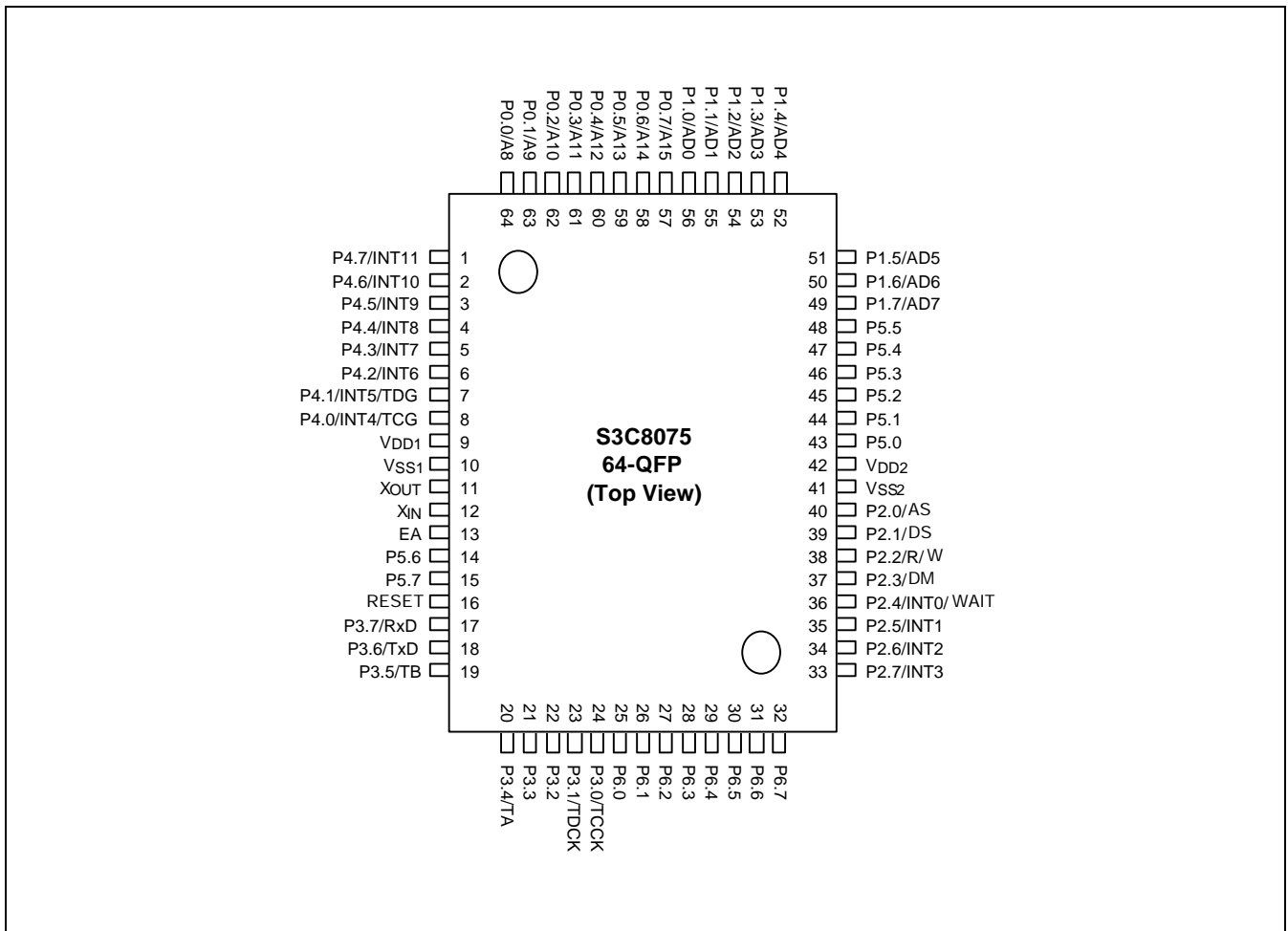**Figure 1-2. S3C8075 Pin Assignments (64-SDIP)**

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Figure 1-3. S3C8075 Pin Assignments (64-QFP)

Table 1-2. S3C8075 Pin Descriptions (64-SDIP)

Pin Name	Pin Type	Pin Description	Circuit Number	SDIP Pin Number	Share Pins
P0.0–P0.7	I/O	I/O port with nibble-programmable pins; Input or push-pull, open-drain output and software assignable pull-ups; also configurable as external interface address lines A8-A15.	E	1–7, 64	A8–A15
P1.0–P1.7	I/O	Same general characteristics as port 0; also configurable as external interface address/data lines AD0–AD7.	E	56–63	AD0–AD7
P2.0–P2.3 P2.4–P2.7	I/O	I/O port with bit-programmable pins; Input or push-pull output. Lower nibble pins 0–3 are configurable for external interface signals; upper nibble pins 4–7 are bit-programmable for external interrupts INT0–INT3. P2.4 can also be used for external WAIT input.	D-1 (lower nibble); D-1 (upper nibble; with noise filter)	40–47	AS, DS, DM, R/W INT0–INT3, WAIT
P3.0–P3.7	I/O	I/O port with bit-programmable pins; Input or push-pull output. Alternate functions include software-selectable UART transmit and receive on pins 3.7 and 3.6, timer B and timer A outputs at pins 3.5 and 3.4, and timer D and C clock inputs at pins 3.1 and 3.0.	D-1	24– 31	TCCK, TDCK, TA, TB, TxD, RxD
P4.0–P4.7	I/O	I/O port with bit-programmable pins; Input or push-pull output; software-assignable pull-ups. Alternate functions include external interrupt inputs INT4-INT11 (with interrupt enable and pending control) and timer C and D gate input at P4.0 and P4.1.	D (with noise filter)	8–15	INT4–INT11, TCG, TDG
P5.0–P5.7	I/O	I/O port with nibble-programmable pins; Input or push-pull, open-drain output; software-assignable pull-ups.	E	21, 22, 50–55	–
P6.0–P6.7	O	Output port with nibble-programmable pins; push-pull, open-drain output; software-assignable pull-ups.	E-8	32–39	–
RxD	I/O	Bi-directional serial data input pin	–	24	P3.7
TxD	I/O	Serial data output pin	–	25	P3.6
TA, TB	I/O	Timer A and B output pins	4	27, 26	P3.4, P3.5
TCCK, TDCK	I/O	Timer C and D external clock input pins	D-1	30, 31	P3.0, P3.1
INT0–INT3	I/O	External interrupts. I/O pin 2.4 (share pin with INT0) is also configurable as a WAIT signal input pin for the external interface.	D-1 (with noise filter)	40–43	P2.4–P2.7

Table 1-2. S3C8075 Pin Descriptions (Continued)

Pin Name	Pin Type	Pin Description	Circuit Number	SDIP Pin Number	Share Pins
INT4–INT11	I/O	Bit-programmable external interrupt input pins with interrupt pending and enable /disable control	D (with noise filter)	8–15	P4.0–P4.7
X_{IN}, X_{OUT}	–	System clock input and output pins	–	18, 19	–
RESET	I	System reset pin (internal pull-up: 280 KΩ)	B	23	–
EA	I	External access (EA) pin with three modes: 0 V: Normal operation (internal ROM) 5 V: ROM-less operation (external interface)	–	20	–
V_{DD2}, V_{SS2}	–	Power input pins for port output (external)	–	49, 48	–
V_{DD1}, V_{SS1}	–	Power input pins for CPU (internal)	–	16, 17	–

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PIN CIRCUIT

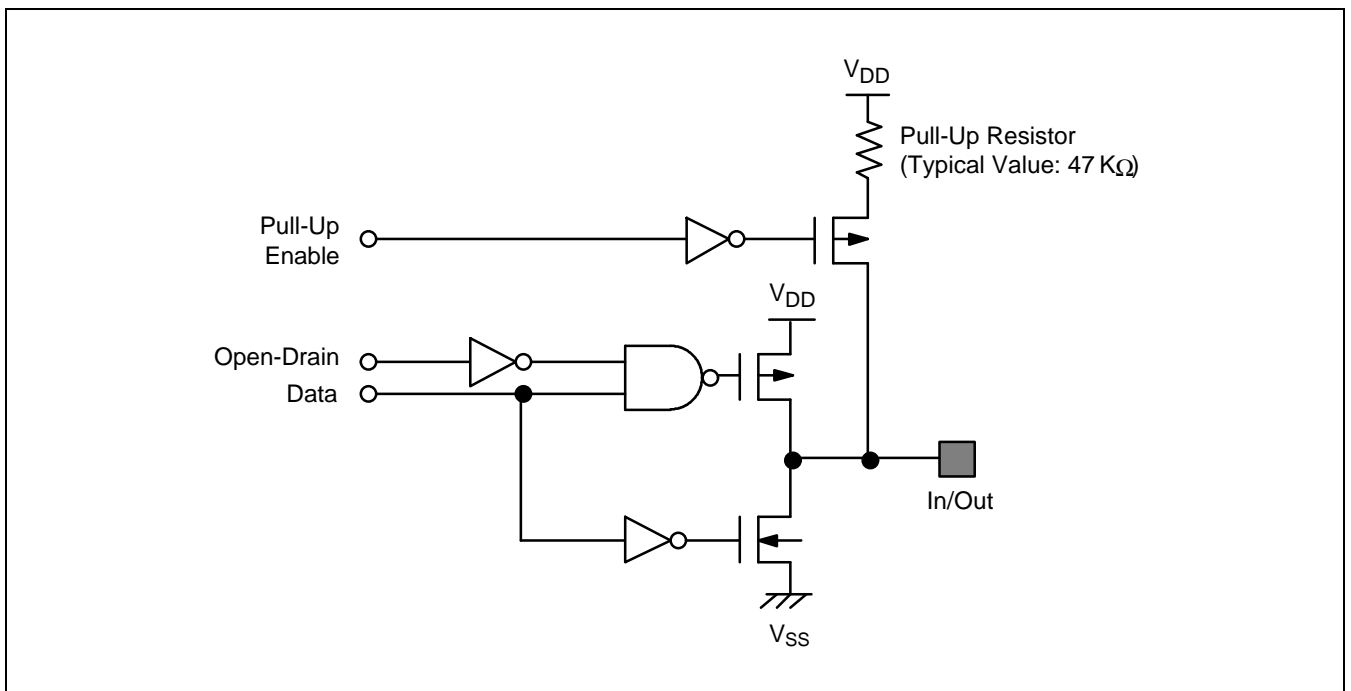**Figure 1-4. Pin Circuit Type E (Ports 0, 1, 5)**

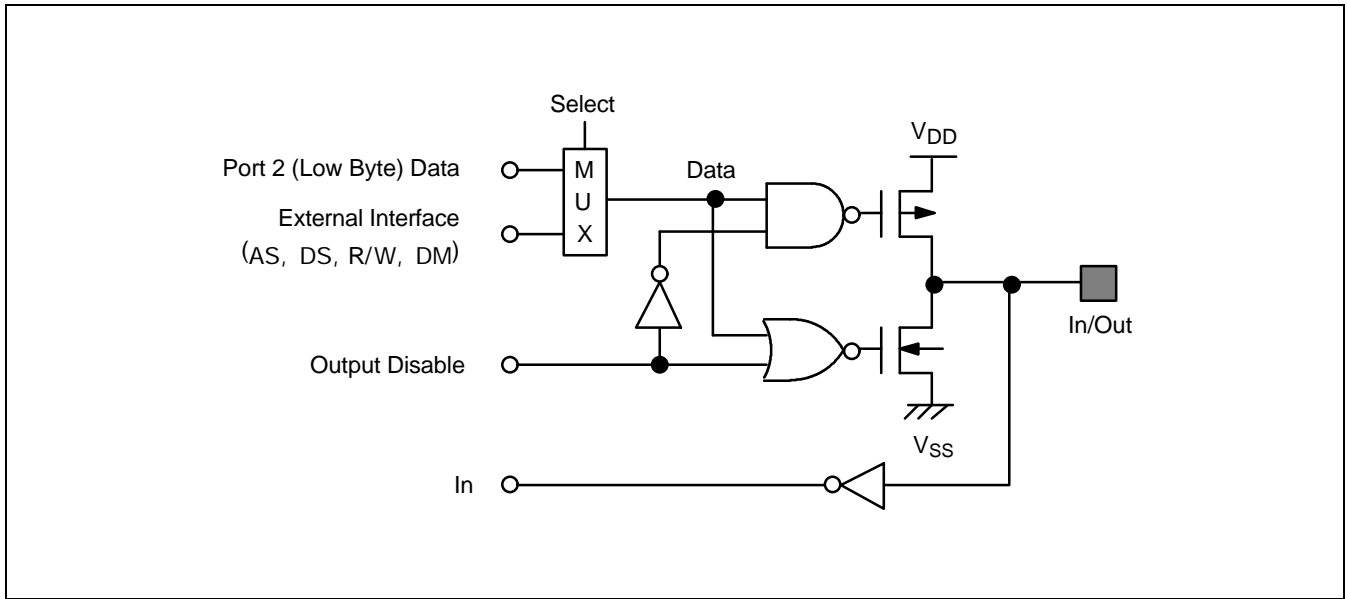**Figure 1-5. Pin Circuit Type E-8 (Ports 6)**

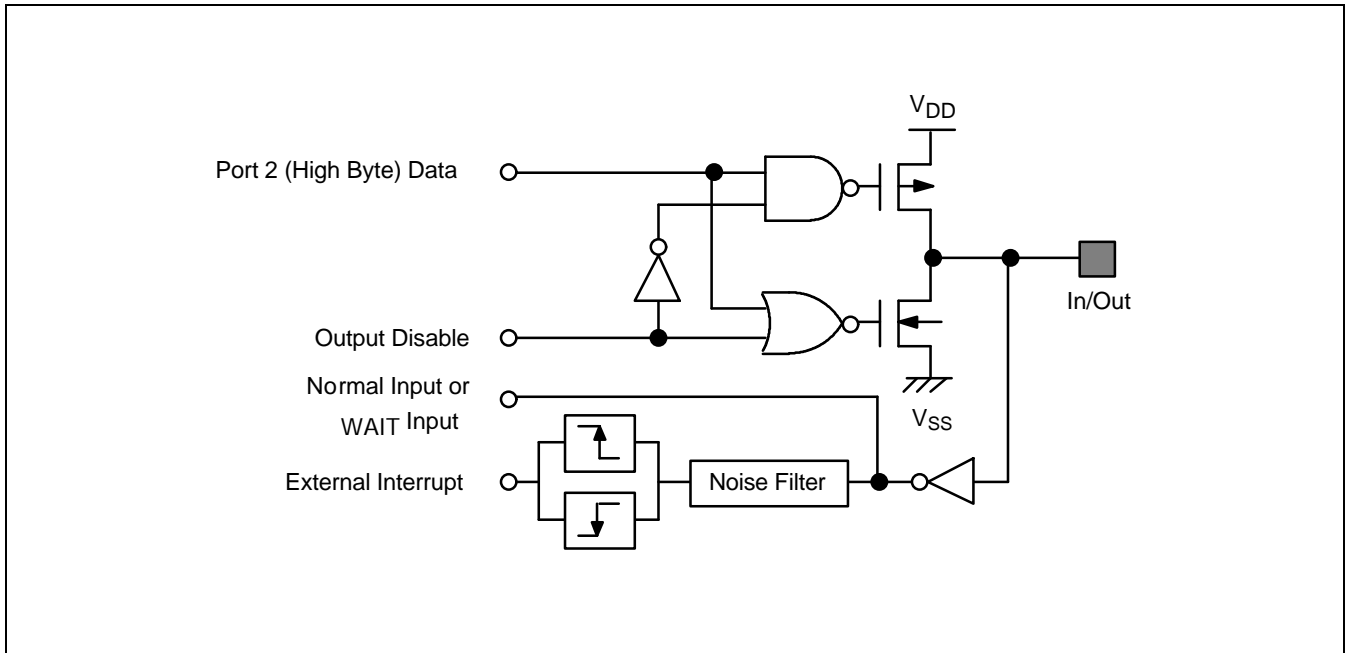**Figure 1-6. Pin Circuit Type D-1 (P2.0–P2.3)**
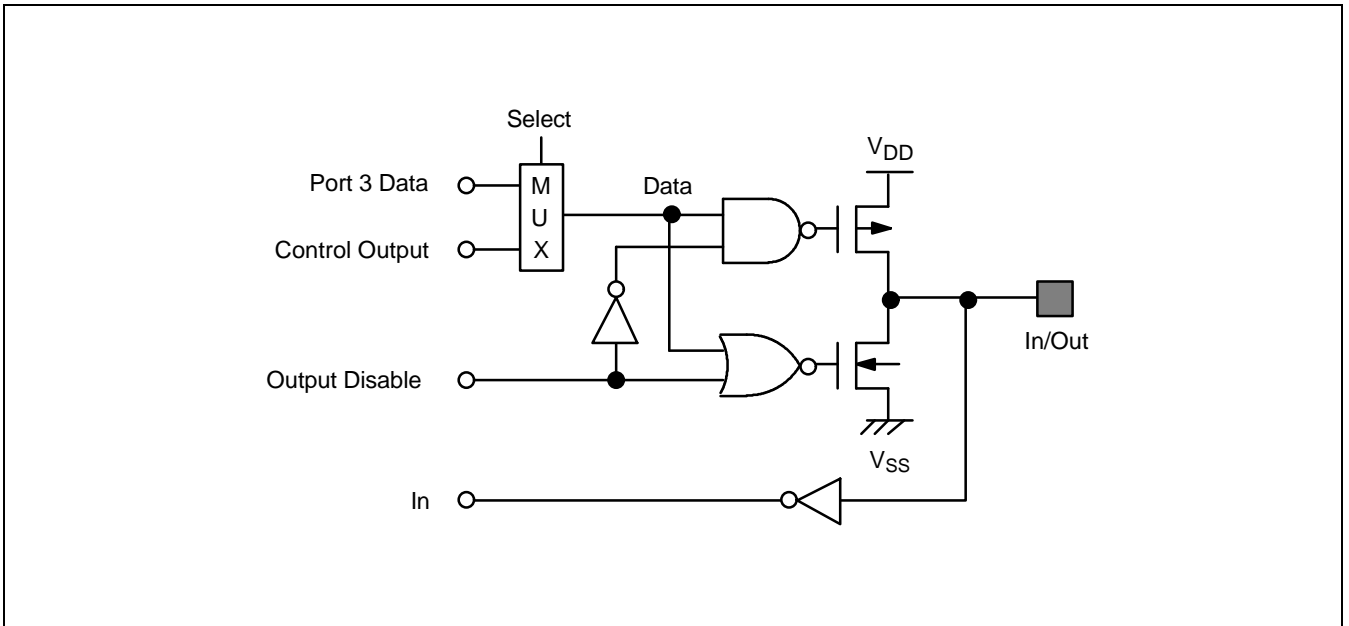

Figure 1-7. Pin Circuit Type D-1 (P2.4–P2.7)

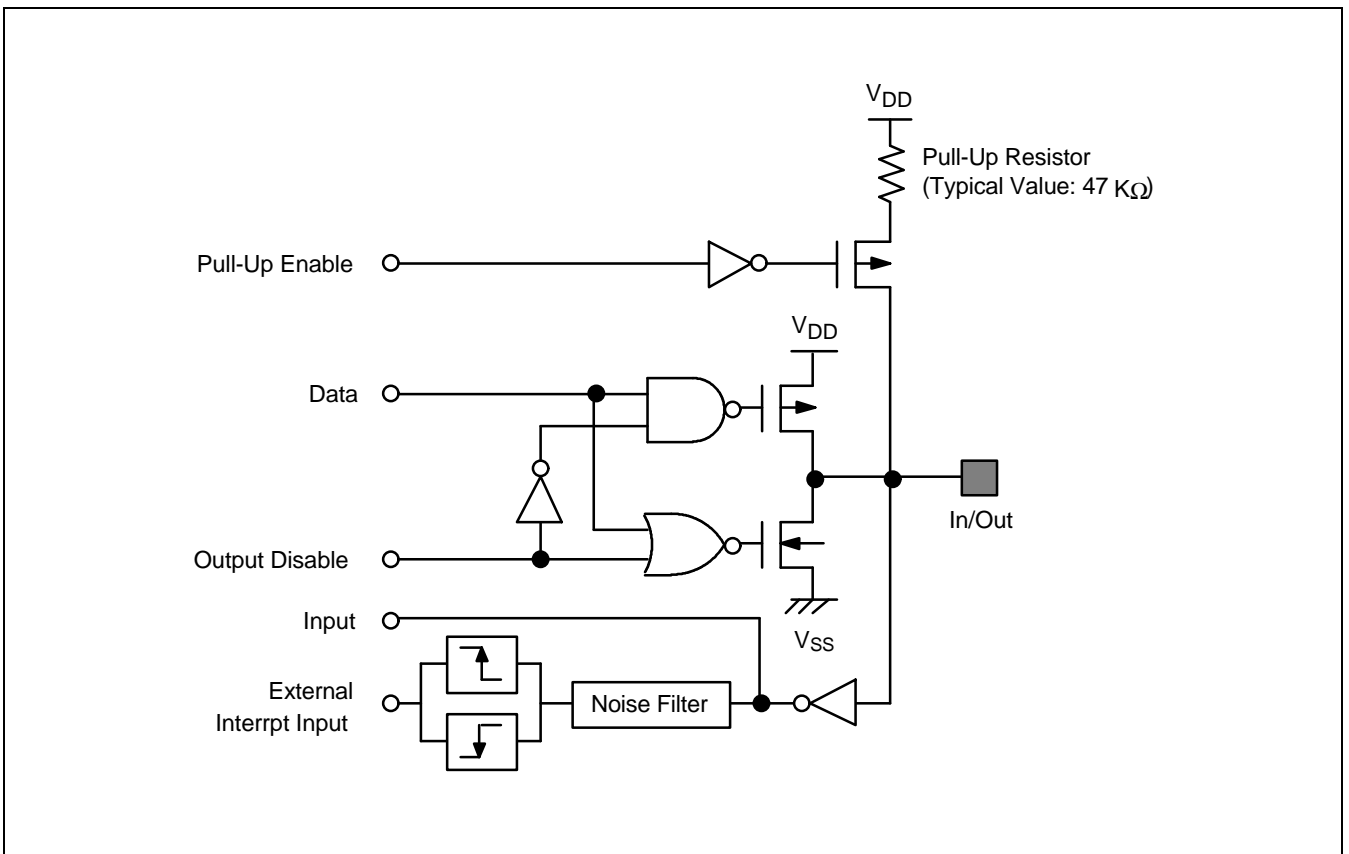**Figure 1-8. Pin Circuit Type D-1 (Port 3)**
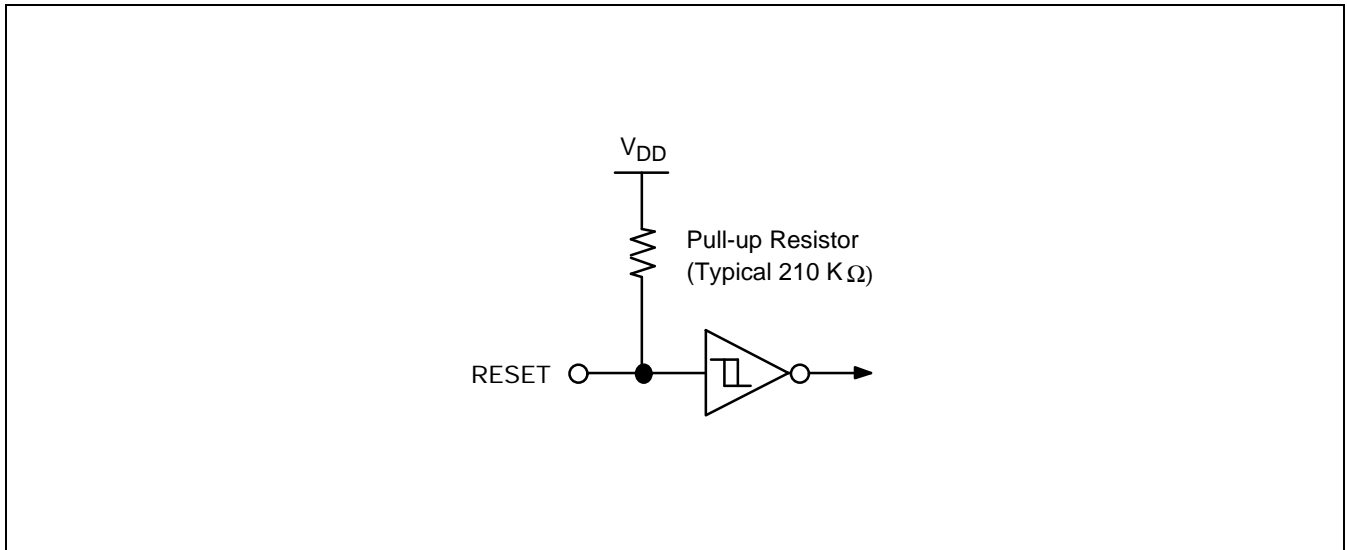

Figure 1-9. Pin Circuit Type D (Port 4)

Figure 1-10. Pin Circuit Type B (RESET**)**

14 ELECTRICAL DATA

OVERVIEW

In this section, S3C8075 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings

— D.C. electrical characteristics

— I/O capacitance

— A.C. electrical characteristics

— Oscillation characteristics

— Oscillation stabilization time

Table 14-1. Absolute Maximum Ratings

$(T_A = 25 °C)$

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		-0.3 to $+6.5$	V
Input voltage	V_I	All ports (in input mode)	-0.3 to $V_{DD} + 0.3$	
Output voltage	V_O	All ports (in output mode)	-0.3 to $V_{DD} + 0.3$	V
Output current high	I_{OH}	One I/O pin active	-10	mA
		All I/O pins active	-60	
Output current low	I_{OL}	One I/O pin active	$+30$	mA
		Total pin current for ports 0–4	$+100$	
		Total pin current for ports 5 and 6	$+100$	
Operating temperature	T_A		-40 to $+85$	$°C$
Storage temperature	T_{STG}		-65 to $+150$	$°C$

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Table 14-2. D.C. Electrical Characteristics

$(T_A = -40 °C$ to $+85 °C$, $V_{DD} = 2.7$ V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	V_{IH1}	All input pins except V_{IH2}	$0.8\ V_{DD}$	–	V_{DD}	V
	V_{IH2}	X_{IN}	$V_{DD} - 0.5$			
Input low voltage	V_{IL1}	All input pins except V_{IL2}	–	–	$0.2\ V_{DD}$	V
	V_{IL2}	X_{IN}			0.4	
Output high voltage	V_{OH1}	$V_{DD} = 4.5$ V to 5.5 V $I_{OH} = -4$ mA Port 5, 6	$V_{DD} - 1.0$	–	–	V
	V_{OH2}	$V_{DD} = 4.5$ V to 5.5 V $I_{OH} = -1$ mA All output pins except port 5, 6				
Output low voltage	V_{OL1}	$V_{DD} = 4.5$ V to 5.5 V $I_{OL} = 15$ mA Ports 5 and 6	–	–	1.0	V
	V_{OL2}	$I_{OL} = 2$ mA Ports 0–4			0.4	
Input high leakage current	I_{LIH1}	$V_{IN} = V_{DD}$ All input pins except X_{IN}, X_{OUT}	–	–	3	μA
	I_{LIH2}	$V_{IN} = V_{DD}$, X_{IN}, X_{OUT}			20	
Input low leakage current	I_{LIL1}	$V_{IN} = 0$ V All input pins except X_{IN}, X_{OUT}	–	–	-3	μA
	I_{LIL2}	$V_{IN} = 0$ V, X_{IN}, X_{OUT}			-20	
Output high leakage current	I_{LOH}	$V_{OUT} = V_{DD}$ All output pins	–	–	5	μA
Output low leakage current	I_{LOL}	$V_{OUT} = 0$ V	–	–	-5	μA
Pull-up resistor	R_{L1}	$V_{IN} = 0$ V; $V_{DD} = 5$ V Ports 0, 1, 4, 5 and 6	30	47	70	KΩ
	R_{L2}	$V_{IN} = 0$ V; $V_{DD} = 5$ V RESET only	110	210	310	

Table 14-2. D.C. Electrical Characteristics (Continued)

(T_A = $-40\,^{\circ}$C to $+85\,^{\circ}$C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current [1]	I_{DD1} [2]	V_{DD} = 5 V ± 10 % 12-MHz oscillation	–	12	25	mA
		4-MHz oscillation		4.5	10	
		V_{DD} = 3 V ± 10 % 12-MHz oscillation		6	15	
		4-MHz oscillation		2.5	7	
	I_{DD2} [2]	Idle mode; V_{DD} = 5 V ± 10 % 12-MHz oscillation		3	10	
		4-MHz oscillation		1.5	4	
		Idle mode; V_{DD} = 3 V ± 10 % 12-MHz oscillation		1.2	3	
		4-MHz oscillation		0.6	1.5	
	I_{DD3}	Stop mode: V_{DD} = 5 V ± 10 %		0.1	3	µA

NOTES:
1. Supply current does not include current drawn through internal pull-up resistors or external output current loads.
2. At supply current, the CPU clock frequency is same with oscillation frequency (CPU use non divided clock).

Table 14-3. Data Retention Supply Voltage in Stop Mode

(T_A = $-40\,^{\circ}$C to $+85\,^{\circ}$C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	Stop mode	2	–	6	V
Data retention supply current	I_{DDDR}	Stop mode, V_{DDDR} = 2.0 V	–	–	3	µA

NOTES:
1. During the oscillator stabilization wait time (t_{WAIT}), all CPU operations must be stopped.
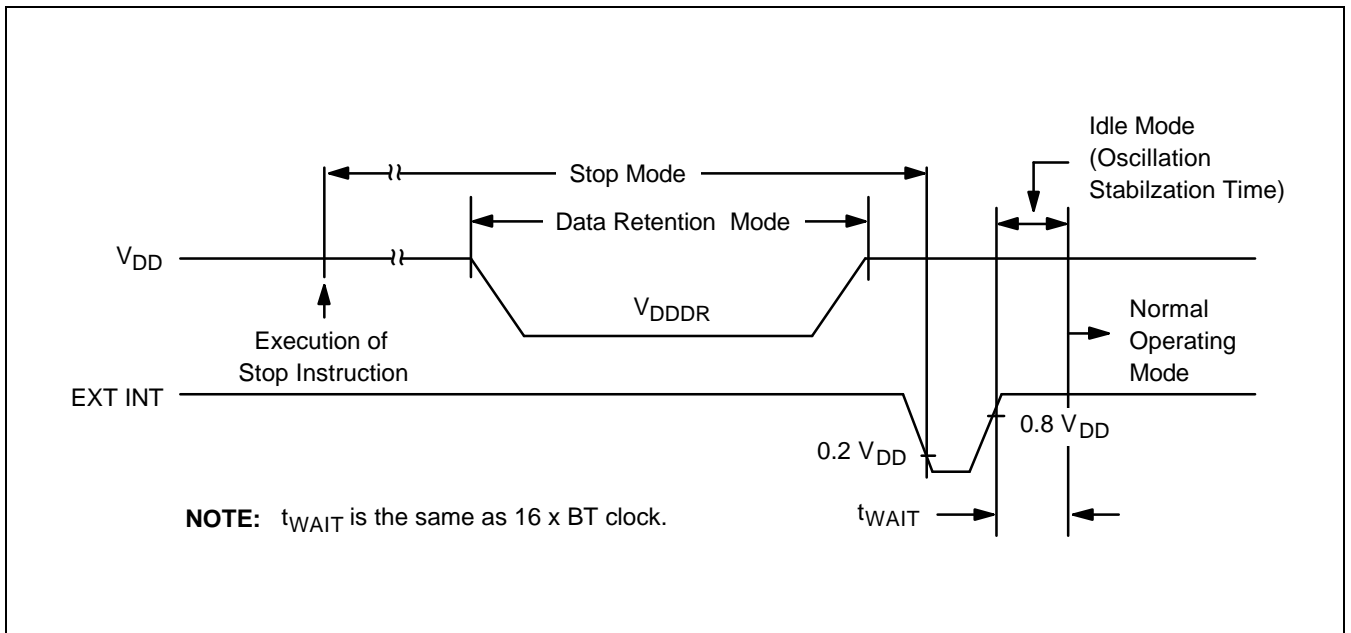2. Supply current does not include drawn through internal pull–up resistors and external output current loads.

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Figure 14-1. Stop Mode Release Timing When Initiated by an External Interrupt
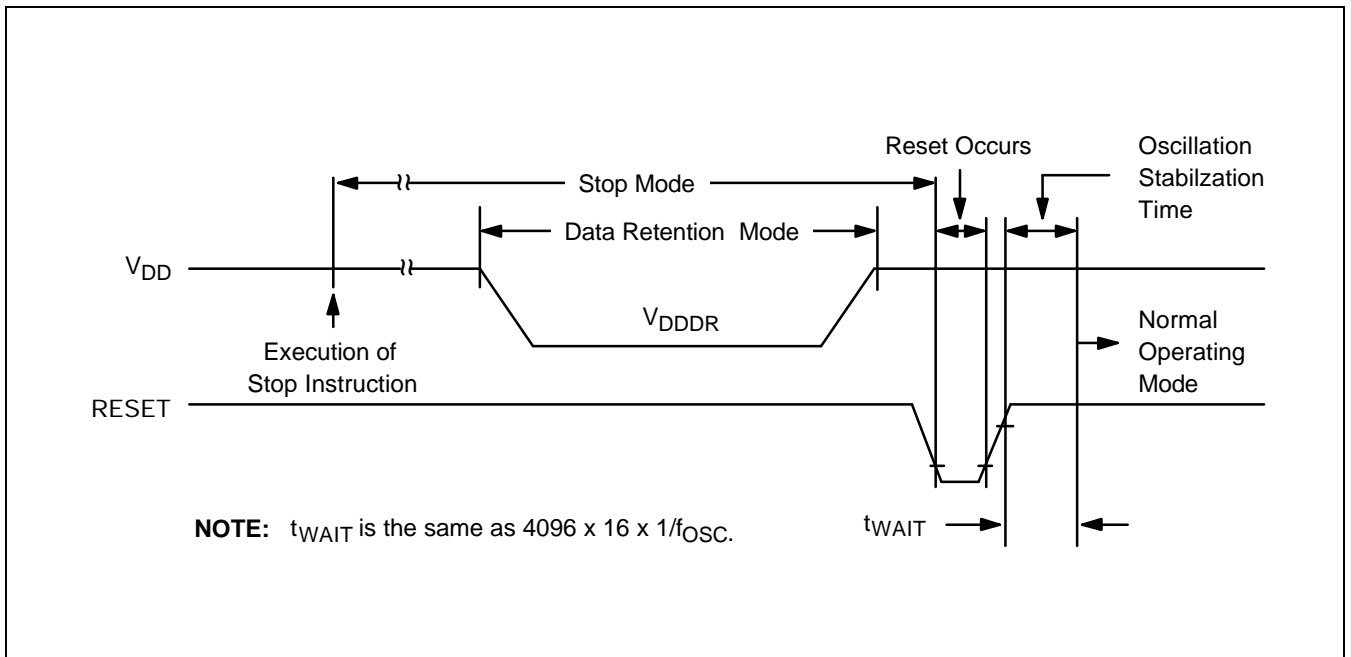

Figure 14-2. Stop Mode Release Timing When Initiated by a Reset

Table 14-4. Input/output Capacitance

(T_A = − 40 °C to + 85 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are connected to V_{SS}	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 14-5. A.C. Electrical Characteristics

(T_A = − 40 °C to + 85 °C, V_{DD} = 2.7 V to 5.5 V)

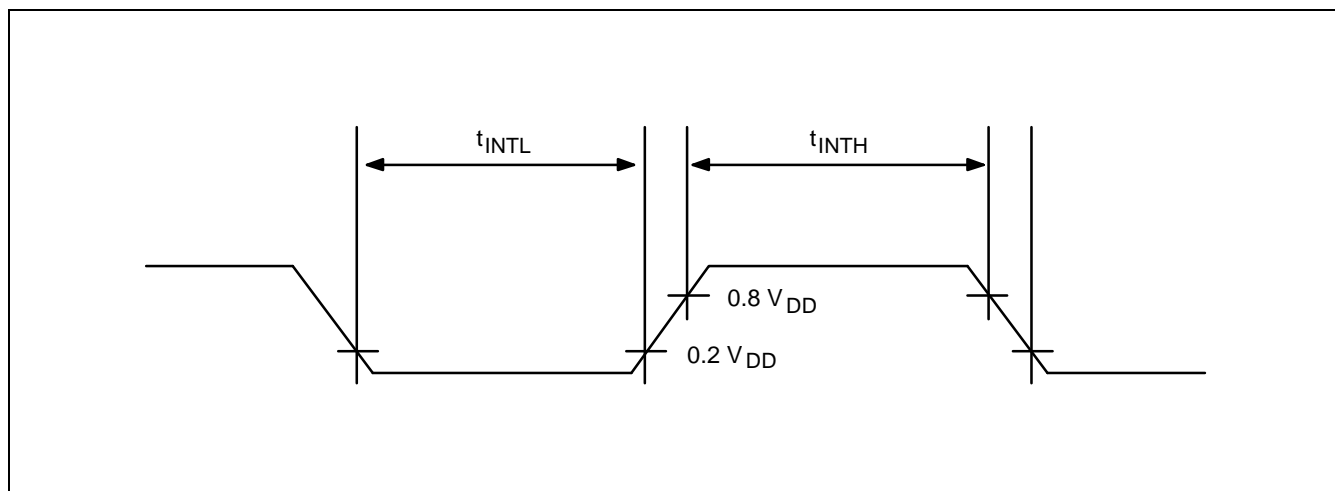| Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input high, low width	t_{INTH}, t_{INTL}	P2.4–P2.7	100	–	–	ns
		P4.0–P4.7	100			
RESET input low width	t_{RSL}	Input	10	–	–	µs

NOTE: User must keep the larger value with the min value.

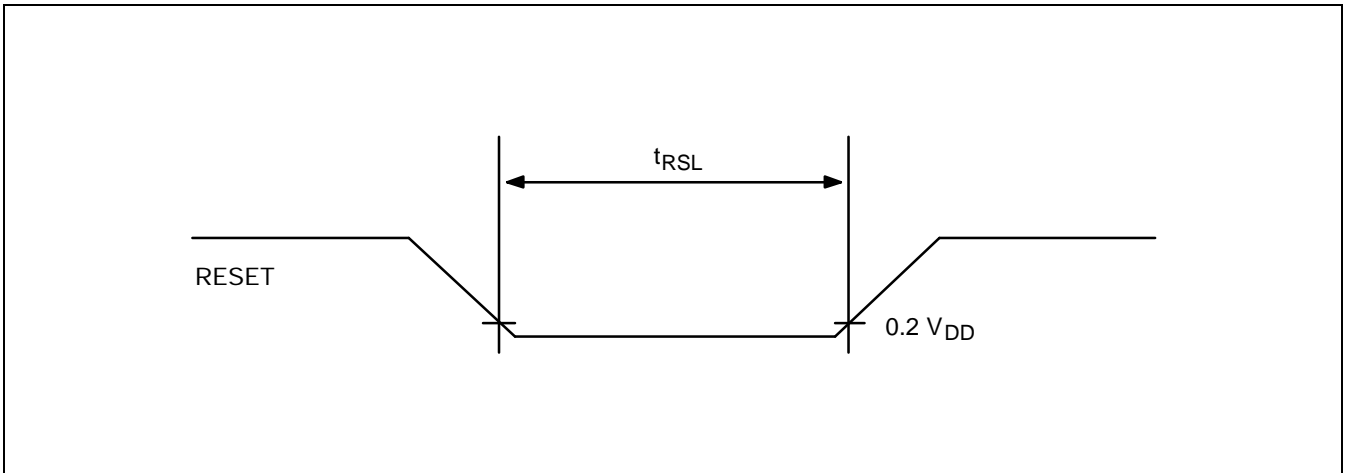**Figure 14-3. Input Timing for External Interrupts (Port 2 and 4)**

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Figure 14-4. Input Timing for RESET

Table 14-6. Oscillation Characteristics

$(T_A = -20\,°C + 85\,°C, V_{DD} = 4.5\ V\ to\ 5.5\ V)$

Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Crystal		Oscillation frequency	1	–	22.1184	MHz
Ceramic		Oscillation frequency	1	–	22.1184	MHz
External clock		X_{IN} input frequency	1	–	22.1184	MHz

Table 14-7. Main Oscillator Clock Stabilization Time (t$_{ST1}$)

(T_A = $-$ 20 $^\circ$C + 85 $^\circ$C, V_{DD} = 4.5 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	V_{DD} = 4.5 V to 5.5 V	–	–	20	ms
Ceramic	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	10	ms

NOTE: Oscillation stabilization time (tST1) is the time required for the CPU clock to return to its normal oscillation frequency after a power-on occurs, or when Stop mode is released by a RESET signal.

Figure 14-5. Frequency VS. Voltage

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15 MECHANICAL DATA

OVERVIEW

The S3C8075 microcontroller is available in a 64-pin SDIP package (64-SDIP-750) and a 64-pin QFP package (64-QFP-1420F).
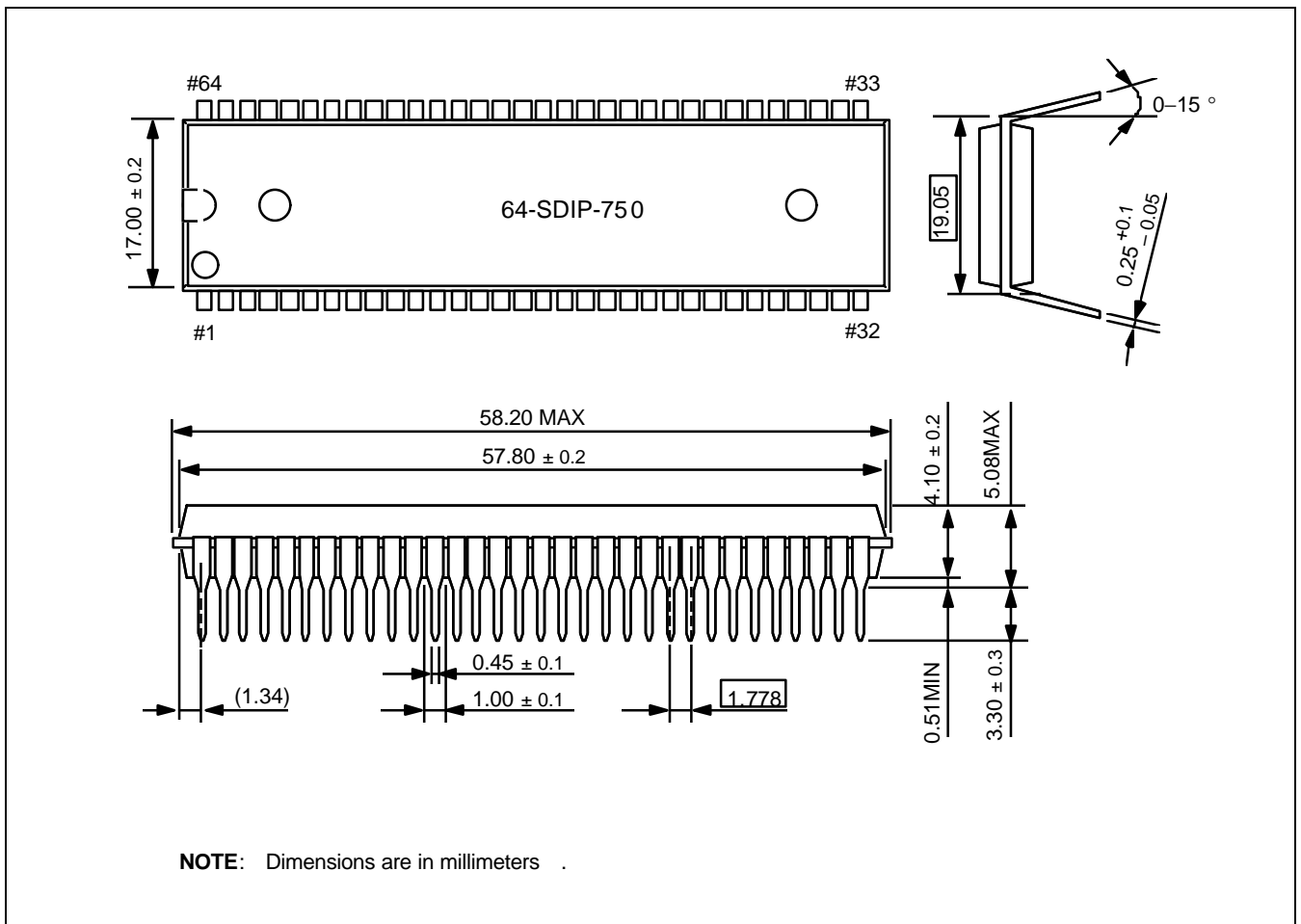

Figure 15-1. 64-SDIP-750 Package Dimensions

13.20 ± 0.3

10.00 ± 0.2

13.20 ± 0.3

10.00 ± 0.2

44-QFP-1010B

#44

#1

0.35 $^{+0.10}_{-0.05}$

0.80

(1.00)

0-8°

0.15 $^{+0.10}_{-0.05}$

0.80±0.20

0.10 MAX

0.05 MIN

2.05 ± 0.10

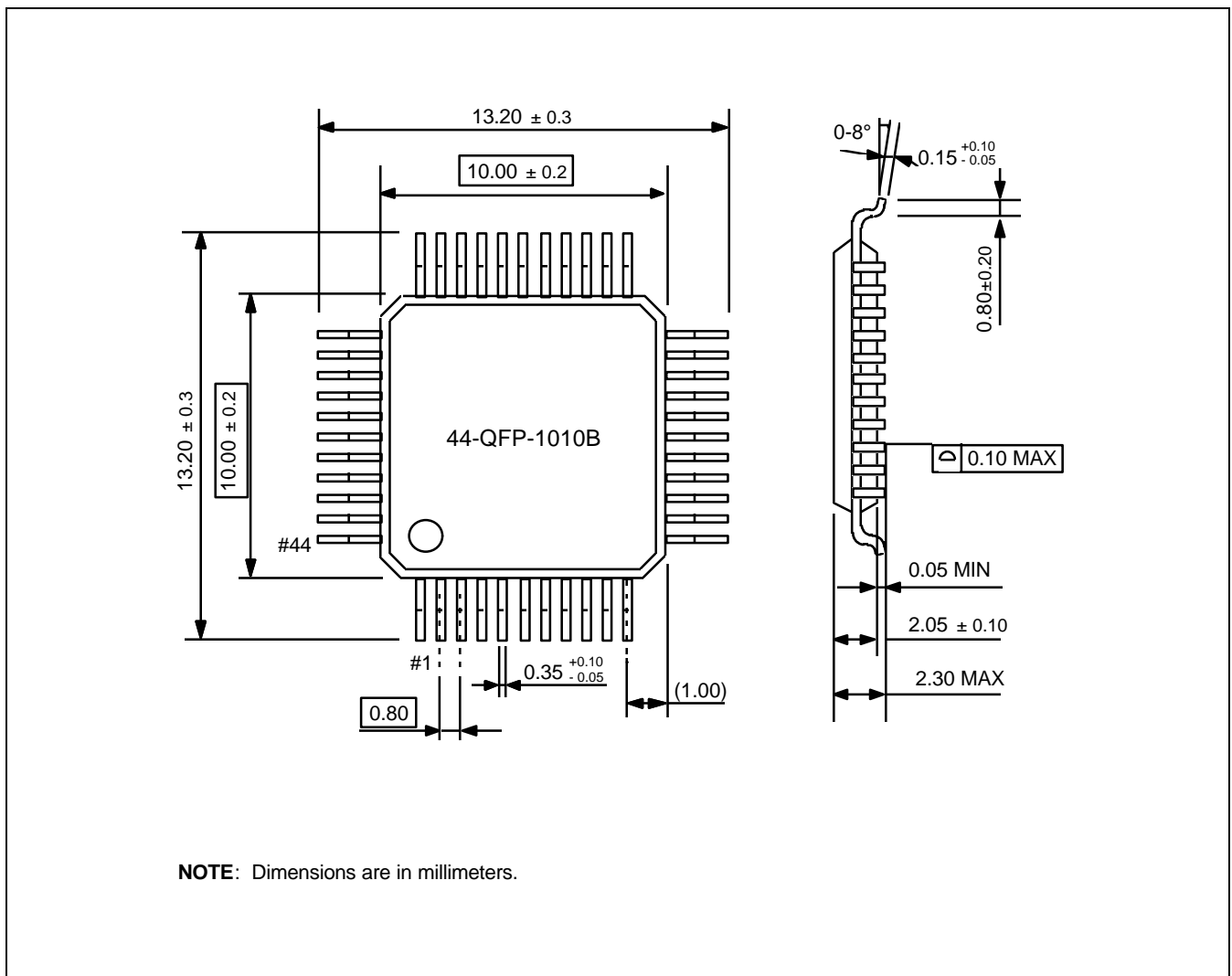2.30 MAX

NOTE: Dimensions are in millimeters.

Figure 15-2. 64-QFP-1420F Package Dimensions

16 S3P8075 OTP

OVERVIEW

The S3C8075 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C8075 microcontrollers. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by serial data format.

S3P8075 is fully compatible with S3C8075, both in function and in pin configuration. As it has simple programming requirements, S3P8075 is ideal for use as an evaluation chip for the S3C8075.
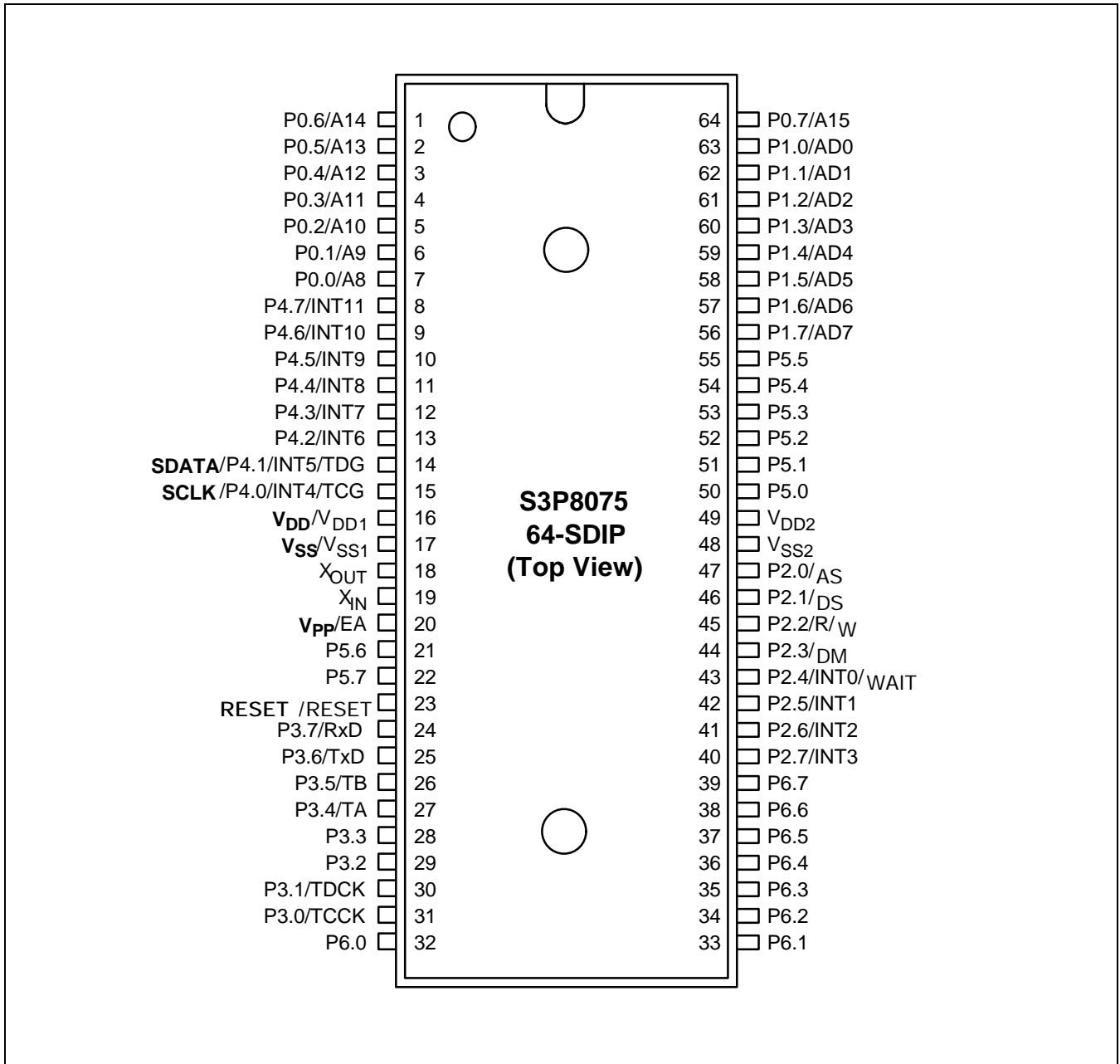
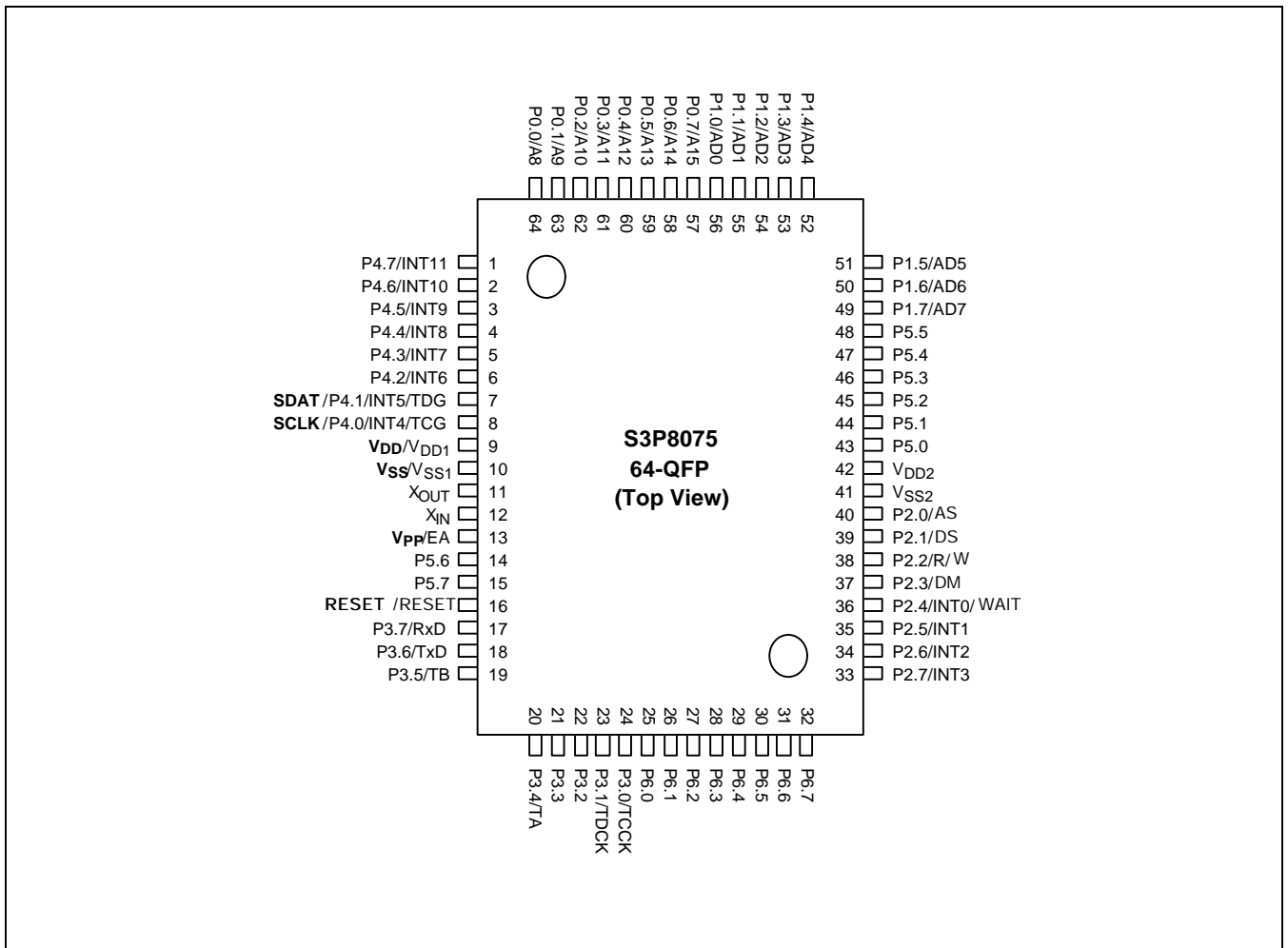**Figure 16-1. S3P8075 Pin Assignments (64-SDIP Package)**

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Figure 16-2. S3P8075 Pin Assignments (64-QFP Package)

Table 16-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P4.1	SDAT	14 (7)	I/O	Serial Data Pin (Output when reading, Input when writing) Input and Push-pull Output Port can be assigned.
P4.0	SCLK	15 (8)	I	Serial Clock Pin (Input Only Pin)
EA	V_{PP}	20 (13)	I	EPROM Cell Writing Power Supply Pin (Indicates OTP Mode Entering) When writing 12.5V is applied and when reading 5 V is applied (Option).
RESET	RESET	23 (9)	I	Chip Initialization
V_{DD1}/V_{SS1}	V_{DD}/V_{SS}	16/17 (9/10)	I	Logic Power Supply Pin. V_{DD} should be tied to 5V during programming.

NOTE: Parentheses indicate 64-QFP pin number.

Table 16-2. Comparison of S3P8075 and S3C8075 Features

Characteristic	S3P8075	S3C8075
Program Memory	16 Kbyte EPROM	16 Kbytes mask ROM
Operating Voltage (V_{DD})	2.7 V to 5.5 V	2.7 V to 5.5V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5V	
Pin Configuration	64 SDIP, 64 QFP	64 SDIP, 64 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of S3P8075, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 15-3 below.

Table 16-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/ MEM	ADDRESS (A15–A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

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D.C. ELECTRICAL CHARACTERISTICS

Table 16-4. D.C. Electrical Characteristics

$(T_A = -40 \,°C \text{ to } +85 \,°C, V_{DD} = 2.7 \text{ V to } 5.5 \text{ V})$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	All input pins except V_{IH2}	$0.8 \, V_{DD}$		V_{DD}	V
	V_{IH2}	X_{IN}	$V_{DD} - 0.5$			
Input Low Voltage	V_{IL1}	All input pins except V_{IL2}			$0.2 \, V_{DD}$	V
	V_{IL2}	X_{IN}			0.4	
Output High Voltage	V_{OH1}	$V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$ $I_{OH} = -4 \text{ mA}$ Port 5, 6	$V_{DD} - 1.0$			V
	V_{OH2}	$V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$ $I_{OH} = -1 \text{ mA}$ All output pins except port 5, 6	$V_{DD} - 1.0$			
Output Low Voltage	V_{OL1}	$V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$ $I_{OL} = 15 \text{ mA}$ Ports 5 and 6			1.0	V
	V_{OL2}	$I_{OL} = 2 \text{ mA}$ Ports 0 - 4			0.4	

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Table 16-4. D.C. Electrical Characteristics (Continued)

$(T_A = -40\ ^\circ C\ to\ +85\ ^\circ C, V_{DD} = 2.7\ V\ to\ 5.5\ V)$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High Leakage Current	I_{LIH1}	$V_{IN} = V_{DD}$ All input pins except X_{IN}, X_{OUT}	–	–	3	uA
	I_{LIH2}	$V_{IN} = V_{DD}$, X_{IN}, X_{OUT}			20	
Input Low Leakage Current	I_{LIL1}	$V_{IN} = 0\ V$ All input pins except X_{IN}, X_{OUT}	–	–	– 3	uA
	I_{LIL2}	$V_{IN} = 0\ V$, X_{IN}, X_{OUT}			– 20	
Output High Leakage Current	I_{LOH}	$V_{OUT} = V_{DD}$ All output pins	–	–	5	uA
Output Low Leakage Current	I_{LOL}	$V_{OUT} = 0\ V$	–	–	– 5	uA
Pull-up Resistor	R_{L1}	$V_{IN} = 0\ V$; $V_{DD} = 5\ V$ Ports 0, 1, 4, 5 and 6	30	47	70	$K\Omega$
	R_{L2}	$V_{IN} = 0\ V$; $V_{DD} = 5\ V$ RESET only	110	210	310	
Supply Current [1]	I_{DD1} [2]	$V_{DD} = 5\ V \pm 10\%$ 12-MHz oscillation	–	12	25	mA
		4-MHz oscillation		4.5	10	
		$V_{DD} = 3\ V \pm 10\%$ 12-MHz oscillation		6	15	
		4-MHz oscillation		2.5	7	
	I_{DD2} [2]	Idle mode; $V_{DD} = 5\ V \pm 10\ \%$ 12-MHz oscillation		2.5	6	
		4-MHz oscillation		1.5	4	
		Idle mode; $V_{DD} = 3\ V \pm 10\ \%$ 12-MHz oscillation		1.2	3	
		4-MHz oscillation		0.6	1.5	
	I_{DD3}	Stop mode: $V_{DD} = 5\ V \pm 10\ \%$		0.1	3	uA

NOTES:

1. Supply current does not include current drawn through internal pull-up resistors or external output current loads.
2. At supply current, the CPU clock frequency is the same as oscillation frequency (CPU use non divided clock).
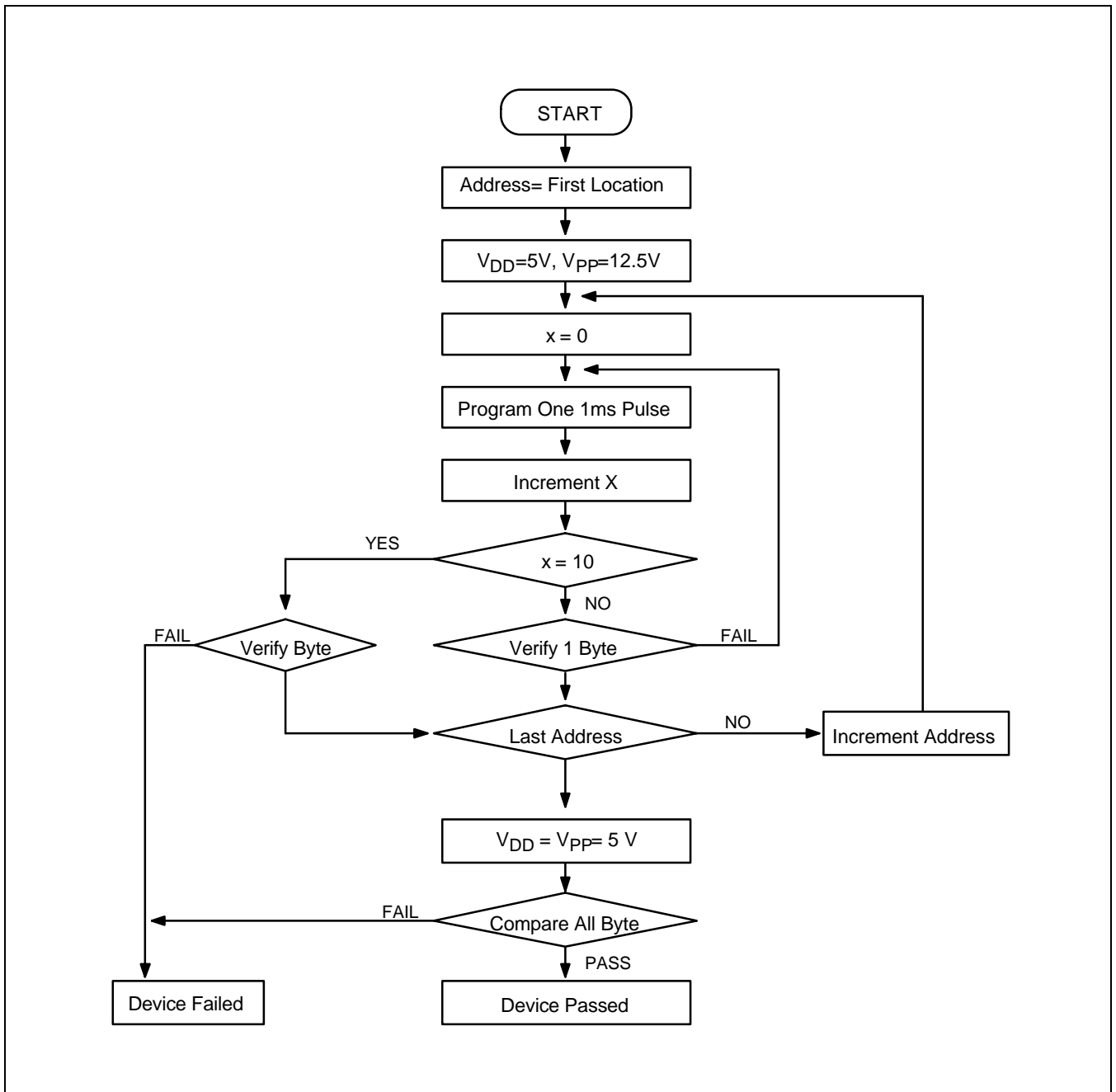
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Figure 16-3. OTP Programming Algorithm

NOTES

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